Pierre Auger Observatory

Surface Detector Electronics Upgrade
UUB Electrical Interface Control Document (EICD)

Abstract:
This document describes the electrical interfaces of the Upgraded Unified Board (UUB).

Document written by:	P. Stassi Project System engineer	*Agreed by:*	T. Suomijärvi Task leader
Date:	*17 January 2018*	*Date:*	*17 January 2018*
Local Reference:	*ATRIUM-2223*	*Project Reference:* *EDMS Reference:*	*WP10-LPSC-05H* *1760315*

Table of Content

ACRONYMS

ADC	Analog to Digital Converter
BGA	Ball Grid Array
CR	Configurational Requirement
DC	Direct Current
EICD	Electrical Interface Control Document
ER	Environmental Requirement
FPGA	Full Programmable Gate Array
FR	Functional Requirements
GPS	Global Positioning System
ICD	Interfaces Control Document
IR	Interface Requirements
JTAG	Joint Test Action Group
n/a	non applicable
OR	Operational Requirements
PBS	Product Breakdown Structure
PCB	printed Circuit Board
PR	Physical Requirements
QR	Quality Requirements
SDE	Surface Detector Electronics
SR	Support Requirements
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UB	Unified Board
UC	Upgrade Committee
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VM	Verification Matrix

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
05	A	18/04/13		DRAFT for approbation
05	B	14/10/13	Stassi	Post Lisbon meeting updates
05	C	10/11/13	Stassi	Post Orsay meeting updates
05	D	26/02/14	Stassi	Post Grenoble meeting update
05	E	28/11/14	Stassi	Post col. meeting Nov 2014 update
05	F	31/03/15	Stassi	Minors modifications
05	G	17/10/16	Stassi	Update before Auger Prime CDR
05	H	17/01/18	Stassi	PMT and digital connectors updates Proto version 2 updates

1 INTRODUCTION

This document describes the electrical interfaces of the Upgraded Unified Board (UUB).

1.1 Reference Documents

RD1 Upgraded UB Development plan, WP10LPSC02_SDEU_Dev_Plan
RD2 SDEU Specification, WP10LPSC03_SDEU_Specification

2 SDEU DIAGRAMS

2.1 SDEU Interaction diagram

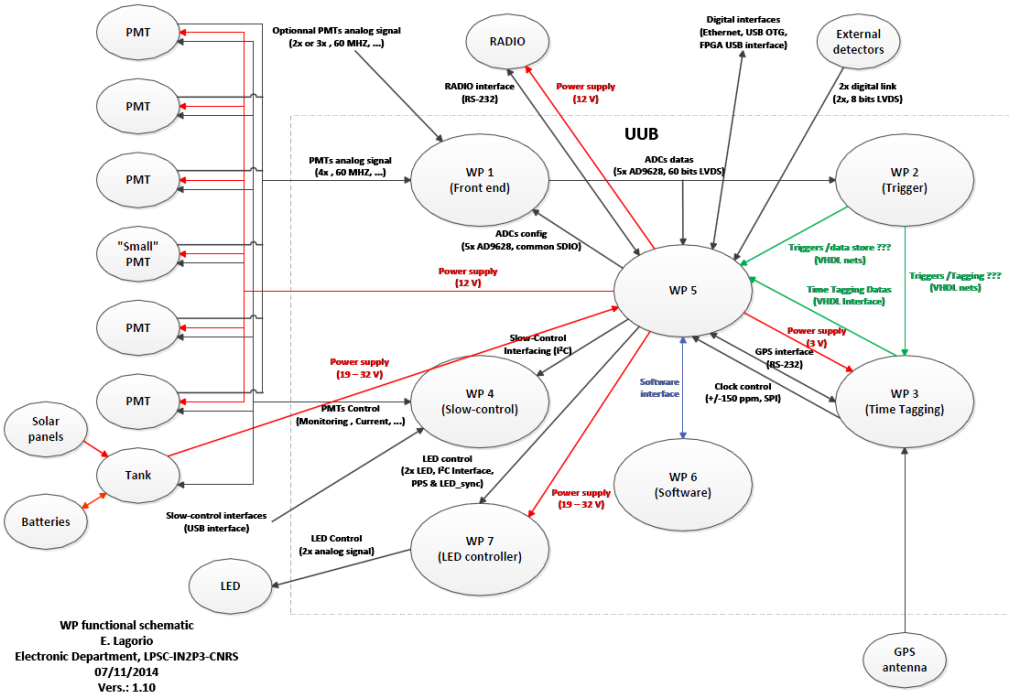


Figure 2.1.a: Interface configuration

2.2 UUB Interconnections diagram

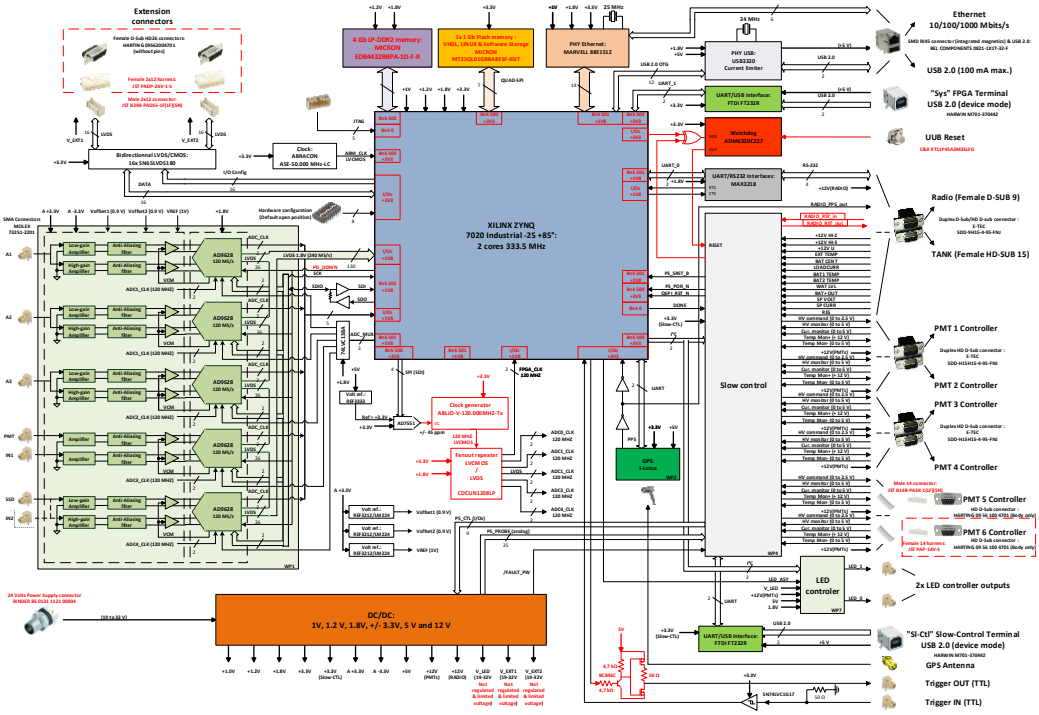


Figure 2.2.a: ***SDEU Functional Block Diagram***

3 UUB ELECTRICAL POWER DEMANDE

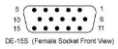
The table below shows the shows the electrical power demand for the UUB, taking into account the following assumption:

- DC-DC efficiency = 97%
- WP1 to WP4, values are maxima taken form datasheets.

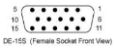
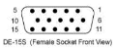
Work Package	Function	Device	Maximum current (mA) / power supply (V) / Device										Max Power / Device	Nb.	Power	Power / WP
			FPGA				Slow C	Analog		GPS	USB	Radio	PMT				
			1	1,2	1,8	3,3	3,3	3,3	-3,3	5	5	12	12				
WP1	Front-End	Anti aliasing filter (TBD)						0						0	3	0,00	
		Low-gain path filter proposal						0	0					0	3	0,00	
		High-gain path filter proposal						0	0					0	3	0,00	4514,70
		Dual Differential amplifier (ADA4927-2)						47,2	47,2					311,52	10	3115,20	
		12 bits ADC 120MS/s (Twin AD9628) proposal			155,5									279,9	5	1399,50	
WP2	Trigger	IN Digital Triggers (SN74LVC1G17)				0,5								1,65	1	1,65	
		OUT Digital Triggers (SN74LVC1G125)				0,5								1,65	1	1,65	56,10
		Test connector (32 signal,) (2x 74LCX16245)				8								26,4	2	52,80	
WP3	Time Tagging	GPS (I-LOTUS: ref ???)				52								171,6	1	171,60	301,60
		Antenna (Type II ref ???)								26				130	1	130,00	
WP4	Slow Control	µ-controller (MPS430F2618)					9,5							31,35	1	31,35	
		LED flasher controller (DAC 4 outputs : AD5624)					0,85							2,805	1	2,81	
		DAC (LTC2637-12)					1,3							4,29	1	4,29	67,55
		Ampliers (LT1112)					0,88							2,904	10	29,04	
		MUX (ADG608)					0,01							0,0165	4	0,07	
WP5	VCO/ fanout/ Clock_ADC	**Clock generator (with VCO control) & DAC :**															
		Clock generator with external VCO control (CDCEL913)			11,7									21,06	1	21,06	
		LVDS double fanout repeater (CDCUN1208LP)			85									153	1	153,00	
		DAC VCO control (AD7390 & REF3318: Rail to Rail)				1,5								4,95	1	4,95	
	FPGA (and µP)	Xilinx ZYNQ 7020 Industrial : 2 cores 333.5Mhz BRA	1864,8	150,15	432,6									2823,66	1	2823,66	
	Extention connector	**interface used an external electronic:**															
		Driver (2x DS90LV047ATM)				15								49,5	4	198,00	
		Receiver differential (DS90LV048ATM)				37								122,1	4	488,40	
	Watchdog/ RESET/ Clock CPU	WATCHDOG : MAX823EUK-S				0,012								0,0396	1	0,04	4799,96
		RESET : MAX811EUS-S				0,01								0,033	1	0,03	
		ABRACON ASE-50,000MHz-LC				19								62,7	1	62,70	
	Control	Switches												0	2	0,00	
	System Memory	LP-DDR2 Low Power4 Gb: MICRON MT42L128M32D1LF-25		210	10									270	1	270,00	
	Flash Memory	1 Gb : µ N25Q00AA13GSF40 @ 3.3 V (Wr cycle)				20								66	1	66,00	
	Interfaces	Radio RS232 (MAX3218)			3									5,4	1	5,40	
		Terminal USB interface (FT232R, powered by USB link)												0	2	0,00	
		Ethernet phy (MARVELL 88E1510 in EEE mode	14		35	14								123,2	1	123,20	
		USB (USB3320)			46,4									83,52	1	83,52	
		External Slave USB Power									100			500	1	500,00	
WP?	PMT 1,2 & 3 PMT	Main PMT											44,44	533,28	3	1599,84	
		Small PMT (ESTIMATE POWER)											44,44	533,28	1	533,28	5632,32
WP?	RADIO											291,6		3499,2	1	3499,20	
		Total Current / power supply (mA) :	1878,8	360,15	1401,2	331,522	20,47	472	472	26	100	291,6	177,76	**Total power (mW):**		**15372,23**	
		DC/DC efficiency (%) :	93,00	89,10	93,50	94,00	87,00	93,30	82,20	90,90	94,10						
		Power for under 7V power supply (mW) :	2020,22	485,051	2697,5	1163,85	77,6448	1669,45	1894,89	143,014	531,35						
		DC/DC efficiency (%) :	97,10%									97,50%	97,00%				
		Power (mW) :	11002,03									3588,92	2199,09				
		Internal Total Power (SDEU only) :	**16 790,04 mW**														
		Total Power (including 6,4 watts power for external devices) :	**23,19 W**														

Table 3.a: ***SDEU power budget estimation***

4 UUB CONNECTORS LIST

Connector Ref.	Schemat. Ref	Connector Type	Connector Function	Connected to	Comment
J11	PX1-3	SMA, socket 	In, Anode PMT1	PMT Anode 1	On front panel
J12	PX1-4		In, Anode PMT2	PMT Anode 2	On front panel
J13	PX1-5		In, Anode PMT3	PMT Anode 3	On front panel
J14	PX1-2		In, Anode Small PMT	Small PMT An.	On front panel
J15	PX2-2		In, Analog 1	Scint. detector 1	On front panel
J16	PX1-1		In, Analog 2	Scint. detector 2	On front panel
J17	PX2-1		In, Analog 3	Ext. detector 3	On front panel
J21		DB15HD socket 	In/Out, PMT1 monitoring	PMT base 1	On front panel
J22	J14		In/Out, PMT2 monitoring	PMT base 2	On front panel
J23	J4		In/Out, PMT3 monitoring	PMT base 3	On front panel
J24	J5		In/Out, Small PMT monitoring	Small PMT base	On front panel
J25	J6	B14B-PASK-1(LF)(SN) 1x14 pin 	In/Out, PMT 5 monitoring	PMT base 5	On board, connected to DB15S HD on front panel
J26	J7		In/Out, PMT 6 monitoring	PMT base 6	
J31	U4A	DB15HD socket	In, Slow control sensors reading	TPCB	On front panel
J41	J2	10 pin (2x5) socket 	In/Out, GPS power and com.	GPS board	On board, connected to the GPS receiver board
J51	J1	Binder 99-3431-202-04 	In, 24V power supply	TPCB	On front panel
J61	PX3	SMA, socket 	Out, LED Flasher 1 cde.	LED Flasher 1	On front panel
J62	PX4		Out, LED Flasher 2 cde.	LED Flasher 2	On front panel
J71	PX2		In, External trigger input	TBD	On front panel
J72	PX1		Out, Internal trigger output	TBD	On front panel
J81	J12	USB Type B, Socket 	In/Out, System com.	Maintenance	On front panel
J82	J13		In/Out, Slow Control com.	Maintenance	On front panel
J83	CO1B	USB Type A, Socket 	In/Out, maintenance	Maintenance	On front panel 100 mA maxi
J84	CO1A	RJ45, Socket 	In/Out, Ethernet	Maintenance	On front panel
J85	U2	SUBD9, socket 	In/Out, Radio interface	BSRU (radio)	On front panel
J91	J7	B24B-PADSS-1F(LF)(SN) 2x12 pins socket 	In/Out, and out power supply	TBD	On board, connected to DB26S HD on front panel
J92	J9		In/Out, and out power supply	TBD	
J93	J6	HE14 2x7 pin 	In/Out, Jtag system (FPGA)	Maintenance	On board
J94			In/Out, Jtag system (Slow Cont.)	Maintenance	On board

5 UUB CONNECTORS PIN ALLOCATION (RD2)

Conn. ID	*Name*	*Signal Name*	*Pin[1] #*	*Direction*	*Signal description*	*Connector type*
J11	PMT A1	Anode PMT1	n/a	IN	50Ω, -2V Fs	SMA, socket 
J12	PMT A2	Anode PMT2	n/a	IN	50Ω, -2V Fs	
J13	PMT A3	Anode PMT3	n/a	IN	50Ω, -2V Fs	
J14	PMT 4	PMT4	n/a	IN	50Ω, -2V Fs	
J15	DET IN1	Input 1	n/a	IN	50Ω, -2V Fs	
J16	DET IN2	Input 2	n/a	IN	50Ω, -2V Fs	
J17	DET IN3	Input 3	n/a	IN	50Ω, -2V Fs	
J21 J22 J23 J24	PMT 1 Monit. PMT 2 Monit. PMT 3 Monit. PMT 4 Monit[2].	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	
J25 J26	PMT 5 Monit PMT 6 Monit	HV command	5	OUT	DC, 0 to 2.5V	B14B-PASK-1(LF)(SN) 1x14 pin 
		HV monitor	2	IN	DC, 0 to 5V	
		Cur. monitor	8	IN	DC, 0 to 5V	
		Temp. Mon +	11	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	NC	n/a	Not currently used	
		NC	NC	n/a	Not currently used	
		+12V	14	OUT	DC, +12V	
		GND	1	n/a	Ground	
		GND	3	n/a	Ground	
		GND	6	n/a	Ground	
		GND	12	n/a	Ground	
		GND	4	n/a	Ground	
		GND	10	n/a	Ground	
		GND	13	n/a	Ground	
J31	Slow Control	+12V HI-1	5	OUT	DC +12V through 1KΩ	DB15HD socket 
		+12V HI-2	4	OUT	DC +12V through 1KΩ	
		+12V HI-3	2	OUT	DC +12V through 1KΩ	
		+12V LI	1	OUT	DC +12V through 22KΩ	
		EXT TEMP	7	IN	0 to +5 V	
		BAT CENT	3	IN	0 to +5 V	
		LOADCURR	8	IN	0 to +5 V	
		BAT1 TEMP	9	IN	0 to +5 V	
		BAT2 TEMP	10	IN	0 to +5 V	
		WAT LVL	11	IN	0 to +5 V	
		BAT+ OUT	12	IN	0 to +5 V	
		SP VOLT	13	IN	0 to +5 V	
		SP CURR	14	IN	0 to +5 V	
		Not Used	15	n/a	Not Used	
		GND	6	n/a	GND	

[1] From the UUB point of view only
[2] Small PMT.

Conn. ID	*Name*	*Signal Name*	*Pin[1] #*	*Direction*	*Signal description*	*Connector type*
J41	GPS Board	RxD1	1	IN	Receive Data (3V logic)	10 pin (2x5) socket 
		TxD1	2	OUT	Transmit Commands (3V logic)	
		+3V PWR	3	OUT	Regulated 3Vdc supply	
		1PPS	4	IN	1 pulse-per-second input	
		Ground	5	n/a	Signal and Power common	
		Battery	6	OUT	Optional External Backup	
		Reserved	7	n/a	Not currently used	
		RTCM In	8	OUT	RTCM correction output	
		Antenna Bias	9	OUT	3V-5V antenna bias output	
		Reserved	10	n/a	Not currently used	
J51	Main Power	24VDC	1	IN	DC, +20 to +30V	Binder 99-3431-202-04 
		GND	2	n/a	n/a	
J61	LED FLASH 1	Uout 1	n/a	OUT	+0 to +20V	SMA, socket 
J62	LED FLASH 2	Uout 2	n/a	OUT	+0 to +20V	
J71	External Trigger	EXT TRIG	n/a	IN	TTL	
J72	Internal Trigger	INT TRIG	n/a	OUT	TTL	
J81	USB SYS	VCC	1	OUT	+5V	USB Type B, Socket 
		D-	2	IN/OUT	Data -	
		D+	3	IN/OUT	Data +	
		GND	4	n/a	GND	
J82	USB Slow Ctrl	VCC	1	OUT	+5V	
		D-	2	IN/OUT	Data -	
		D+	3	IN/OUT	Data +	
		GND	4	n/a	GND	
J83	USB OTG	VCC	1	OUT	+5V (100mA maxi)	USB Type A, Socket 
		D-	2	IN/OUT	Data -	
		D+	3	IN/OUT	Data +	
		GND	4	n/a	GND	
J84	Ethernet	T+	1	OUT	Transmit +	RJ45, Socket 
		T-	2	OUT	Transmit -	
		R+	3	IN	Receive +	
		NC	4	n/a	Reserved	
		NC	5	n/a	Reserved	
		R-	6	IN	Receive -	
		NC	7	n/a	Reserved	
		NC	8	n/a	Reserved	
J85	TELECOM[3]	SU PWR	1	OUT	SU Power, DC +12V (14V, max)	SUBD9, socket 
		SU RXD	2	OUT	SU TXD	
		SU TXD	3	IN	SU RXD	
		1PPS	4	IN	SU Reset out, see SU spec., RD2	
		GND	5	n/a	Ground	
		TELRESCPU	6	OUT	One pulse per second,+3.3V	
		RTS	7	IN	SU CTS	
		CTS	8	OUT	SU RTS	
		CPURESTEL	9	OUT	SU Reset in, see SU spec., RD2	

[3]For UUB prototype version 1 point of view **only**, external Telecom cable is cross wired on pins 2 & 3, 4 & 6 and 7 & 8.

J91 J92	EXT 1 EXT 2	D1+	1	IN or OUT	Configurable	B24B-PADSS-1F(LF)(SN) 2x12 pins socket 
		D1-	2	IN or OUT	Configurable	
		VCC[4]	**6**	OUT	+24V, unregulated, switchable	
		GND	**5**	n/a	Ground	
		D0+	3	IN or OUT	Configurable	
		D0-	4	IN or OUT	Configurable	
		D2+	7	IN or OUT	Configurable	
		D2-	8	IN or OUT	Configurable	
		NC	-	n/a	NC	
		NC	-	n/a	NC	
		D4+	9	IN or OUT	Configurable	
		D4-	10	IN or OUT	Configurable	
		D3+	13	IN or OUT	Configurable	
		D3-	14	IN or OUT	Configurable	
		VCC[3]	**12**	OUT	+24V, unregulated, switchable	
		GND	**11**	n/a	Ground	
		D5+	15	IN or OUT	Configurable	
		D5-	16	IN or OUT	Configurable	
		D6+	19	IN or OUT	Configurable	
		D6-	20	IN or OUT	Configurable	
		VCC[3]	**18**	OUT	+24V, unregulated, switchable	
		GND	**17**	n/a	Ground	
		D7+	21	IN or OUT	Configurable	
		D7-	22	IN or OUT	Configurable	
		VCC[3]	**24**	OUT	+24V, unregulated, switchable	
		GND	**23**	n/a	Ground	

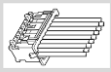
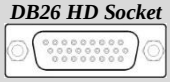
[4] 100 mA maximum per connector.

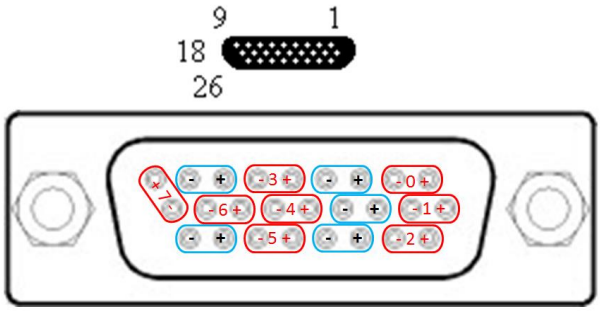
Conn. ID	*Name*	*Signal Name*	*Pin[5] #*	*Direction*	*Signal description*	*Connector type*
J93	JTAG System	GND	1	n/a	Ground	HE14 2x7 pin 
		+3.3V Bias	2	OUT	DC, +3.3 Volts	
		GND	3	n/a	Ground	
		JTAG TMS	4	IN	0 to +3.3V	
		GND	5	n/a	Ground	
		JTAG TCK	6	IN	0 to +3.3V	
		GND	7	n/a	Ground	
		JTAG TDO	8	OUT	0 to +3.3V	
		GND	9	n/a	Ground	
		JTAG TDI	10	IN	0 to +3.3V	
		GND	11	n/a	Ground	
		Not Used	12	n/a	Not currently used	
		GND	13	n/a	Ground	
		Not Used	14	n/a	Not currently used	
J94	JTAG Slow Ctrl	JTAG TDO	1	OUT	0 to +3.3V	HE14 2x7 pin 
		VCC OUT	2	OUT	DC, +3.3 Volts	
		JTAG TDI	3	IN	0 to +3.3V	
		VCC IN	4	IN	DC, +3.3 Volts	
		JTAG TMS	5	IN	0 to +3.3V	
		Not Used	6	n/a	Not currently used	
		JTAG TCK	7	IN	0 to +3.3V	
		Not Used	8	n/a	Not currently used	
		GND	9	n/a	Ground	
		Not Used	10	n/a	Not currently used	
		JTAG RST	11	IN	0 to +3.3V	
		Not Used	12	n/a	Not currently used	
		Not Used	13	n/a	Not currently used	
		Not Used	14	n/a	Not currently used	

Interconnections between onboard multipoint connectors and front panel connectors:

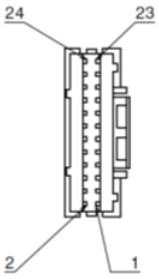
[5] From the UUB point of view only

Digital I/O connectors

UUB Conn. ID	*Name*	*Signal Name*	*•ST PADP-24V-01-S*  *Pin#*	*Front Panel connector DB26 HD Socket*  *Pin#*	*Signal description*
J91 J92	EXT 1 EXT 2	D1+	1	10	Configurable
		D1-	2	11	Configurable
		VCC	**6**	**3**	**+24V, unregulated, switchable**
		GND	**5**	**4**	**Ground**
		D0+	3	1	Configurable
		D0-	4	2	Configurable
		D2+	7	19	Configurable
		D2-	8	20	Configurable
		NC	**-**	**12**	**NC**
		NC	**-**	**13**	**NC**
		D4+	9	14	Configurable
		D4-	10	15	Configurable
		D3+	13	5	Configurable
		D3-	14	6	Configurable
		VCC	**12**	**21**	**+24V, unregulated, switchable**
		GND	**11**	**22**	**Ground**
		D5+	15	23	Configurable
		D5-	16	24	Configurable
		D6+	19	16	Configurable
		D6-	20	17	Configurable
		VCC	**18**	**7**	**+24V, unregulated, switchable**
		GND	**17**	**8**	**Ground**
		D7+	21	9	Configurable
		D7-	22	18	Configurable
		VCC	**24**	**25**	**+24V, unregulated, switchable**
		GND	**23**	**26**	**Ground**



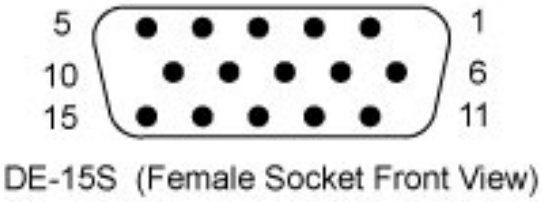
Front panel view

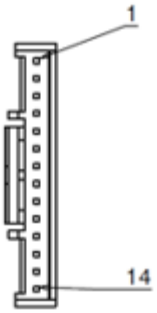


Top view

PMT 5 & 6, I/O connectors

UUB Conn. ID	***Name***	***Signal Name***	***JST PAP-14V-S Pin#***	***Front Panel connector DB15HD Socket Pin#***	***Signal description***
J25 J26	PMT 5 Monit. PMT 6 Monit.	HV command	5	2	DC, 0 to 2.5V
		HV monitor	2	1	DC, 0 to 5V
		Cur. monitor	8	3	DC, 0 to 5V
		Temp. Mon +	11	4	DC, +12V
		Temp Mon -	9	9	DC, 0 to 5V
		NC	NC	11	Not currently used
		NC	NC	13	Not currently used
		+12V	14	5	DC, +12V
		GND	1	6	Ground
		GND	3	7	Ground
		GND	6	8	Ground
		GND	12	10	Ground
		GND	4	12	Ground
		GND	10	14	Ground
		GND	13	15	Ground

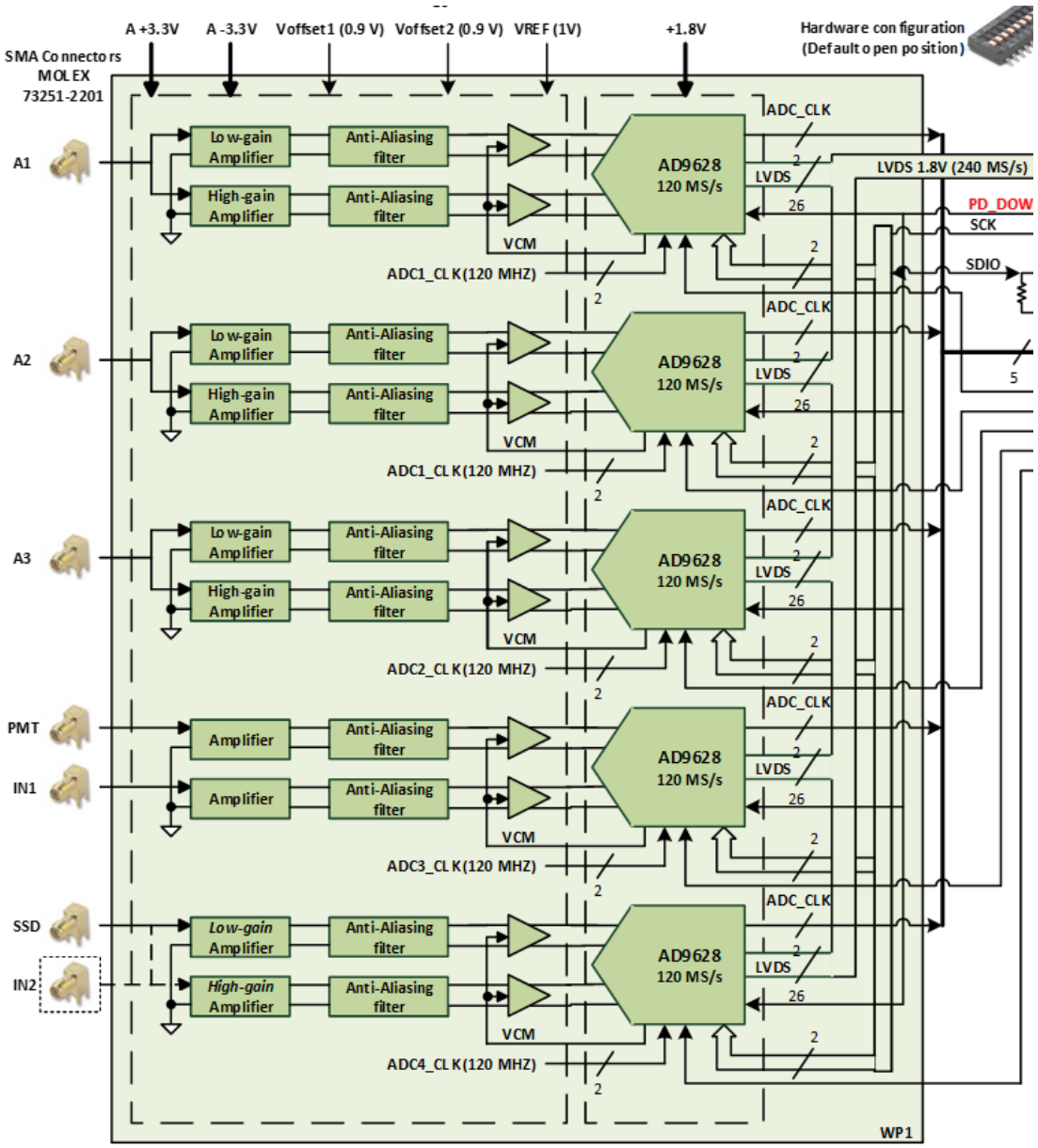




Top view

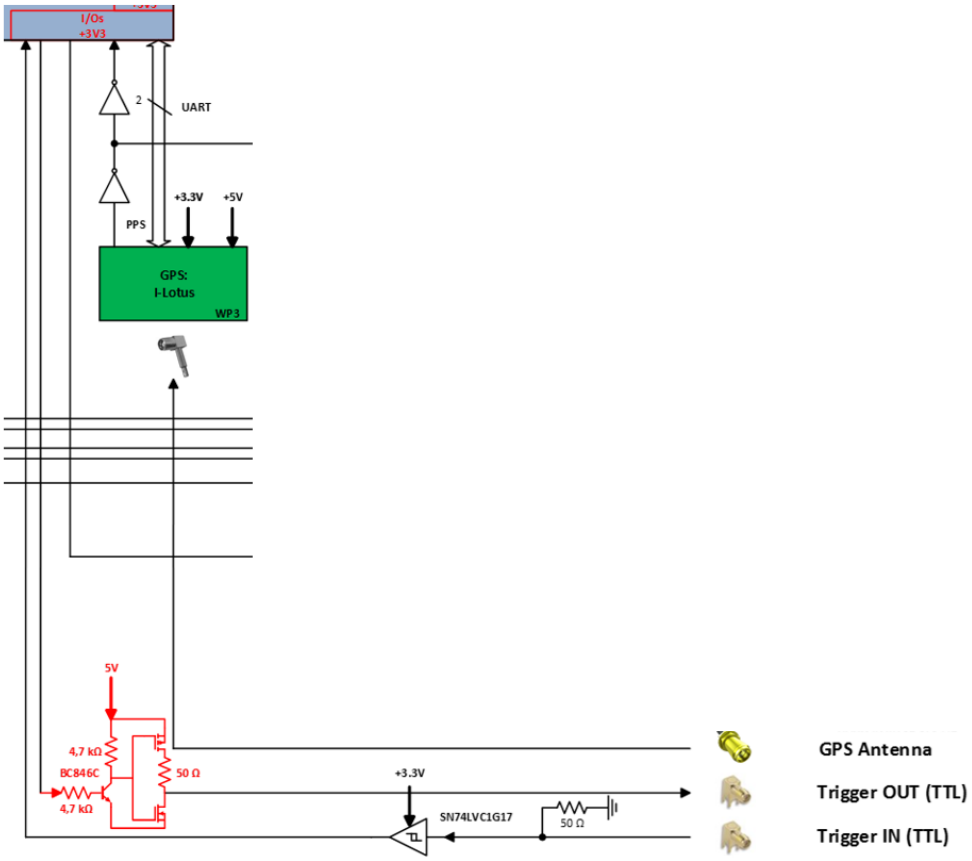
6 UUB ELECTRICAL INTERFACES DESCRIPTION

6.1 Analog input interfaces

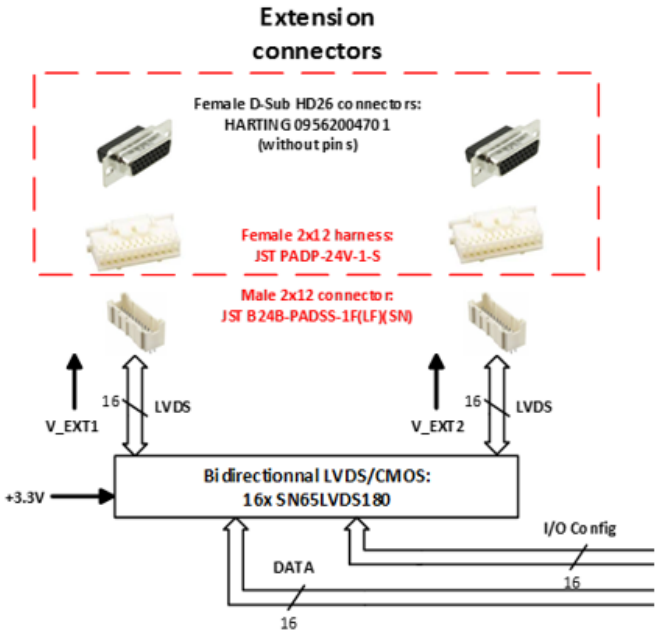


6.2 Digitals interfaces

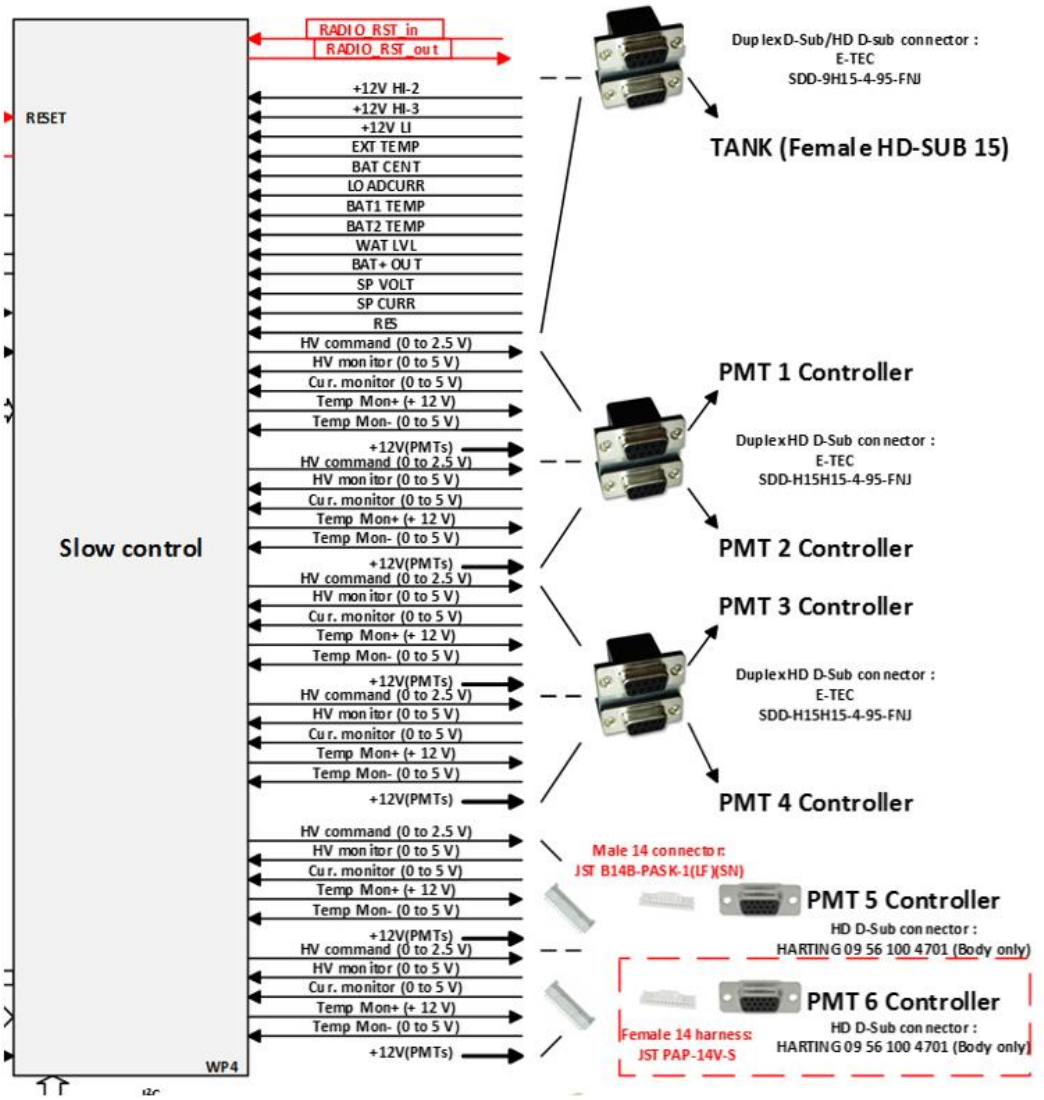
6.2.1 GPS Board and Trigger



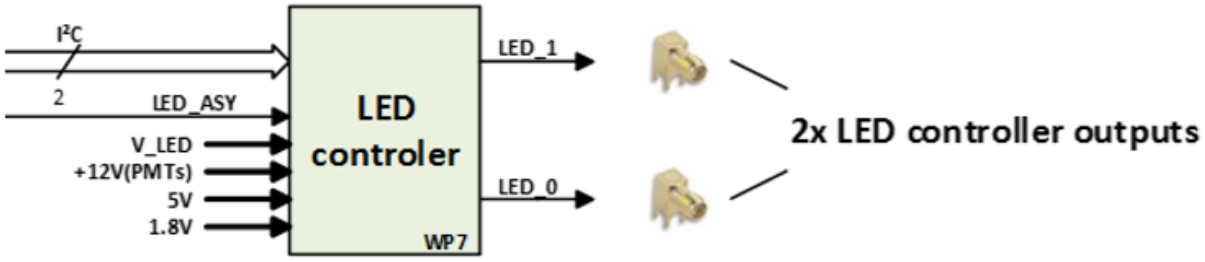
6.2.2 External detectors



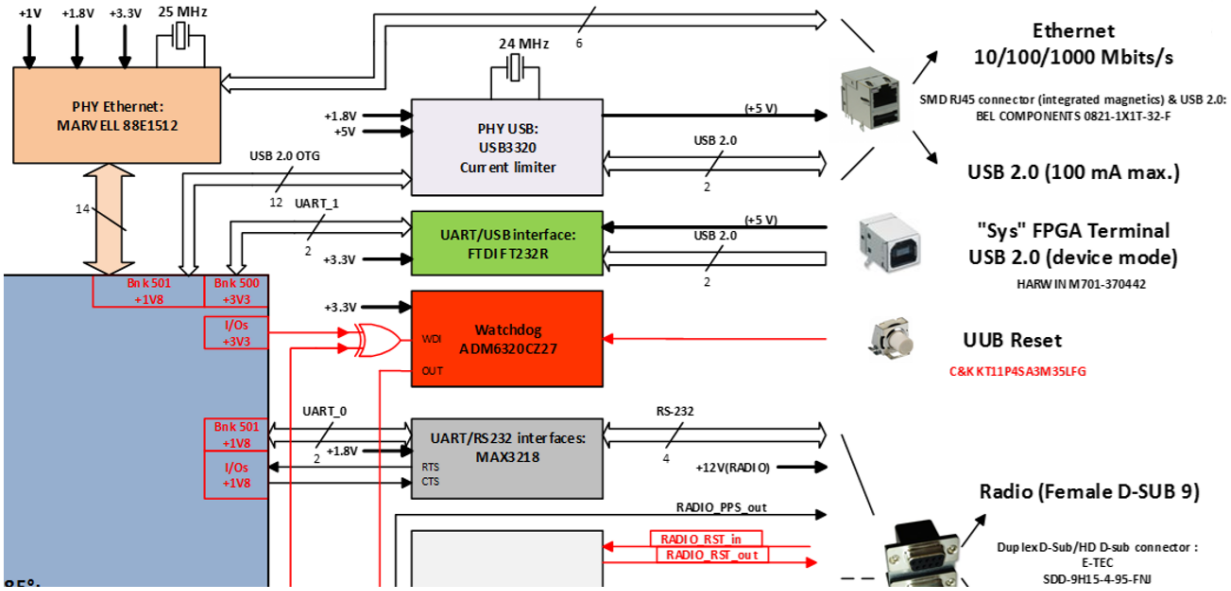
6.3 *Slow Control interfaces*

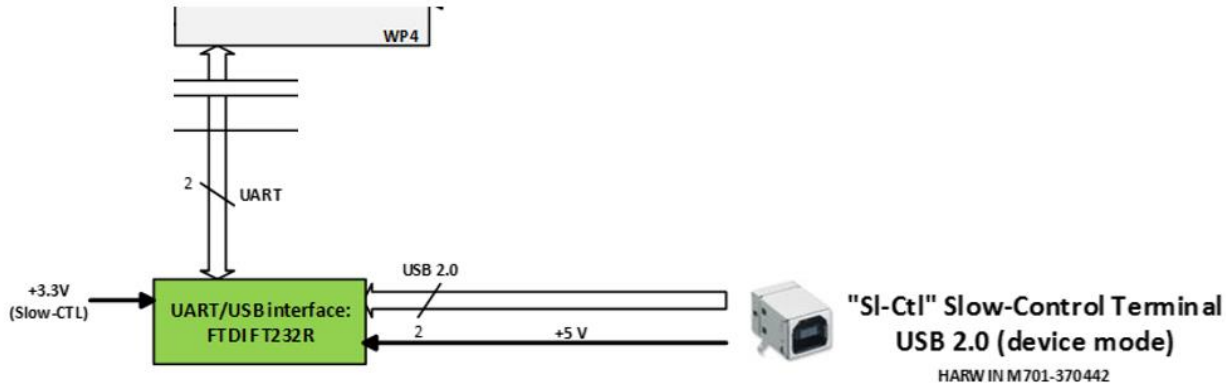


6.1 *LED Controller*



6.2 Communication interfaces





6.3 *Power interface*