

AUGER: SURFACE DETECTOR ELECTRONIC UPGRADE

VERSION: 1.12

DATE: 21/03/2016

BILL OF MATERIAL: X002-002-IE00-VA01



PIERRE
AUGER
OBSERVATORY

REF: /CAO-PROJETS/SPB16X/LAGORIO/AUGER/SDEU/IE00/

LPSC
53, AVENUE DES MARTYRS
38026 GRENOBLE CEDEX
+33 (0)4.76.28.41.65

ETUDE: SDEU

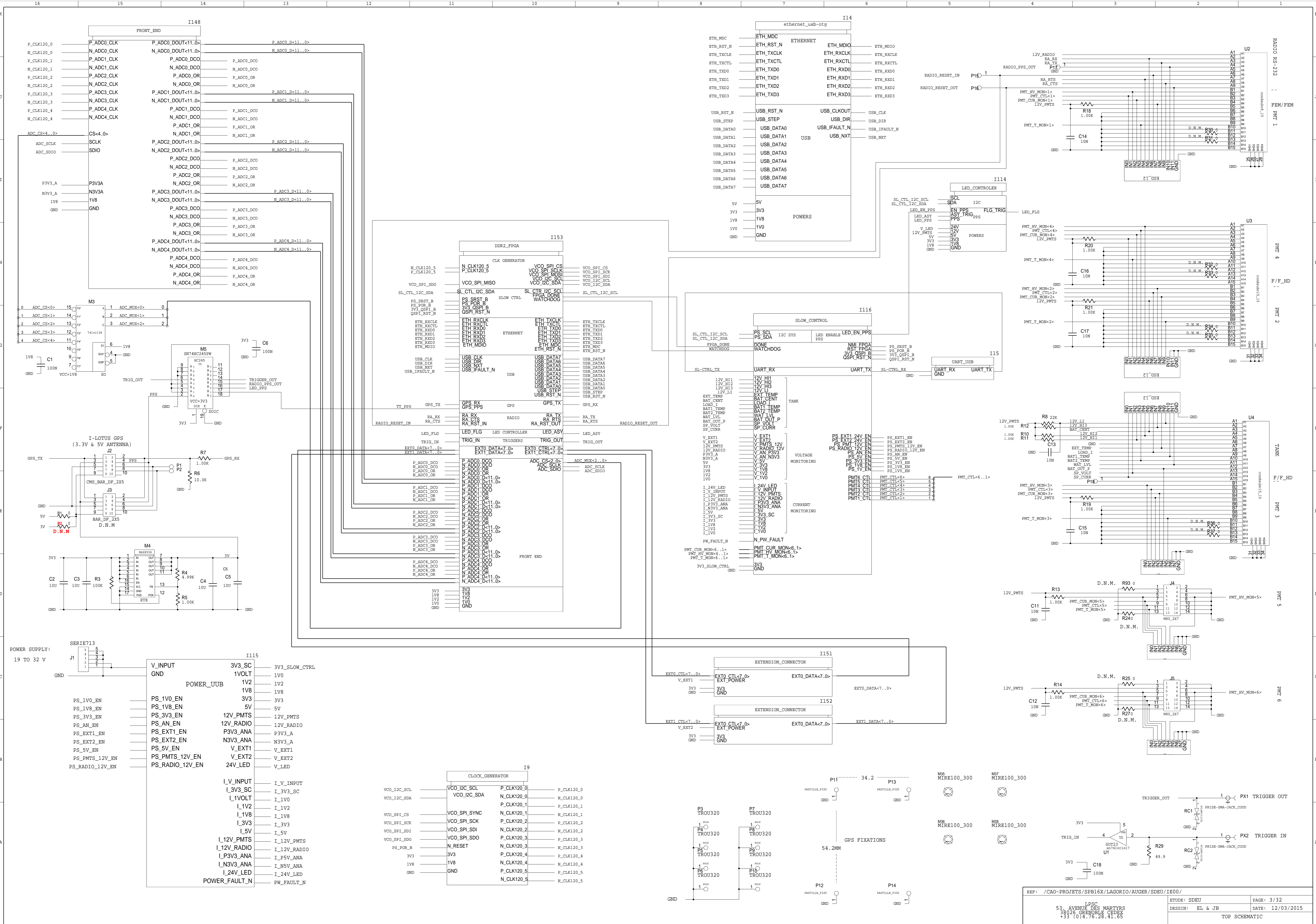
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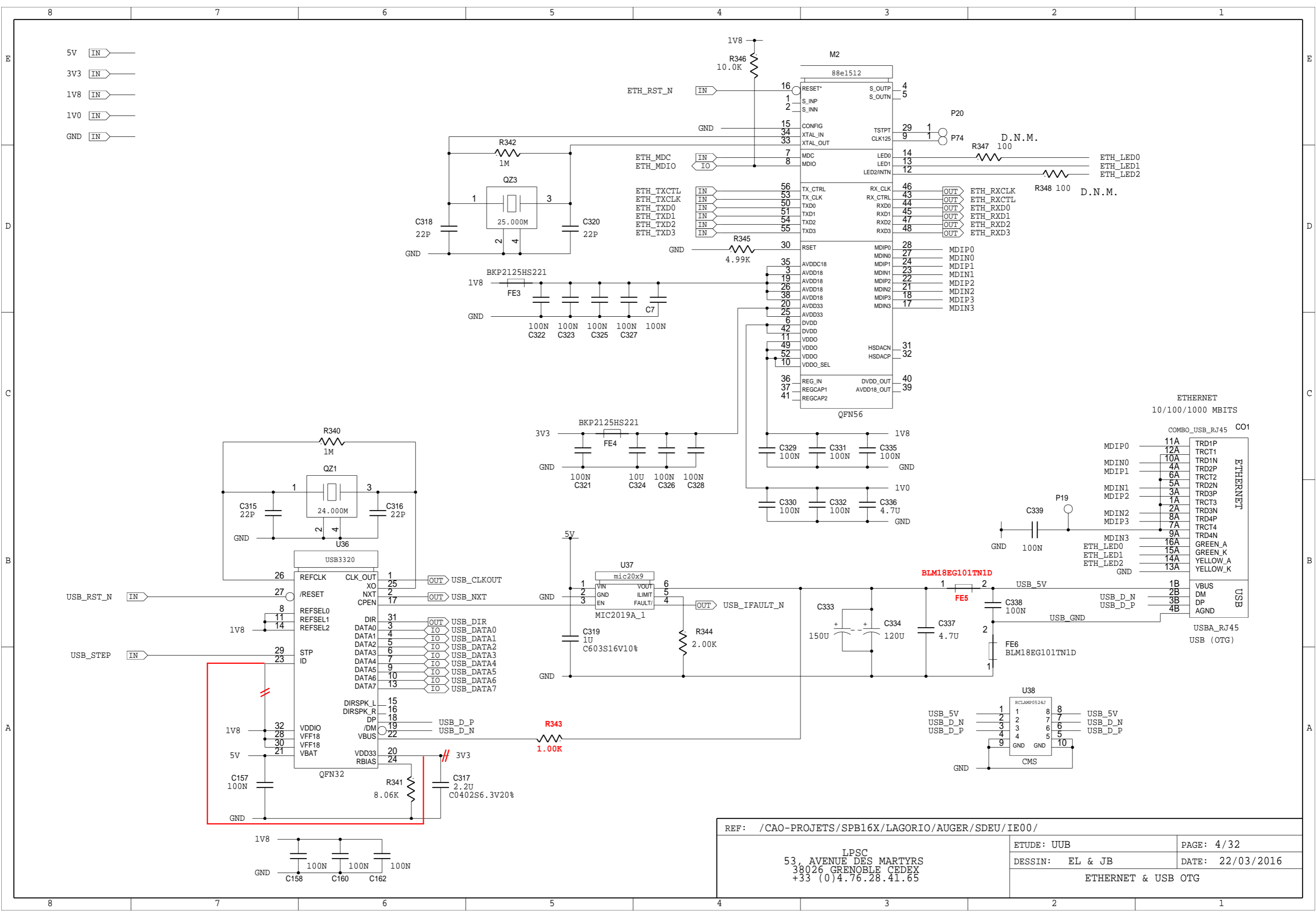
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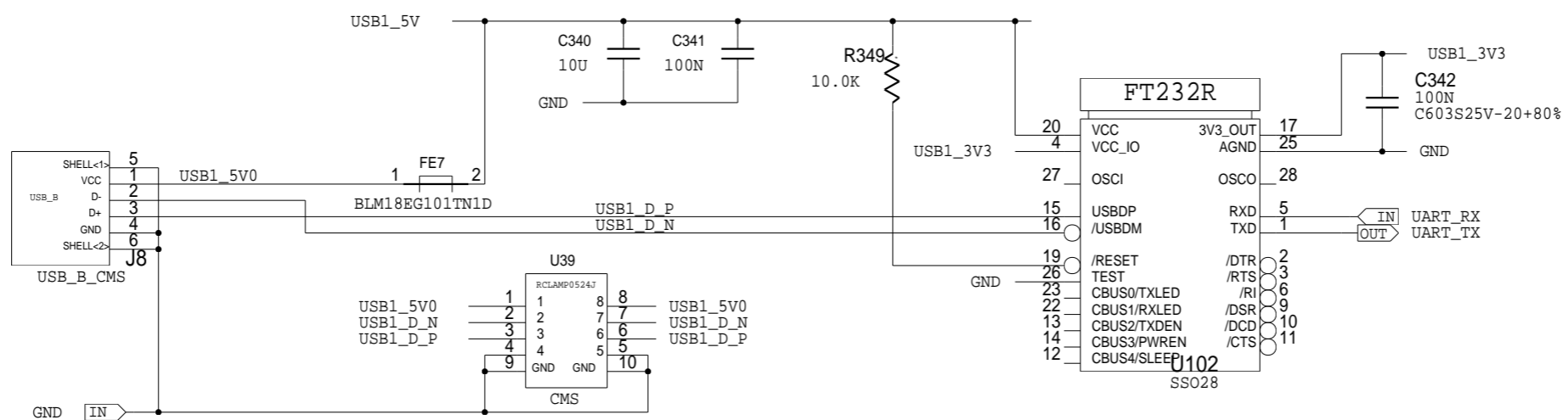
DATE: 22/03/2016

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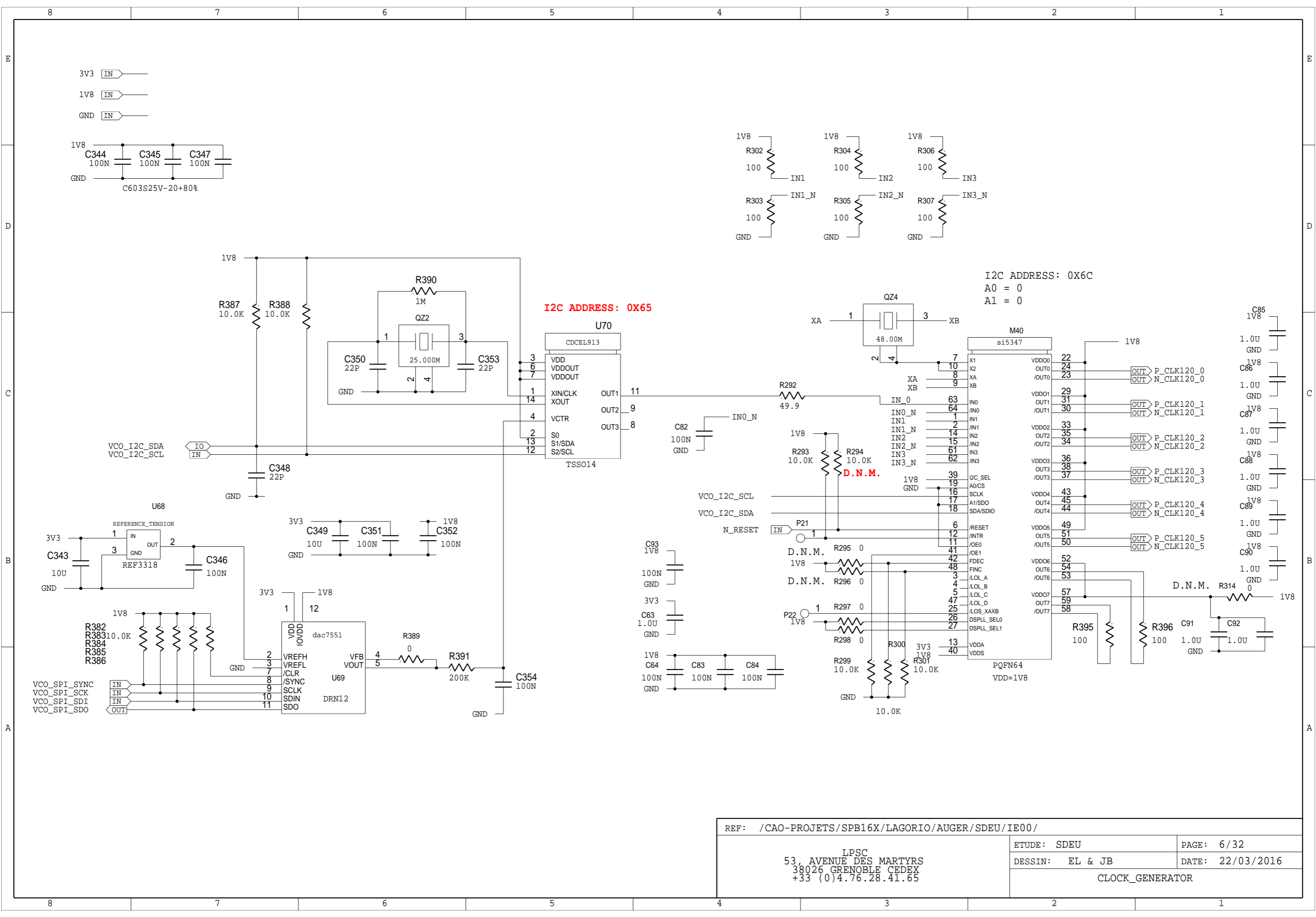
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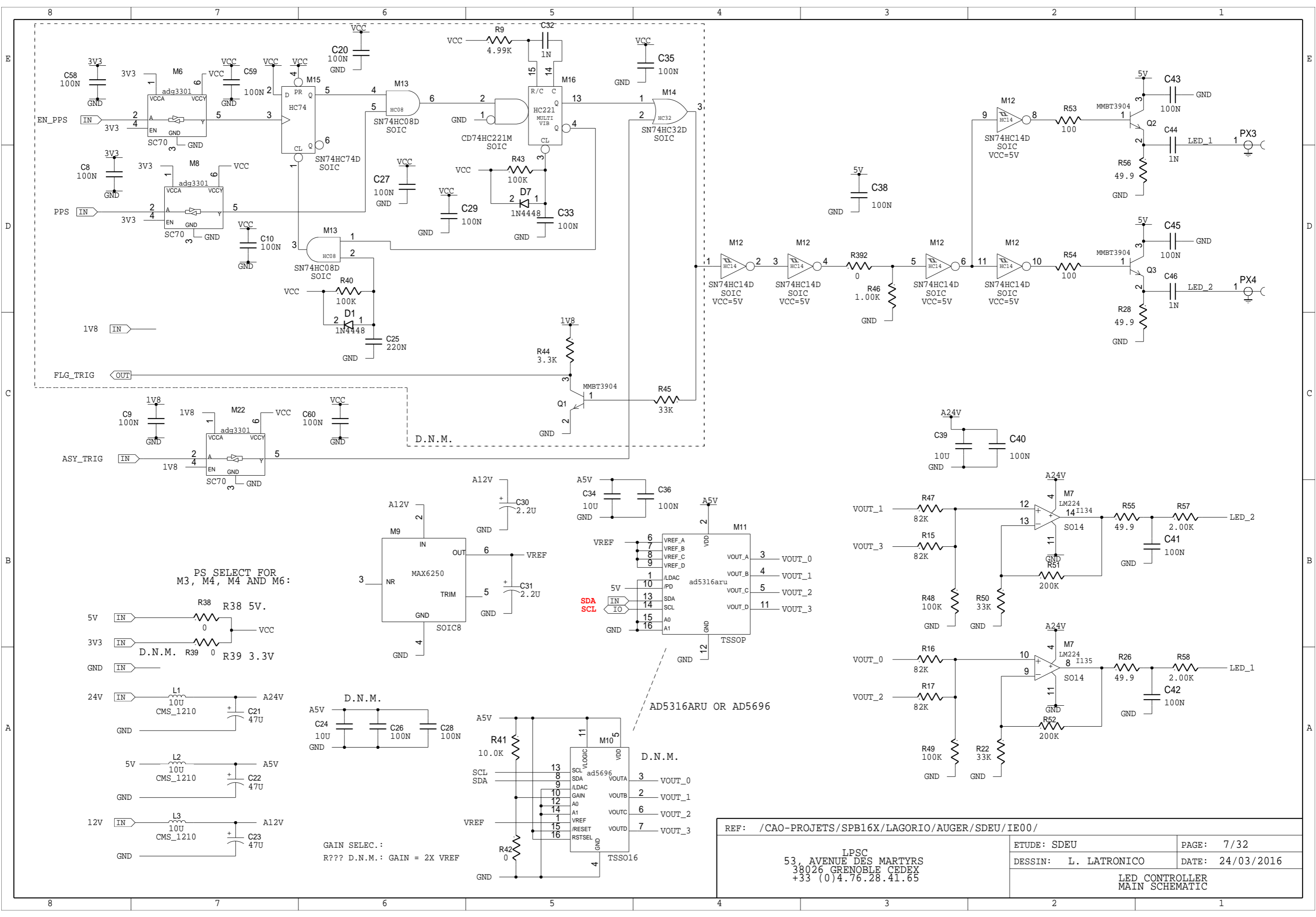
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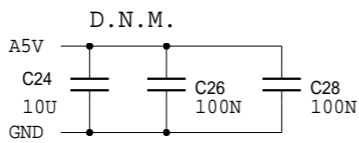
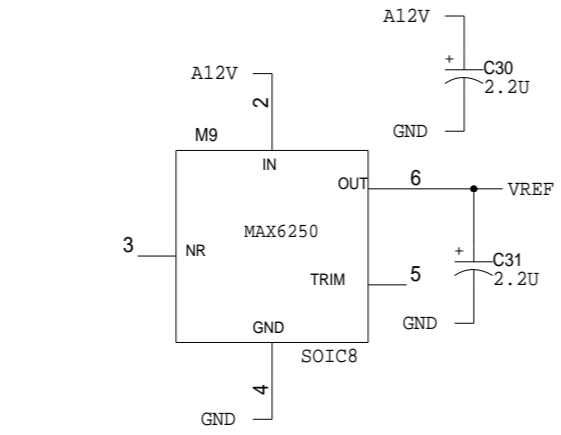
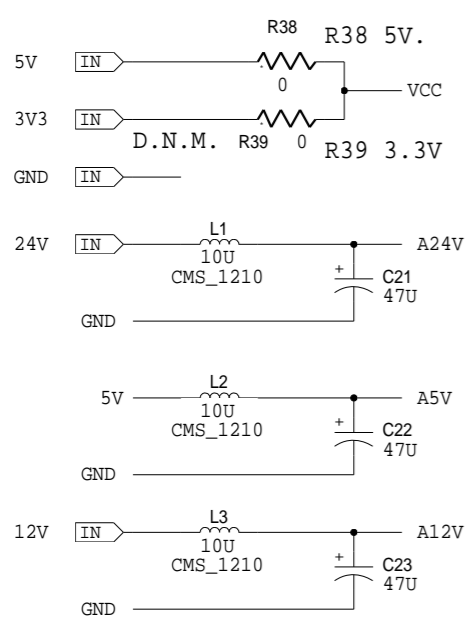
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UART / USB

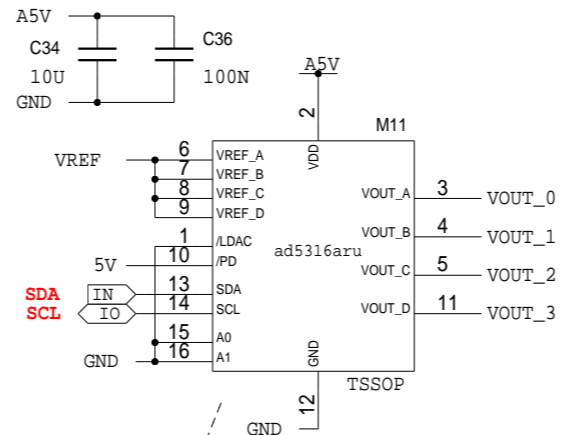




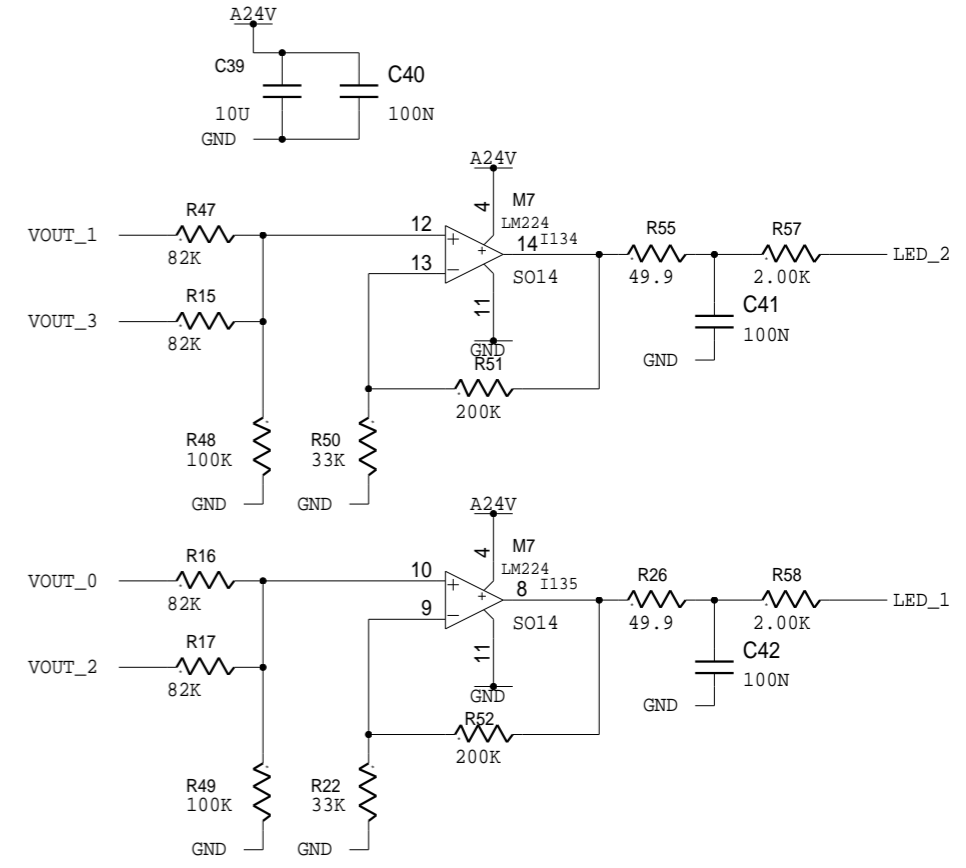
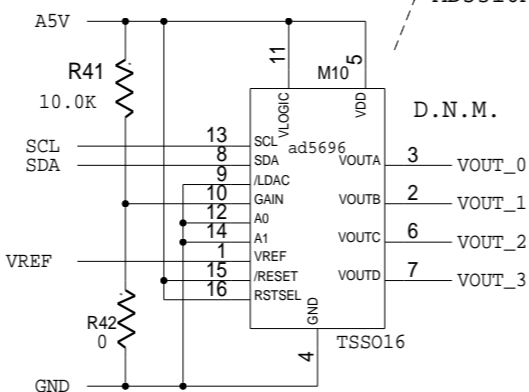
PS SELECT FOR M3, M4, M4 AND M6:



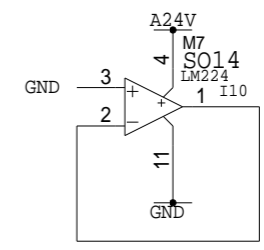
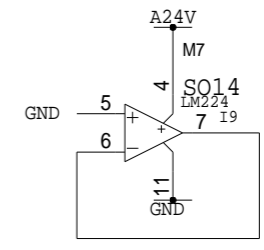
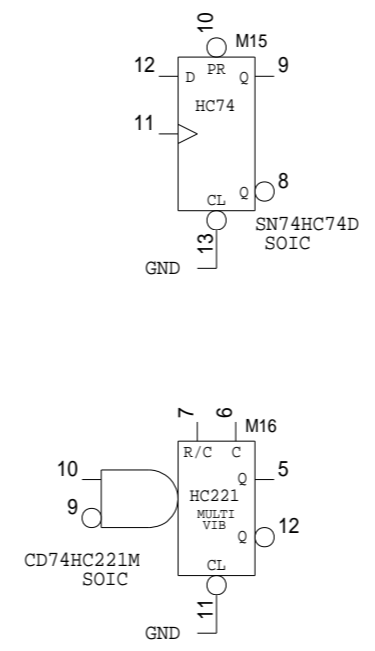
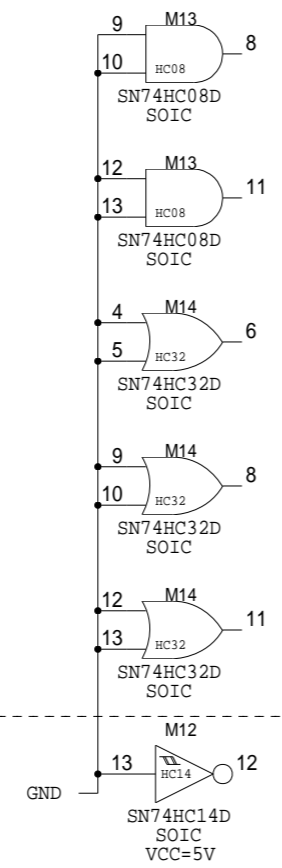
GAIN SELEC.:
R??? D.N.M.: GAIN = 2X VREF



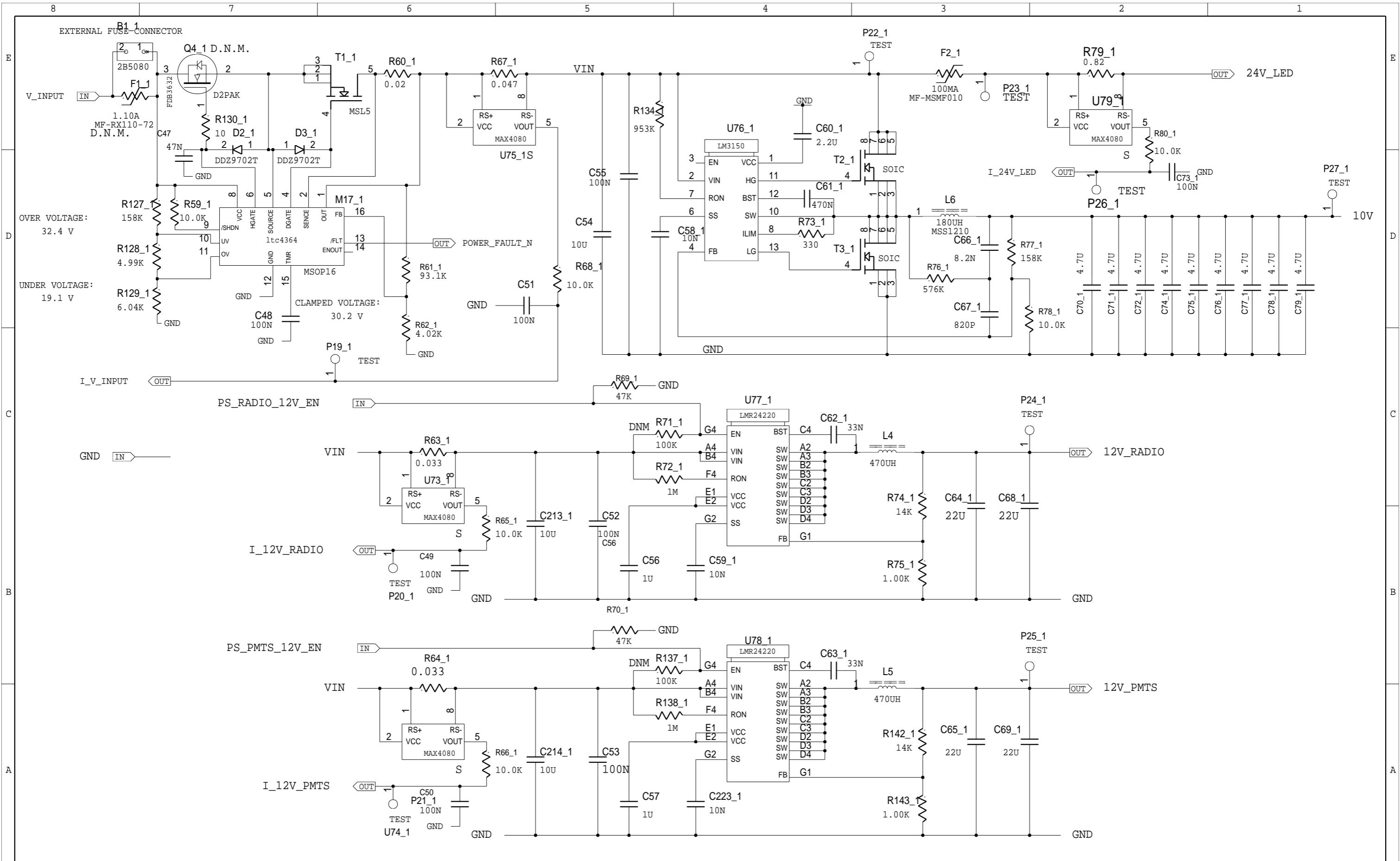
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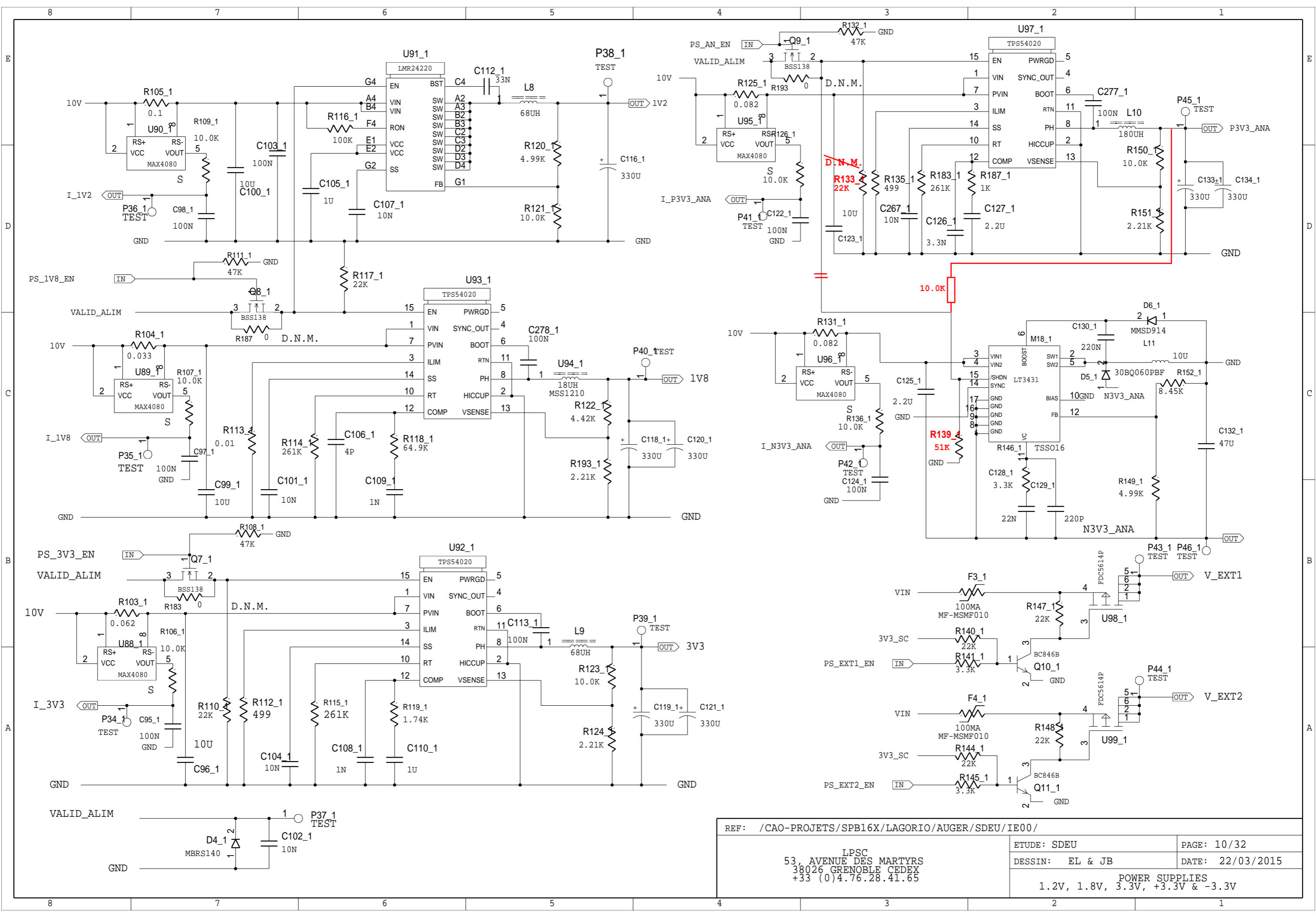


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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65	ETUDE: SDEU
	DESSIN: L. LATRONICO
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DATE: 22/03/2016	
LED CONTROLLER SPARE COMPONENTS	

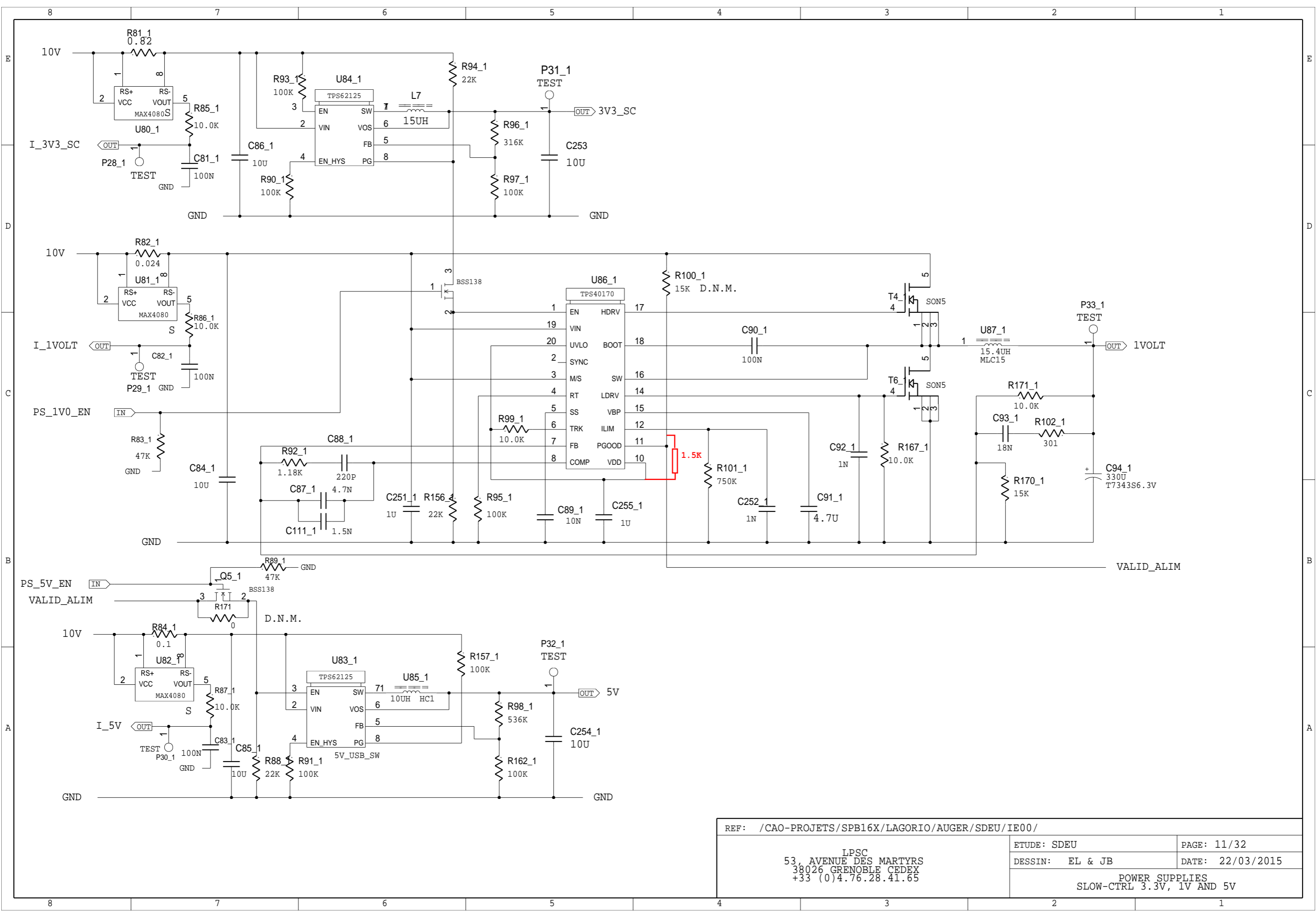




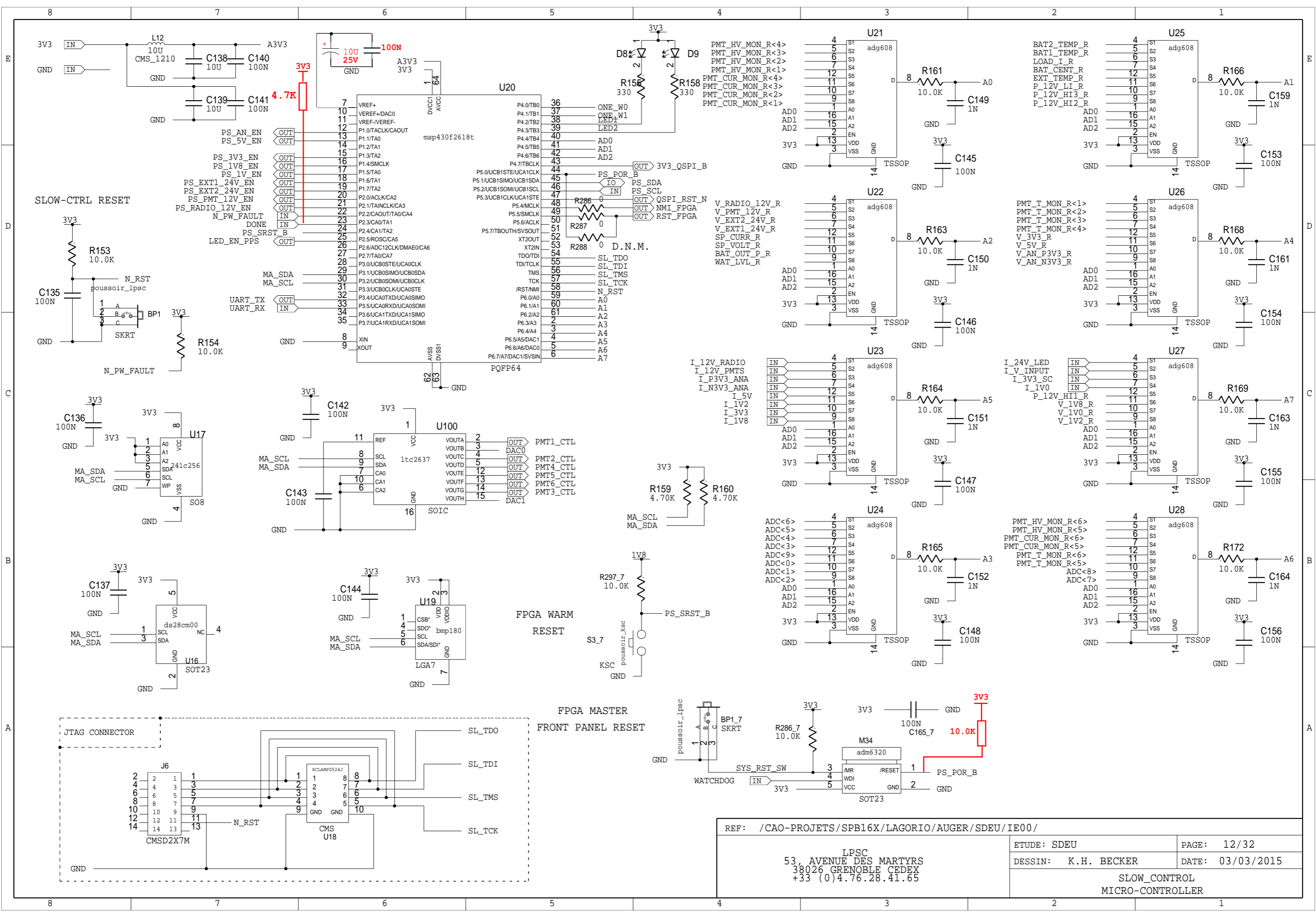
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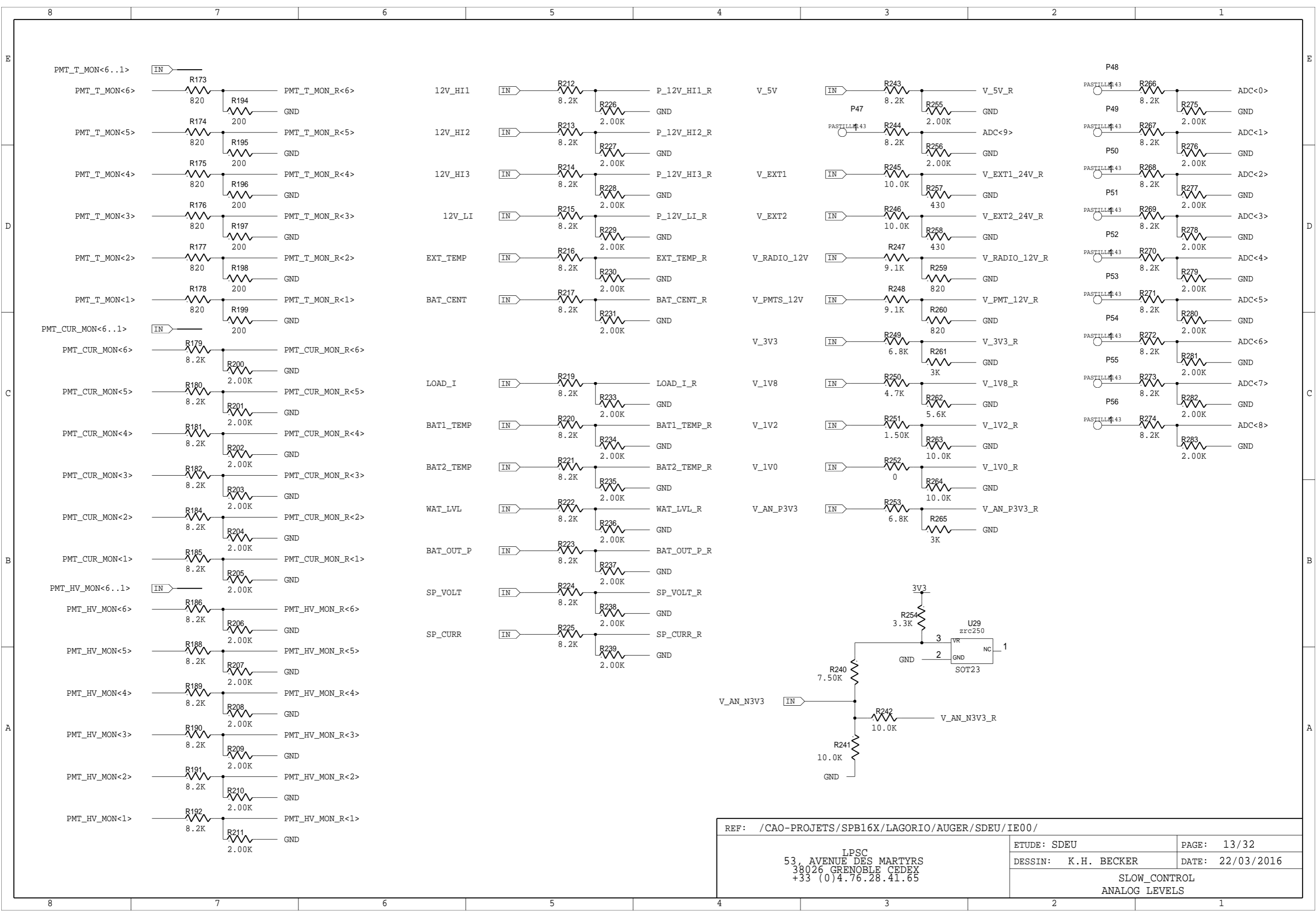
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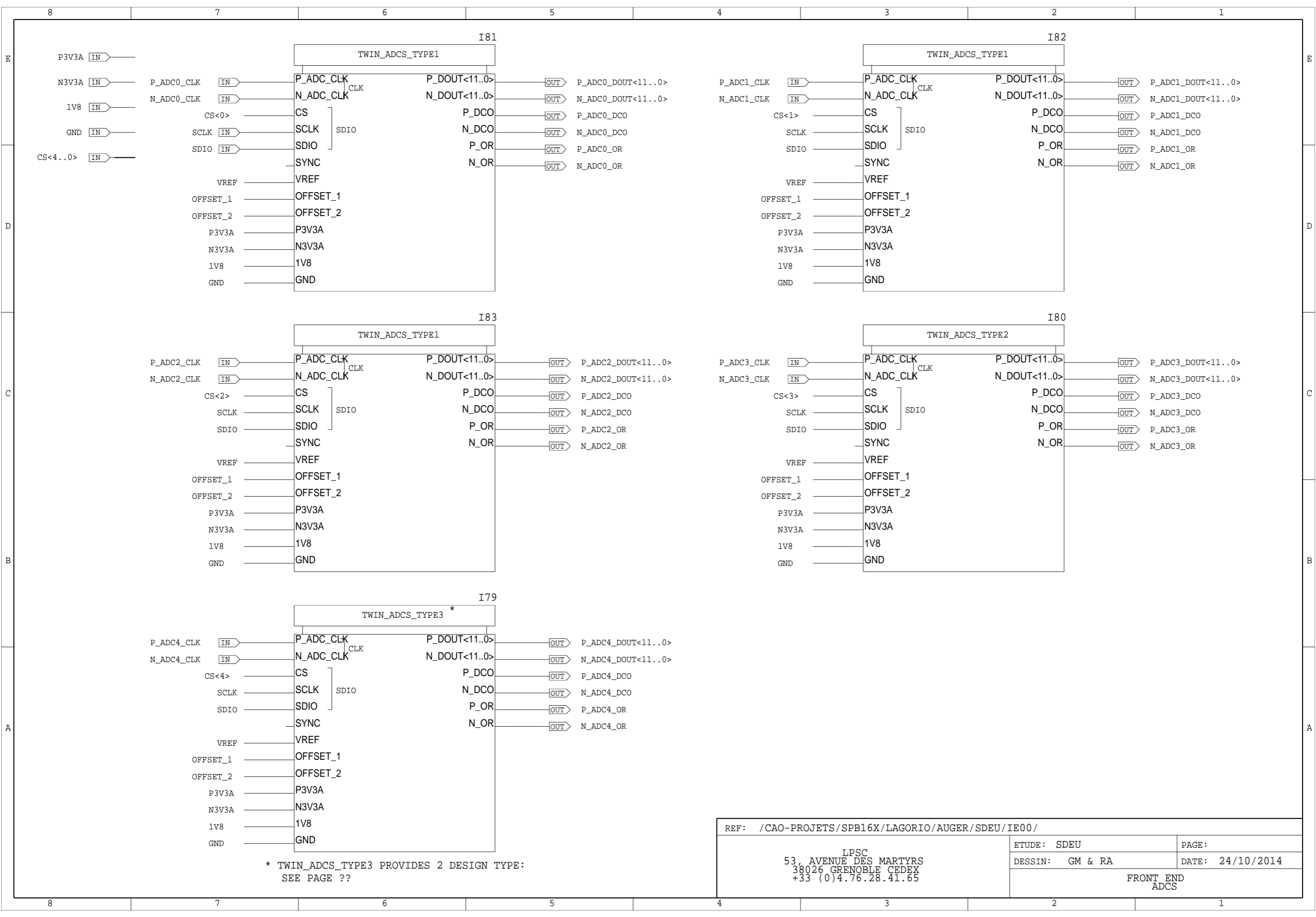
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POWER SUPPLIES	
1.2V, 1.8V, 3.3V, +3.3V & -3.3V	



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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65		ETUDE: SDEU DESSIN: EL & JB PAGE: 11/32 DATE: 22/03/2015
POWER SUPPLIES SLOW-CTRL 3.3V, 1V AND 5V		

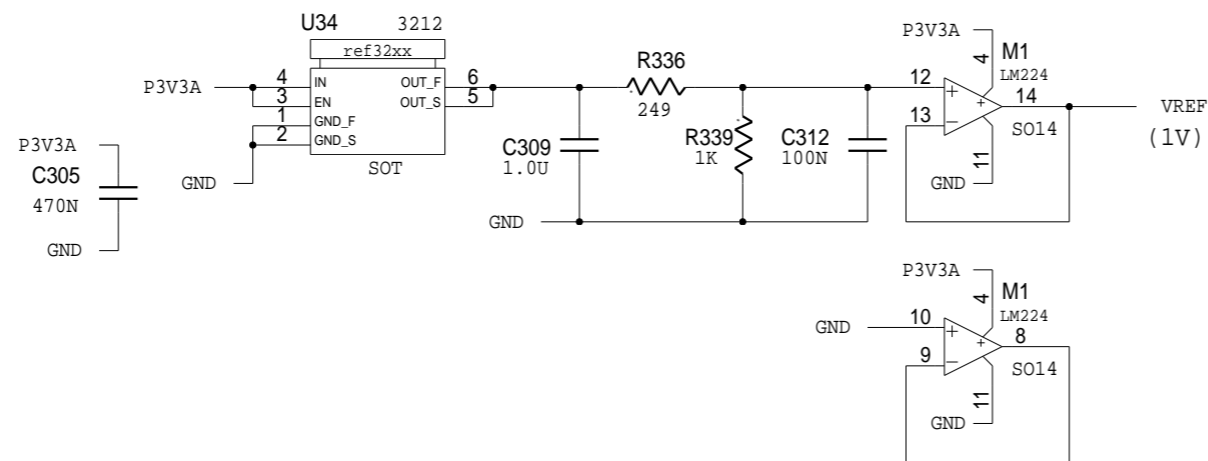
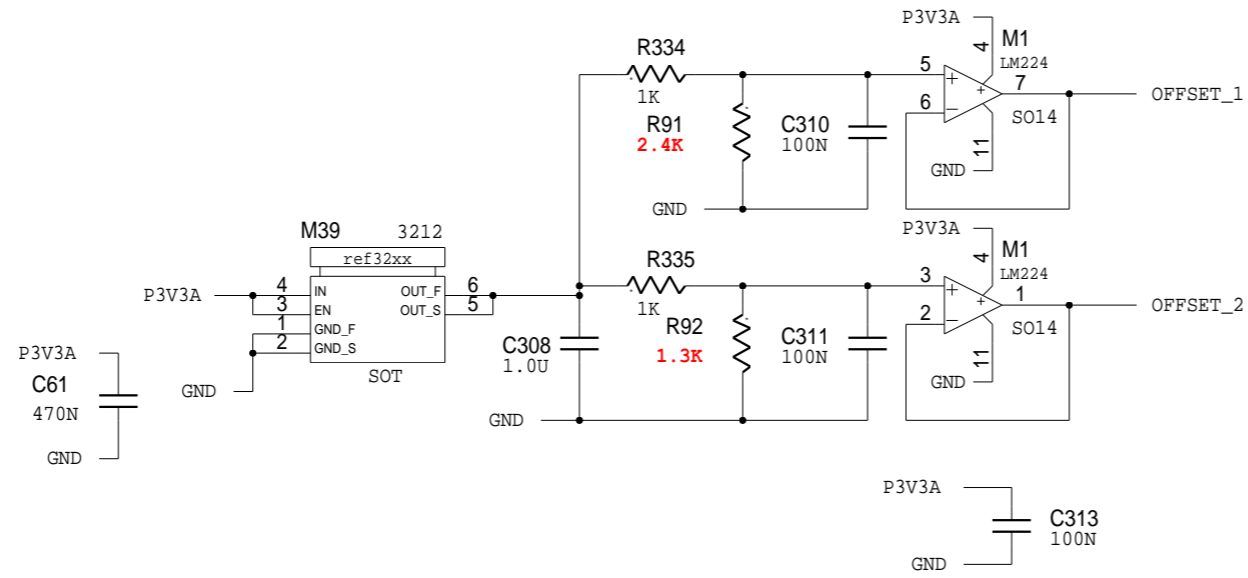






* TWIN_ADCS_TYPE3 PROVIDES 2 DESIGN TYPE:
SEE PAGE ??

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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65		DESSIN: GM & RA	DATE: 24/10/2014
		FRONT END ADCS	



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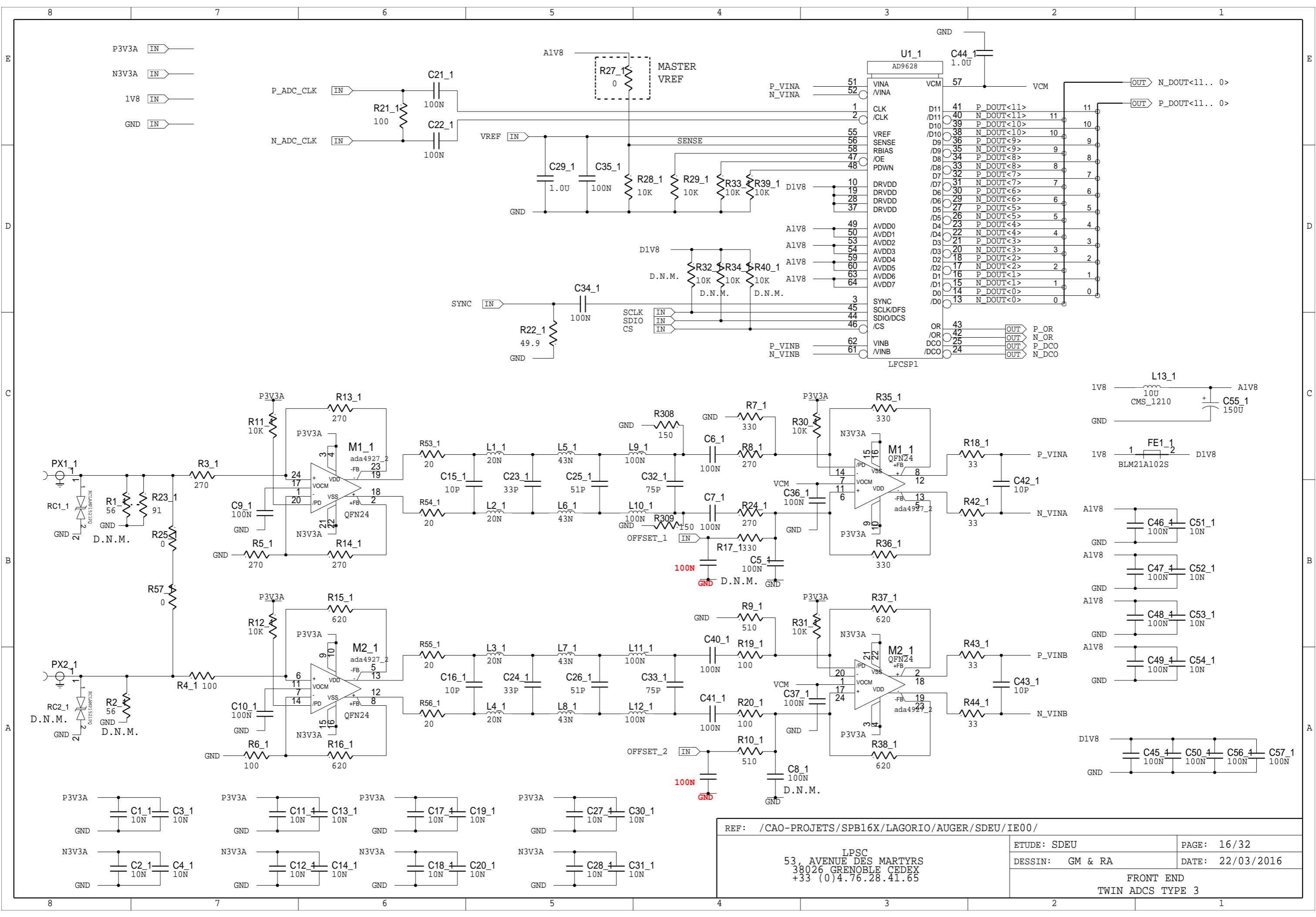
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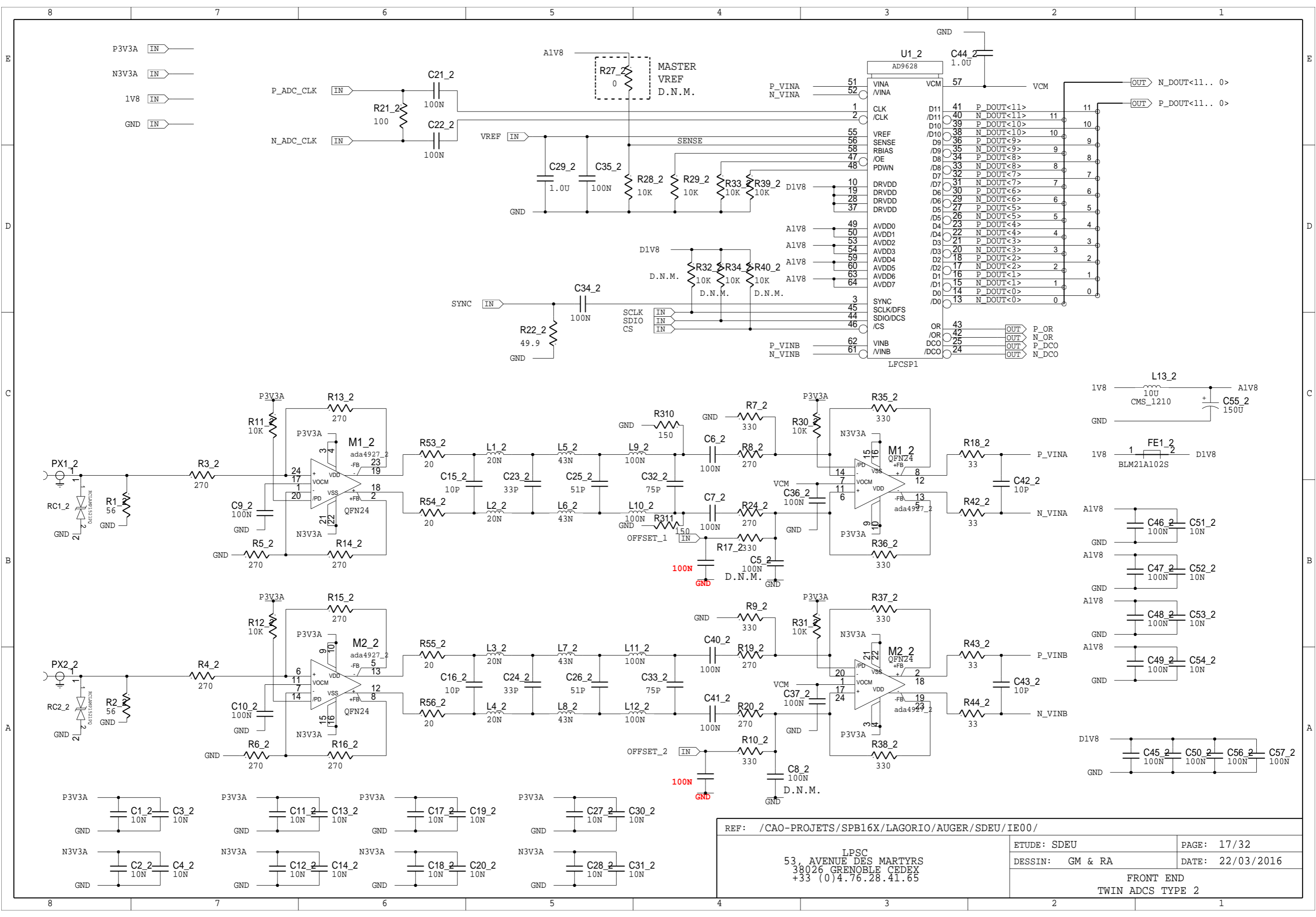
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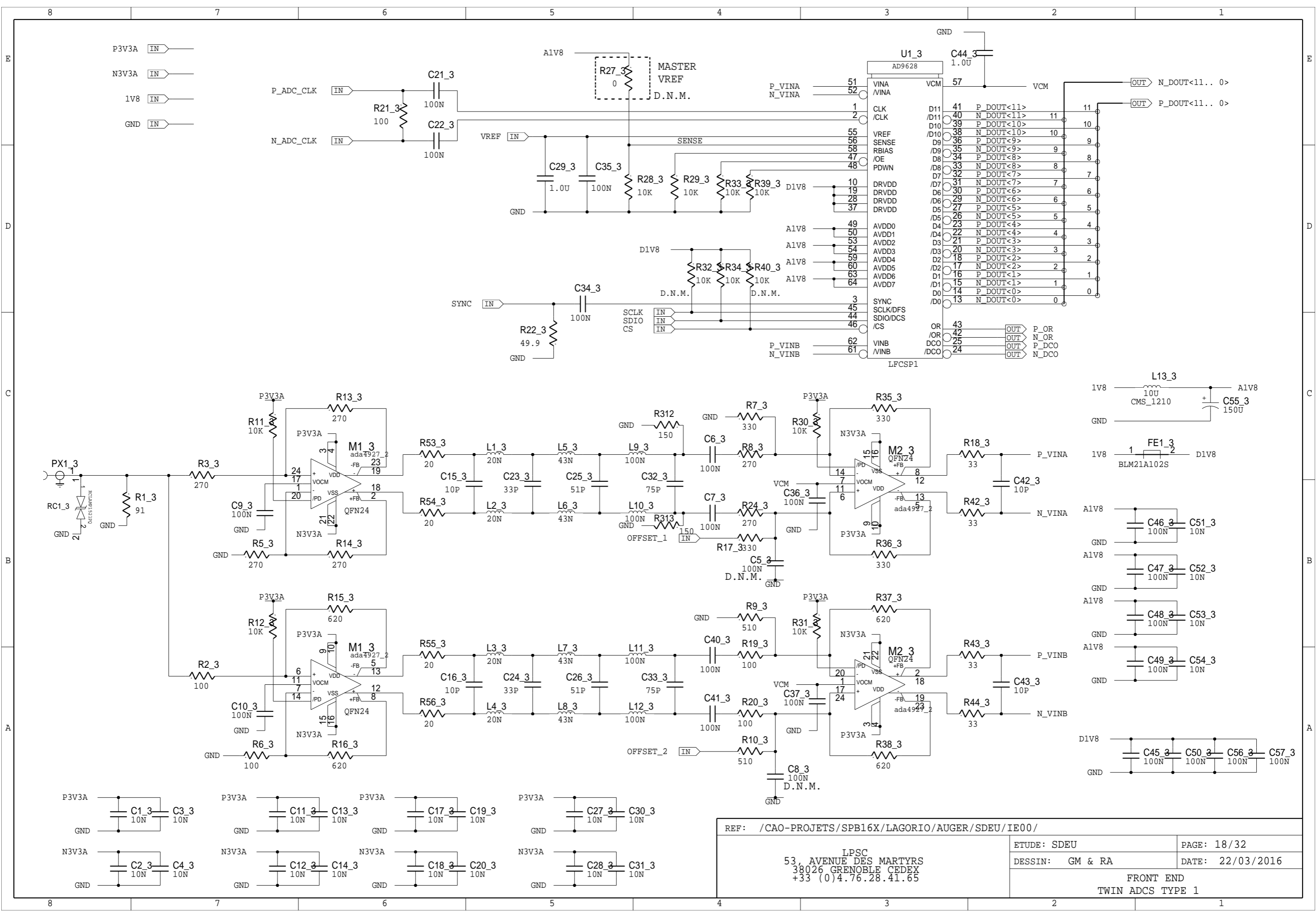
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FRONT END TWIN ADCS TYPE 3	



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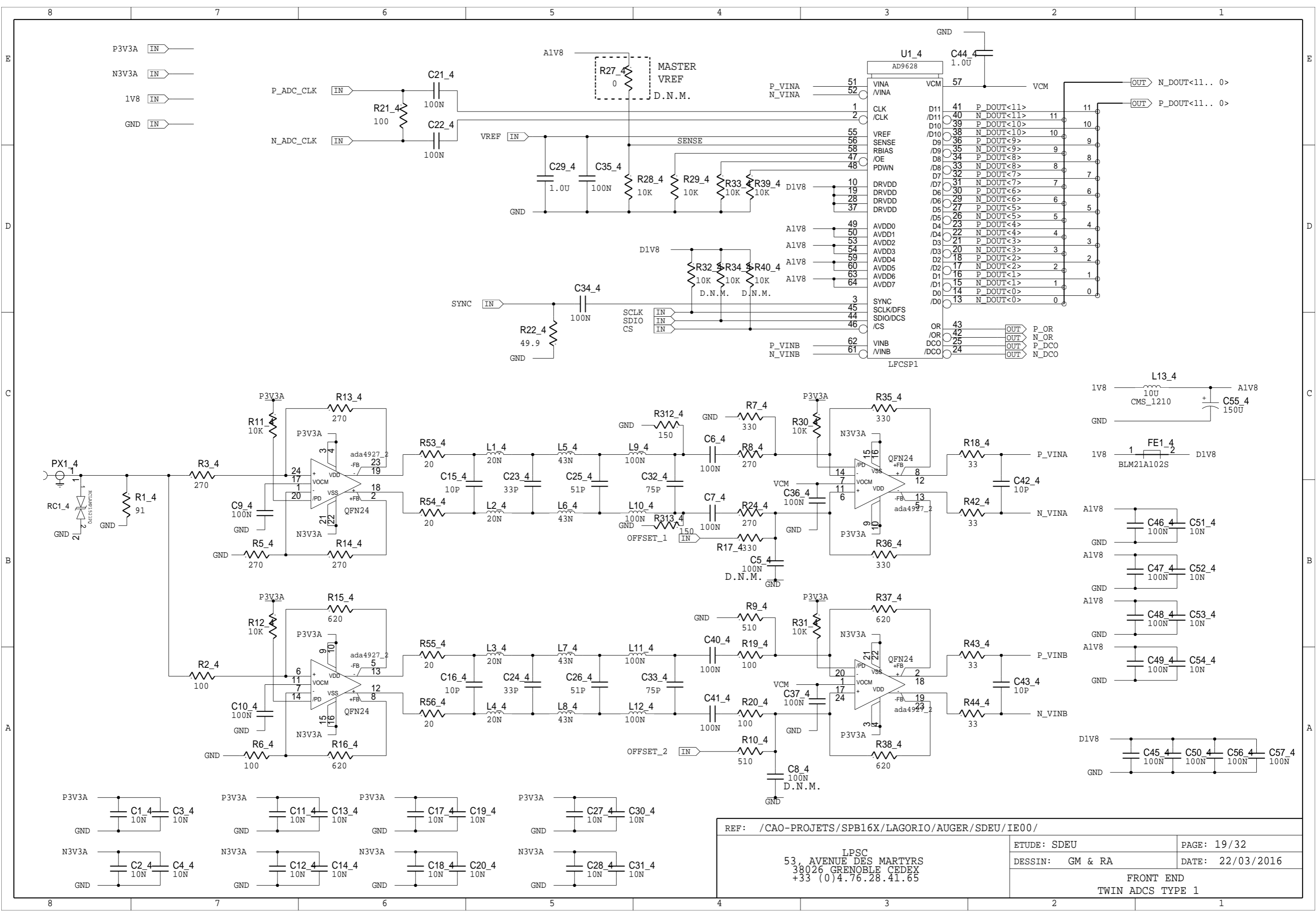
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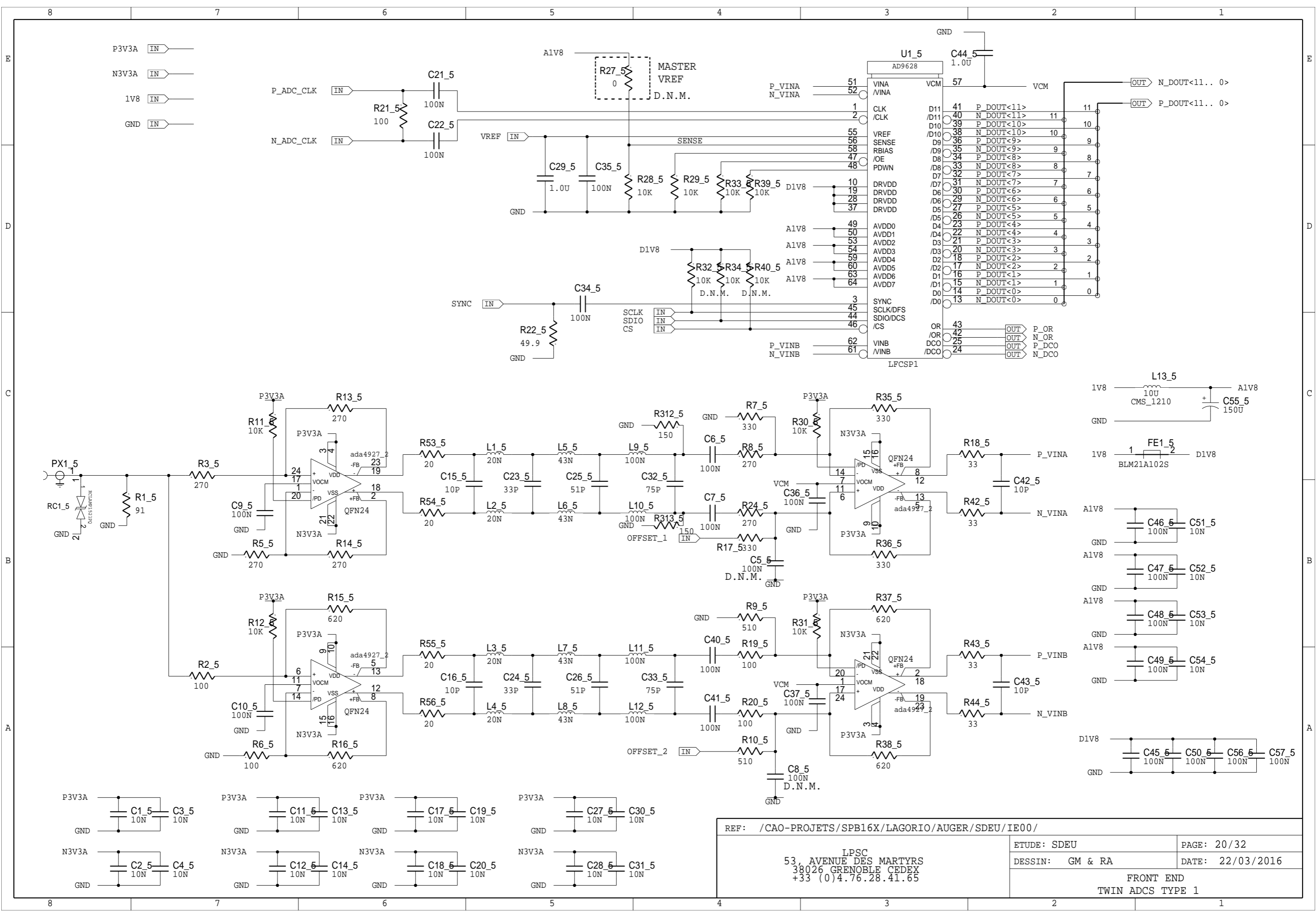
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FRONT END TWIN ADCS TYPE 1	



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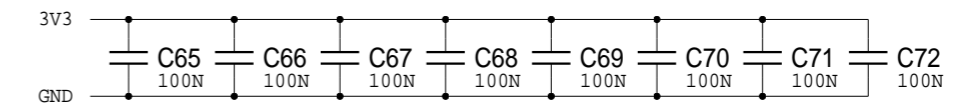
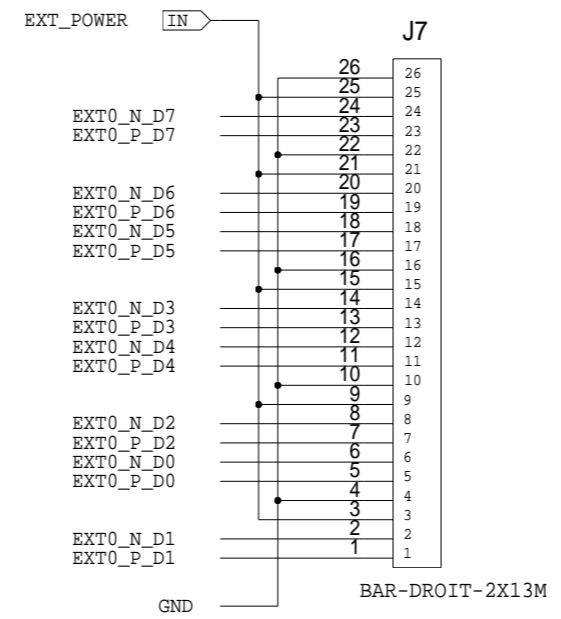
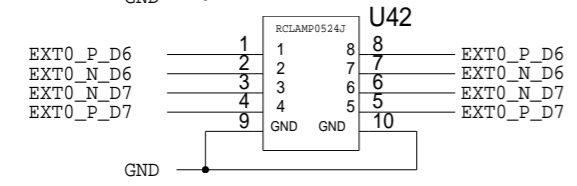
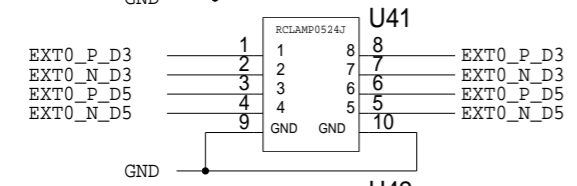
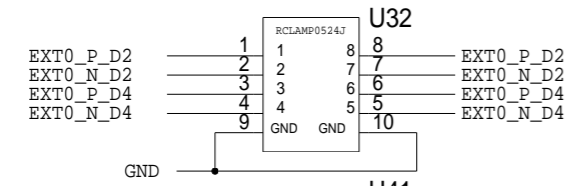
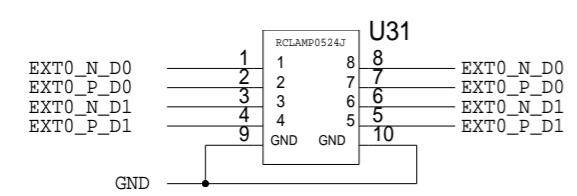
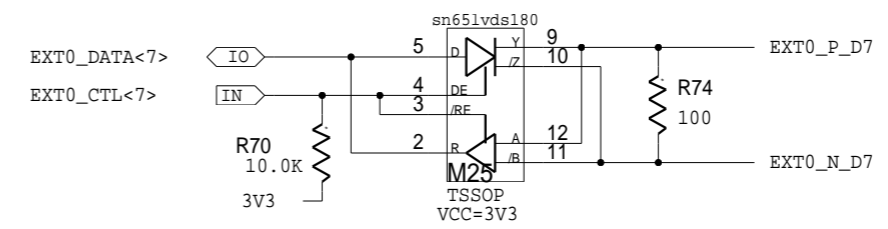
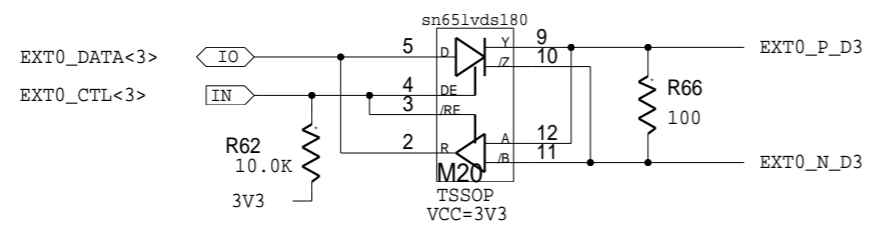
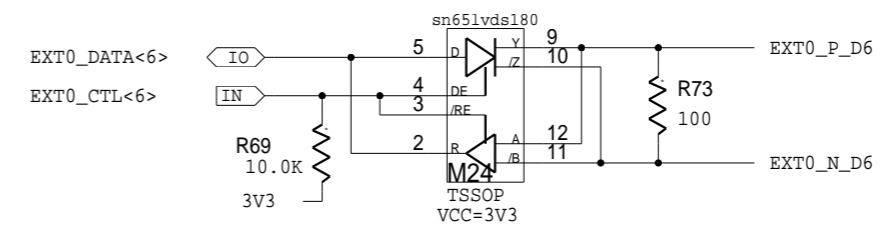
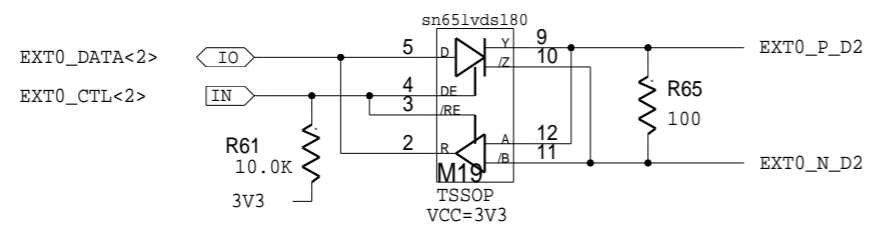
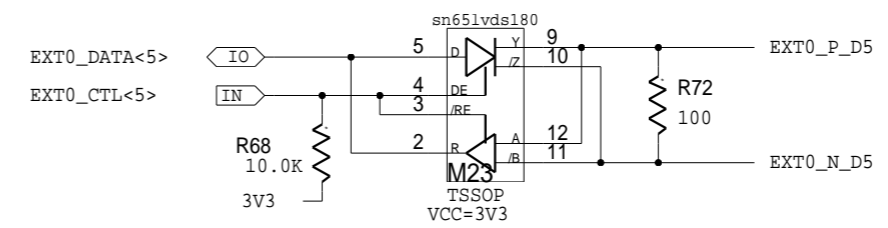
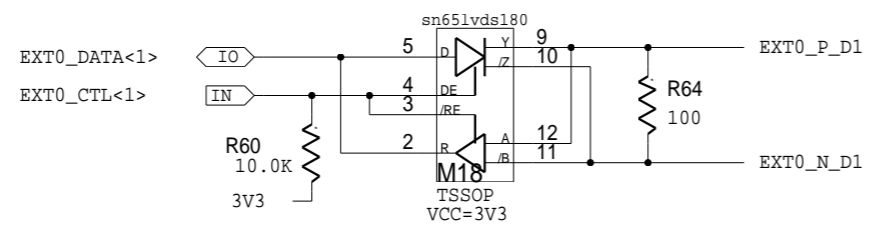
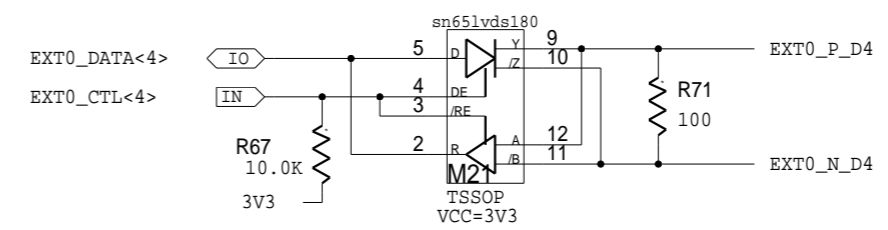
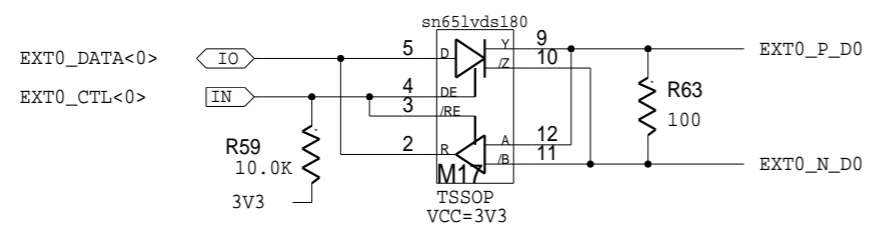
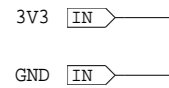
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FRONT END TWIN ADCS TYPE 1	



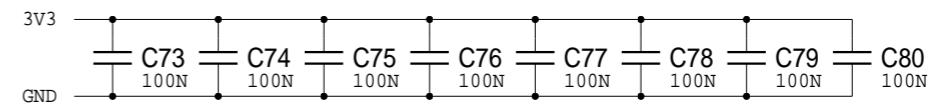
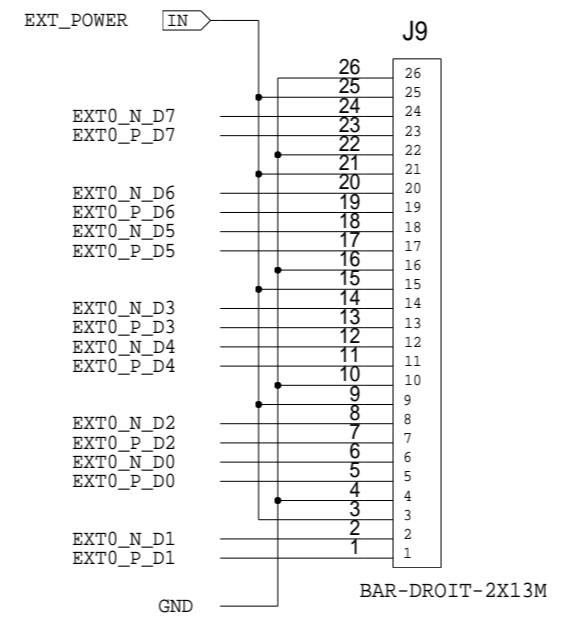
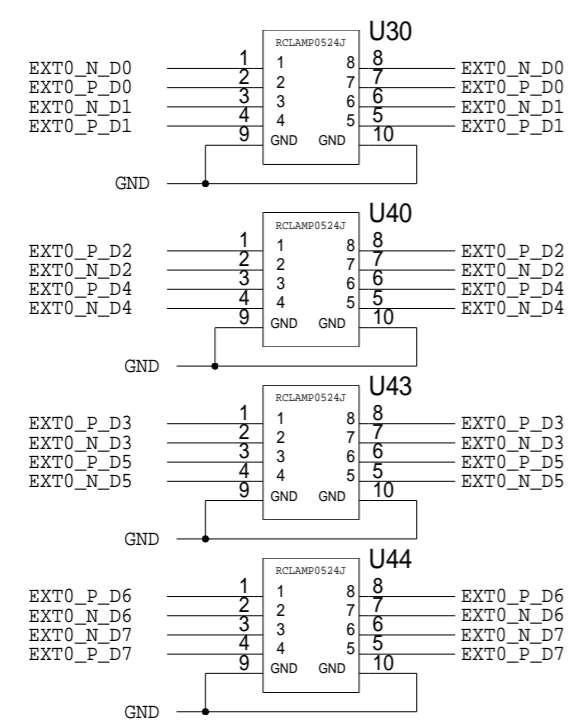
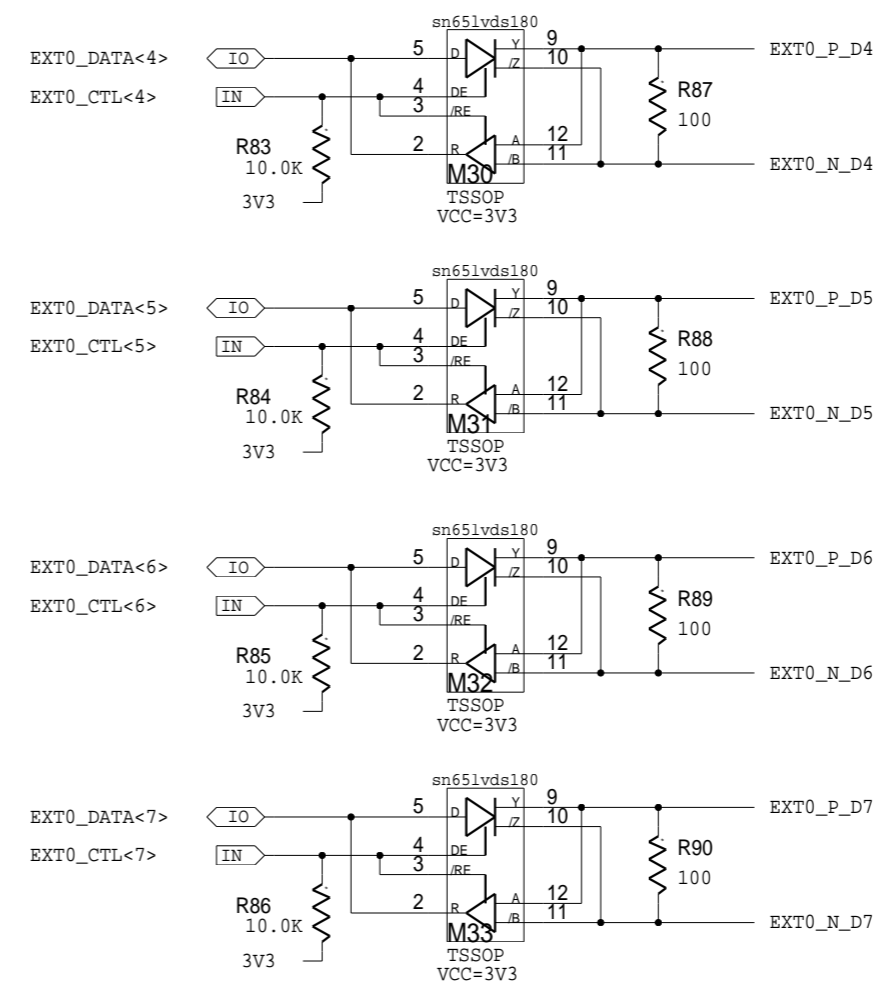
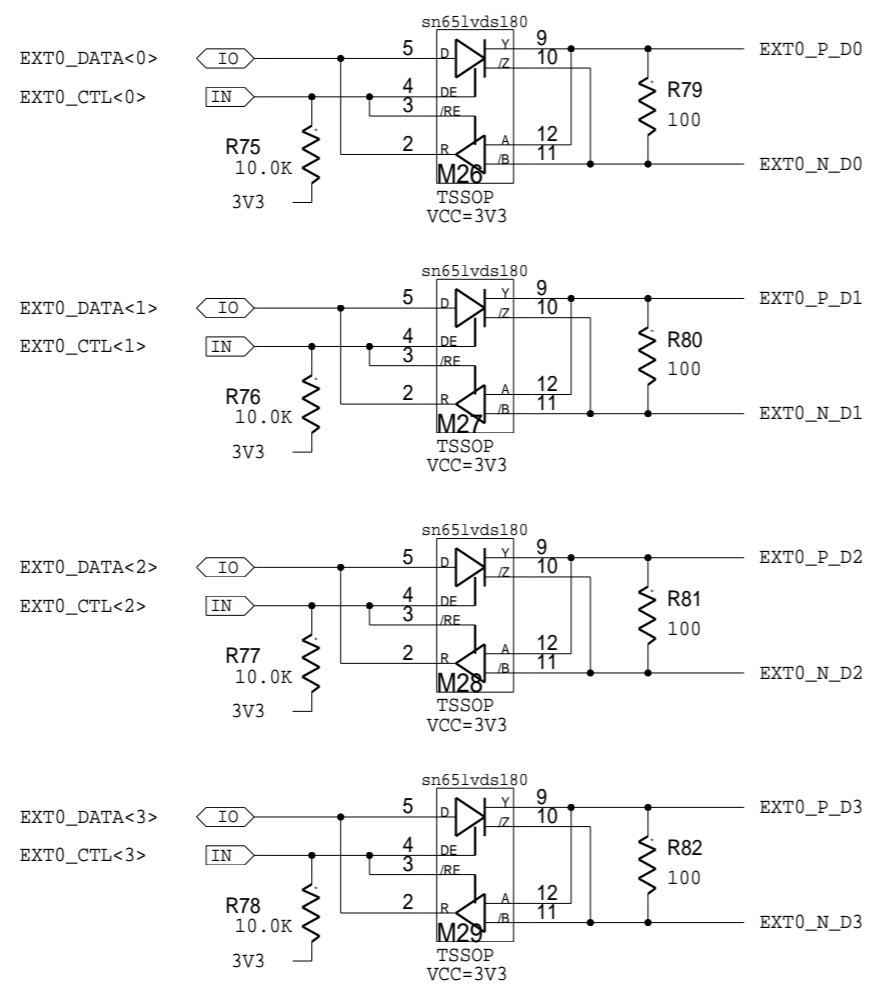
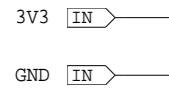
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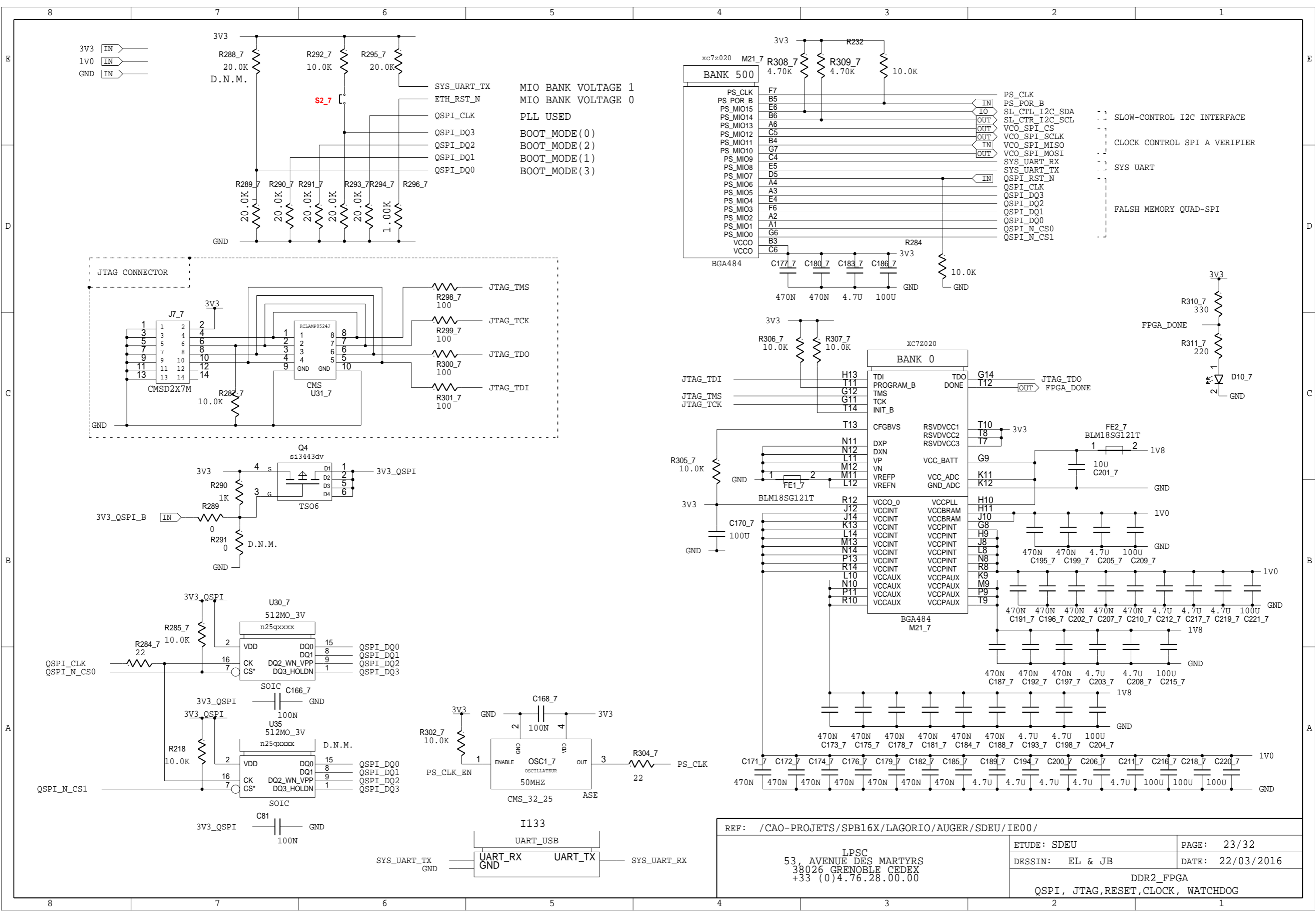
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FRONT END TWIN ADCS TYPE 1	



ALL D.N.M.



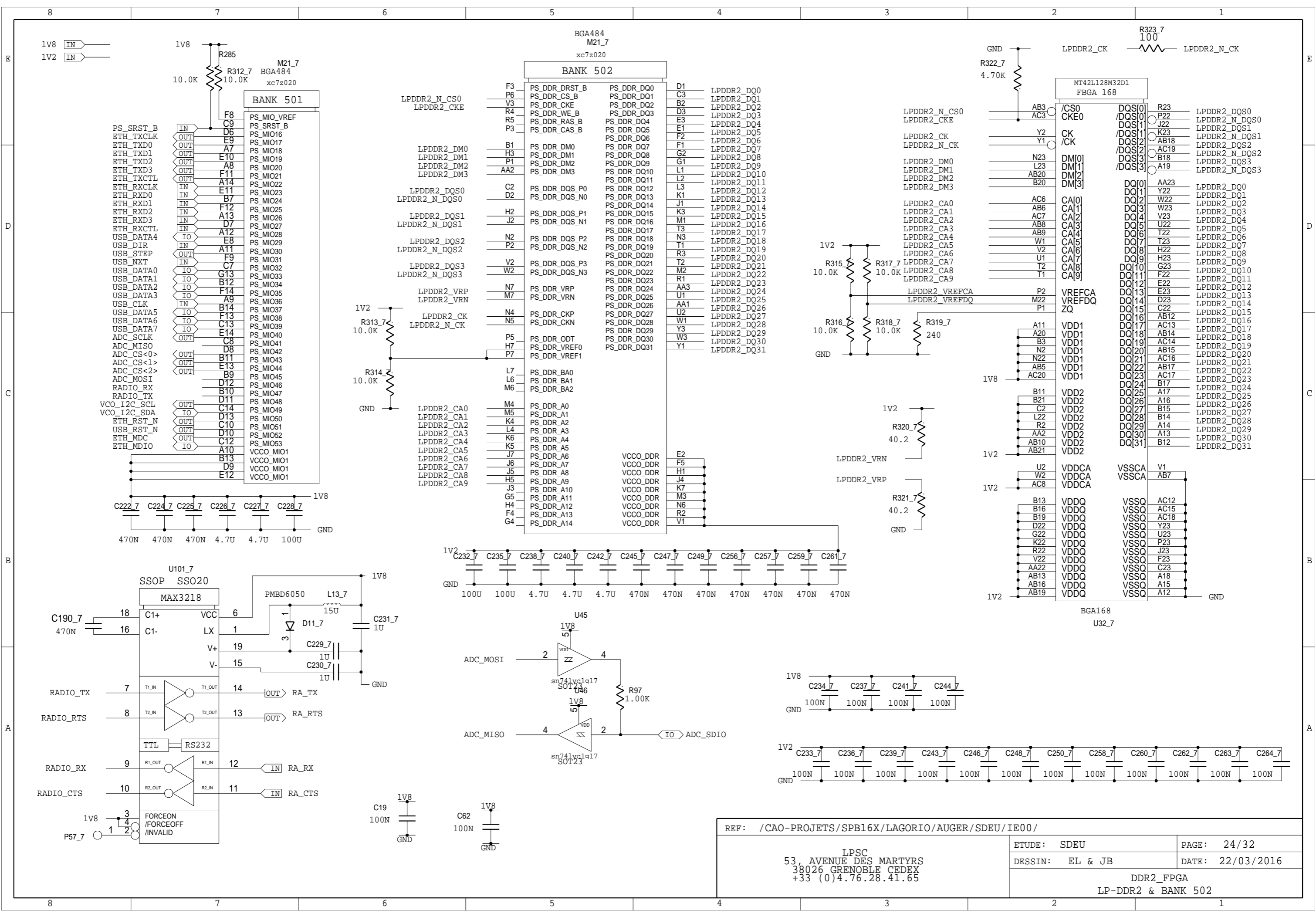
ALL D.N.M.



MIO BANK VOLTAGE 1
MIO BANK VOLTAGE 0
PLL USED
BOOT_MODE (0)
BOOT_MODE (2)
BOOT_MODE (1)
BOOT_MODE (3)

SLOW-CONTROL I2C INTERFACE
CLOCK CONTROL SPI A VERIFIER
SYS UART
FLASH MEMORY QUAD-SPI

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53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.00.00		DESSIN: EL & JB	DATE: 22/03/2016
DDR2_FPGA QSPI, JTAG, RESET, CLOCK, WATCHDOG			

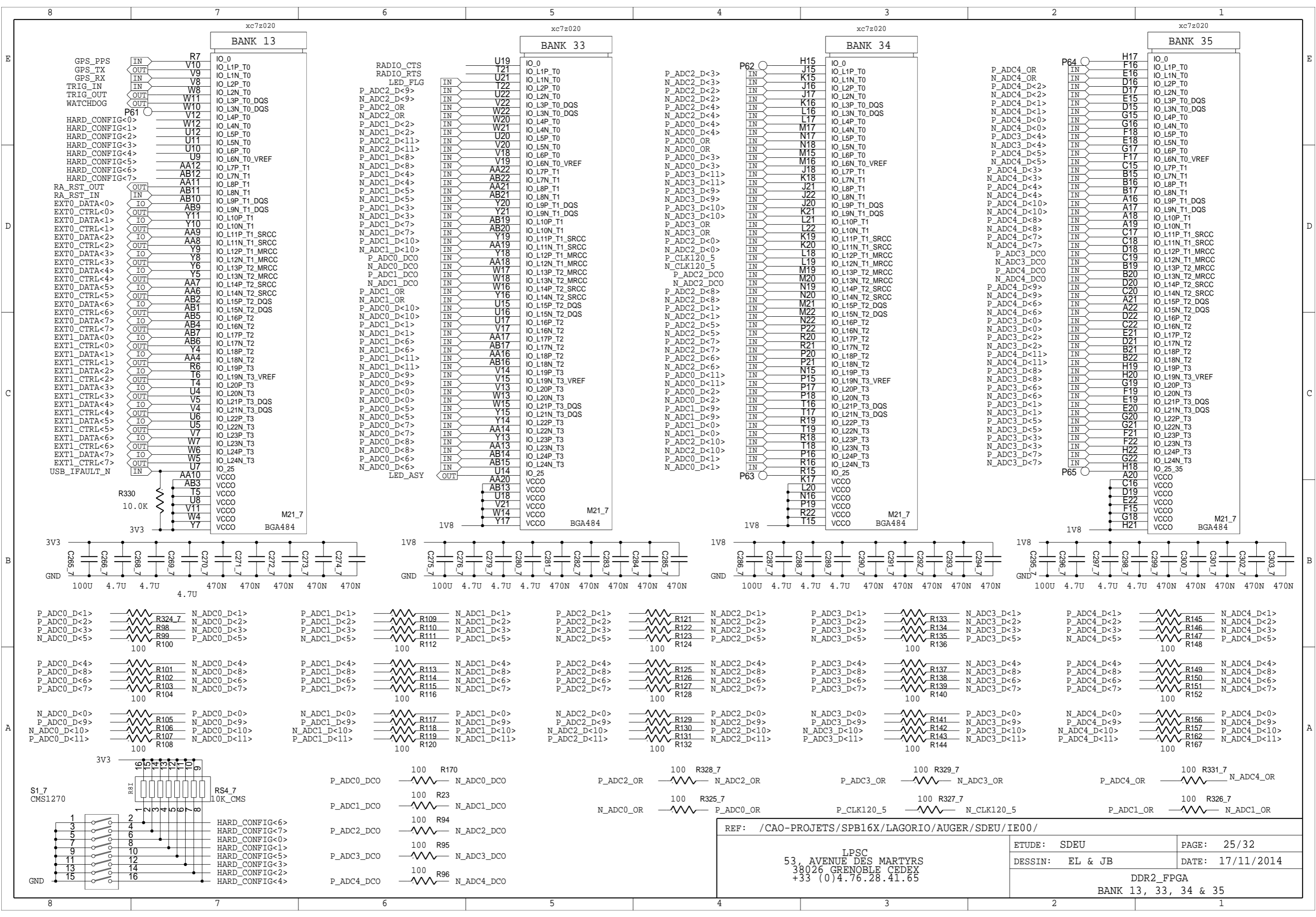


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DDR2_FPGA
LP-DDR2 & BANK 502

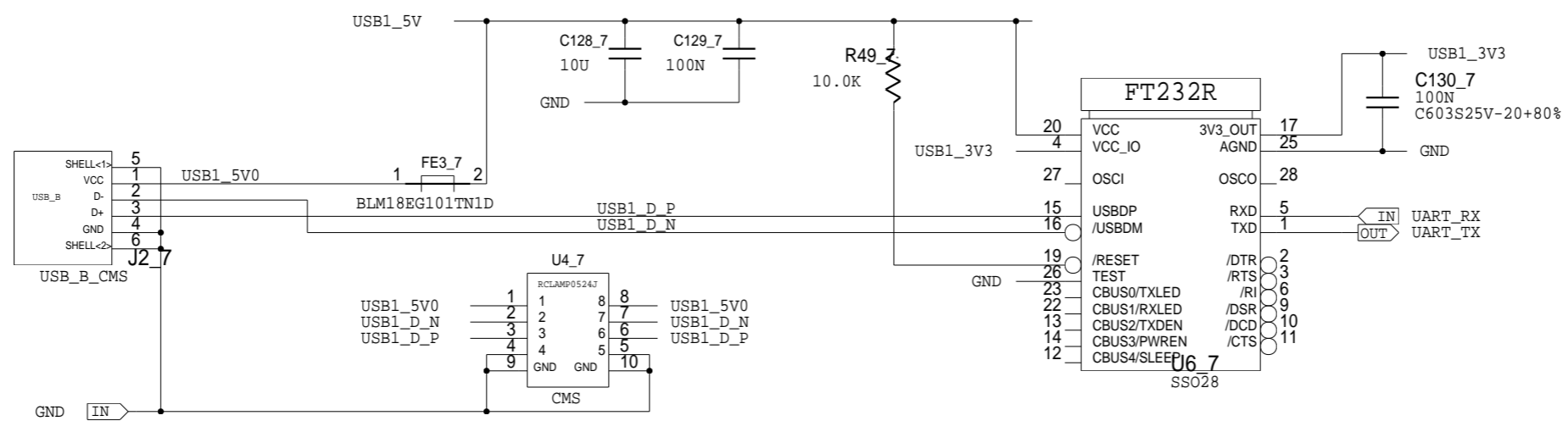


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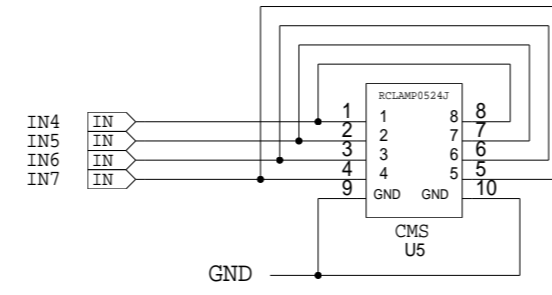
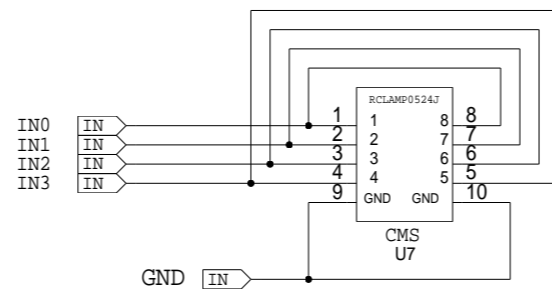
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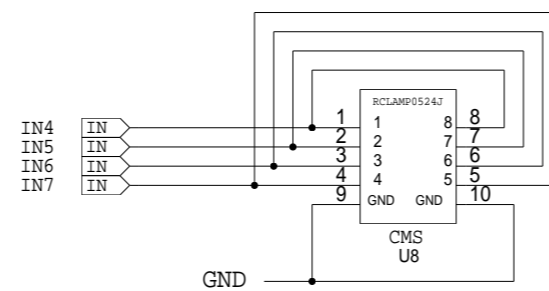
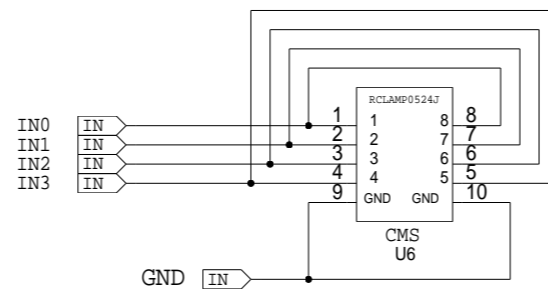
DDR2_FPGA
BANK 13, 33, 34 & 35



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UART / USB		



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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.00.00		DESSIN: EL & JB	DATE: 30/01/2015
		ESD 8 PINS PROTECTION DB15 CONNECTORS	



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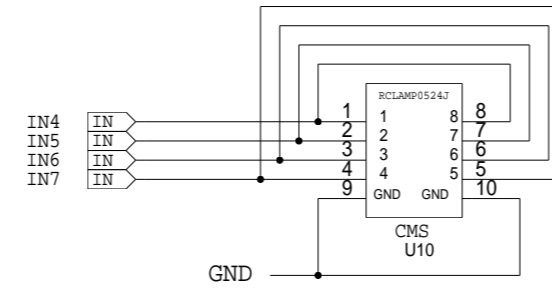
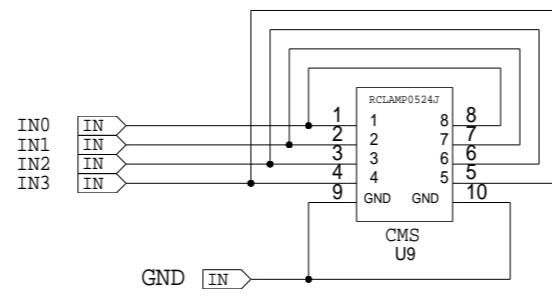
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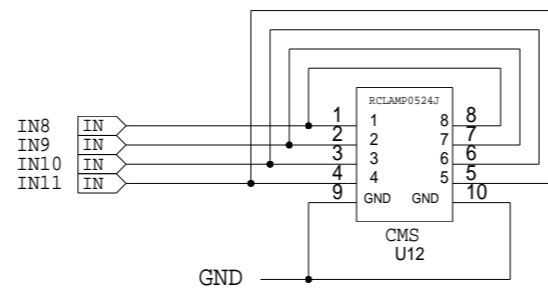
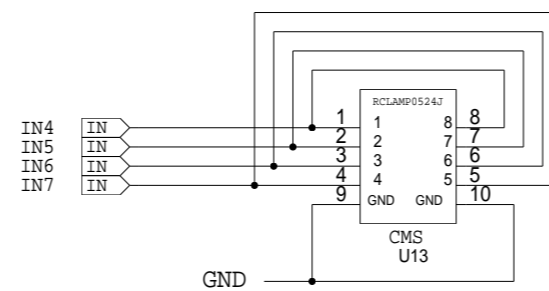
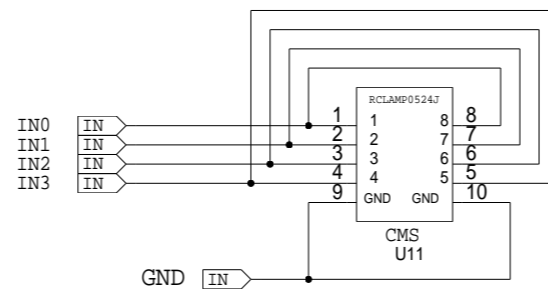
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DATE: 30/01/2015

ESD 8 PINS PROTECTION
DB15 CONNECTORS



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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.00.00	ETUDE: SDEU	PAGE: 29/32
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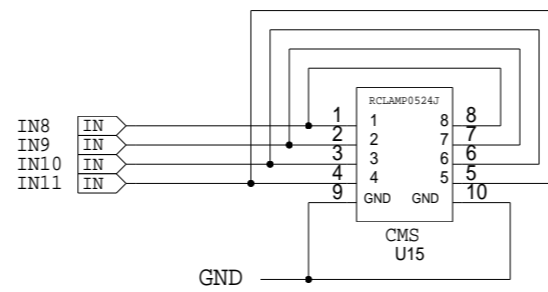
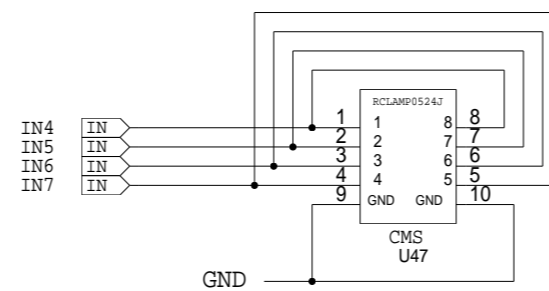
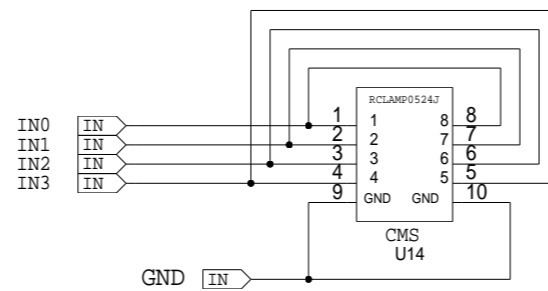
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ESD 12 PINS PROTECTION
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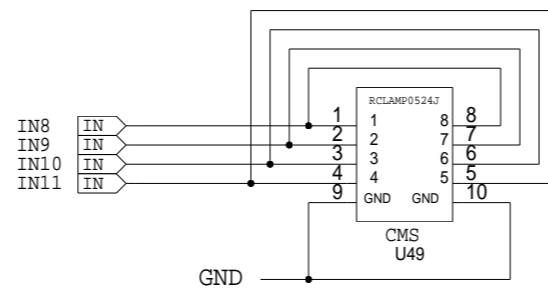
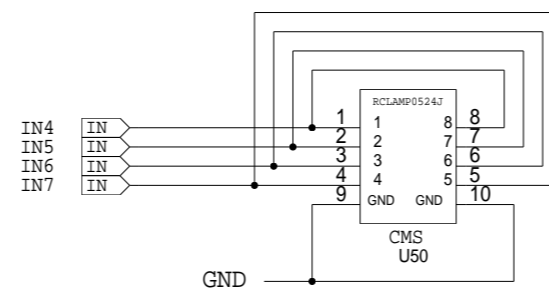
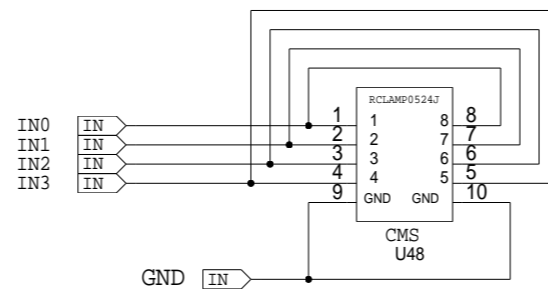
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