Caractéristiques et principaux usages des discriminateurs dans notre communauté

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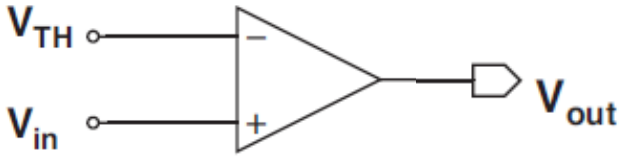


A propos de ce cours …

- A la fin du printemps, Frédéric m'a sollicité pour réaliser ce cours dont le thème principal est les discriminateurs.
- J'en suis un grand utilisateur, et j'en présente souvent l'usage dans des conferences et workshops. Par contre, je n'avais jamais fait une présentation didactique sur ce sujet.

- Dans le peu de temps disponible que j'ai pu trouver, j'ai donc essayé de construire cette synthèse qui couvre à la fois de façon simple les aspects théoriques et la réalisation des circuits, mais aussi leurs principaux usages dans les développements réalisés à l'intérieur de notre communauté.

- Les slides sur la théorie des discriminateurs sont largement inspirés du chapitre 9 du livre **d'Angelo Rivetti** dont je vous recommande la lecture : "**Front-End Electronics for Radiation Sensors**"
- Ceux concernant la mesure de temps sont inspirés d'une présentation d'**Eric Delagnes** sur le sujet.

- Pour des raisons pratiques, la plupart des slides sont rédigés en anglais. J'espère que cela ne sera pas un problème pour vous …

Introduction

- In the field of particle or radiation detectors, current and voltage **comparators** are often called **discriminators** in order to emphasize their function, which consists of **separating the signal from the background**.

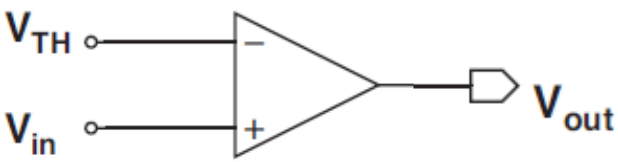
- Synchronous comparators are systematically employed in the implementation of Analog to Digital Converters (ADC) and in many other analog systems.

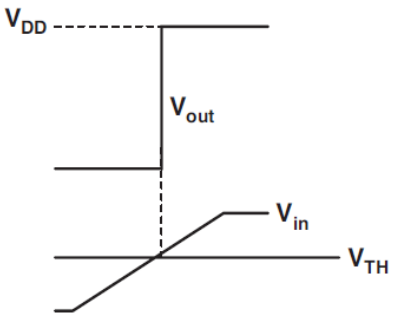
- But in applications involving particle sensors, **the arrival time of the event is mostly unknown**.
  - Even in the applications in which particles arrive at predictable times, such as in colliding beam experiments or beam tests, the simultaneous triggering of many digital cells can become an issue, especially in chips housing many channels.

- For these reasons, **asynchronous topologies** are the most used
  - **Those are the ones we will focus on …**

Definition

- The discriminator task is to **generate a logic signal** that distinguishes if the input signal level sits **below or above a given threshold**.
- This information will then be passed to digital logics that will take the appropriate decisions on the usual following signal processing steps : trigger decision and/or data transmission.
- The discriminator output has therefore two possible states, one corresponding to the logic level "zero" (0 V in a single supply system) and the other to the logic level "one" (in general equal to the *VDD* supply)

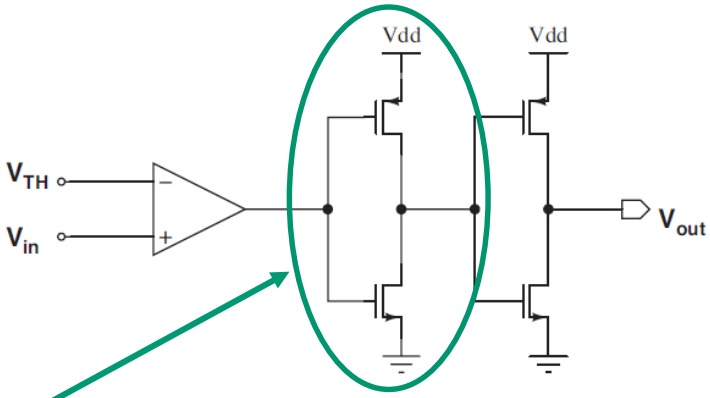




- It switches as rapidly as possible between the two states when the input threshold is crossed.
  - If the comparator was ideal, this transition would be instantaneous
  - But in the real life, there are **gain and speed limitations**, which have to be taken into account for system design

Constitution

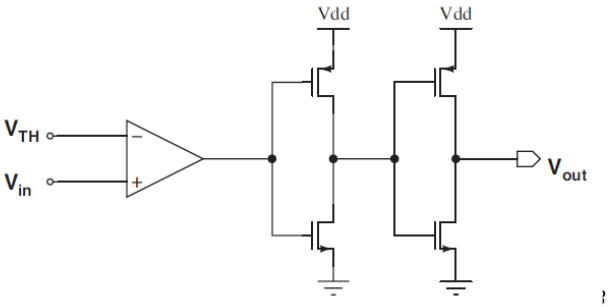
- Actually, a discriminator basically consists of a **high gain differential voltage amplifier followed by a chain of CMOS digital inverters**.
- These inverter gates serve two purposes:
  - they ensure that the comparator delivers to the following digital stage **a well defined logic signal**.
  - they provide **adequate buffering** power to drive the output load.
- The number of inverters and their respective size have to be optimized according to the capacitive load of the net (which can be internal or external to the circuit)



- Concerning the inverter, it is sufficient to recall here that its output flips when the **input crosses a built-in threshold** which depends on the relative sizing of the NMOS and PMOS transistor and it is **typically set to *VDD*/2**.

Working principle

- **The inverter** interprets safely as a "zero" any DC level < 0.2 *VDD* and as a "one" any level > 0.8 *VDD*.
- When ***Vin* ≪ *Vth*** the output of the differential stage is in proximity of the negative rail and produces a voltage *Vol* that must typically be **smaller than 0.2 • *VDD***.
- When ***Vin* ≫ *Vth***, the differential stage output is close to *VDD* and must deliver an output voltage *Voh* typically **greater than 0.8 • *VDD***.
- Delivering **already clear logic signals** to the first inverter is mandatory because otherwise the gate might flip on noise, introducing spurious events.
- Furthermore, both the PMOS and the NMOS transistor could be simultaneously in conduction, increasing significantly the static power consumption of the circuit.
- The difference $Voh - Vol = \mathrm{D}Vo,hl$ divided by the DC gain $Av0$ of the differential amplifier yields the **minimum voltage difference D *Vin*** that must be applied across the comparator inputs to determine a flip in the output voltage, thus defining the resolution.



Characteristics

- However, additional factors limit the circuit ability to detect small signals in practical applications.

- A comparator should in fact provide an answer **within acceptable times**, hence also speed considerations play a critical role in its design.

- The speed performance of a discriminator are constrained by the **small signal bandwidth** of the circuit and by its slew-rate.

- To study the former, we assume that the response of the differential amplifier can be modeled with a **single pole transfer function:**

$$A_v(s) = \frac{A_{v0}}{(1 + s\tau_p)}$$

where τ_p is the time constant associated to the pole.

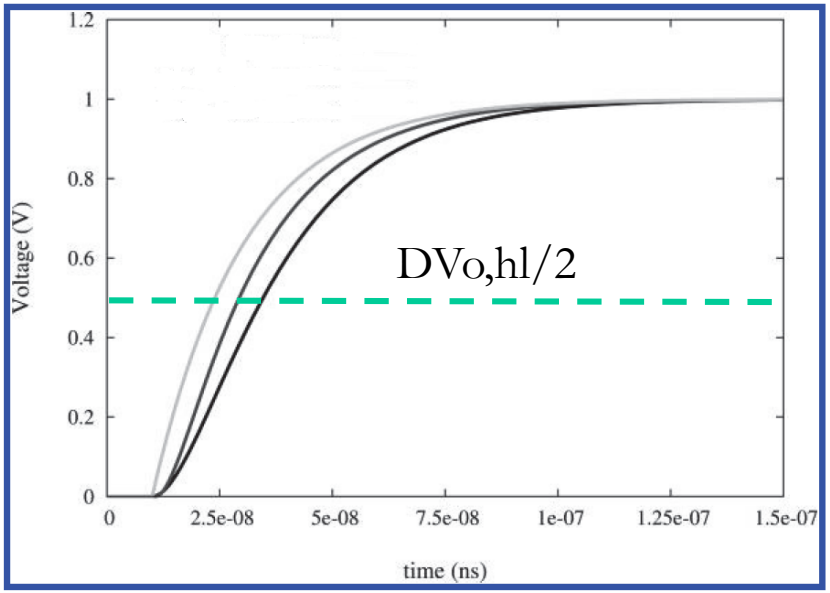
Rise time

- If a rectangular voltage step of amplitude Vin is applied to the input, the output voltage is given by:

$$V_{out} = V_{in} A_{v0} \left(1 - e^{-\frac{t}{\tau_p}}\right)$$

- Due to the bandwidth limitation, the output does not flip instantaneously, but it will change following the equation above. In order to make the inverter flip, the output must swing by at least DVo,hl/2, crossing the inverter threshold point.

- Example of responses to a voltage step with different values of τ_p.
- Delay for crossing DVo,hl/2 depends on τ_p.



Minimum signal at input

- Let's call **α** the ratio between the real signal and the minimum difference that the circuit is able to detect, and $\mathbf{t_d}$ the time the output of the comparator needs to move by DVo,hl/2 due to its limited bandwidth
- A rapid calculation gives:

$$t_d = \tau_p \ln\left(\frac{2\alpha}{2\alpha - 1}\right)$$

- For instance, if we take a 2.5V signal at the output of an amplifier with a gain of 1000, what will be the value of **α** ?

We know that in order to be sure to have a valid output level of the comparator, the input of the first output inverter has to sit out of 0.2 to 0.8 VDD. The corresponding range is thus 0.6 VDD, which corresponds to 1.5V in our case.

With a gain of 1000, this corresponds to 1.5mV of difference between the two inputs of the discriminator

thus **α = 1.5 mV**

Remark : the smaller the technology, the smaller the value of **α** since the ratio between V_T (MOS) and VDD gets smaller …

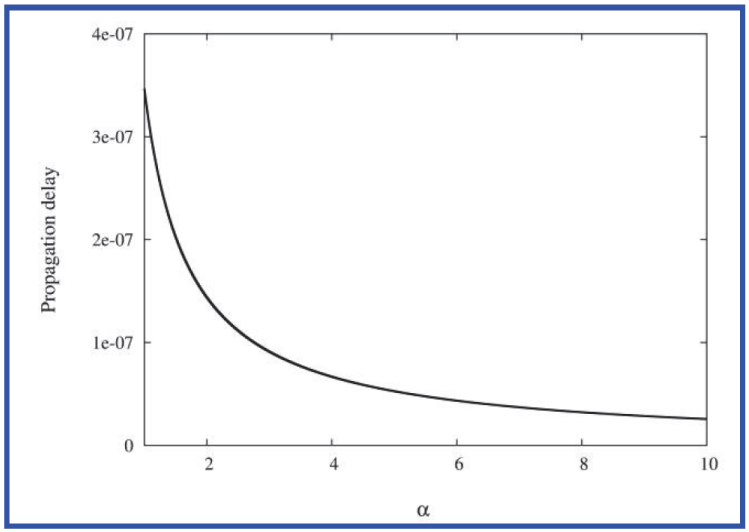
Delay vs signal amplitude

- Let's go back to our equation:

$$t_d = \tau_p \ln\left(\frac{2\alpha}{2\alpha - 1}\right)$$

- The propagation delay is thus of 0.693 τ_p for a signal equal to the minimum one (α = 1) and reduces to 10% of τ_p for α = 5.

- The figure to the right shows the propagation delay of a single pole discriminator as a function of the ratio α between the actual and the minimum signal. A time constant τ_p = 500 ns is assumed here for the pole.
- **Slew rate** then becomes the limitation for high values of α.



Effect of the input noise

- One input of the comparator is usually connected to the front-end electronics output and the other is held fixed at a threshold voltage close to the front-end baseline.
- If the threshold is too close to the baseline, due to the noise, the baseline level is crossed many times, resulting in a series of pulses at the discriminator output.
- To avoid this effect, **the comparator must be unbalanced**, putting the threshold at a value sufficiently distant from the baseline.

- The formula giving the hit rates at the comparator output is the following:

$$f_n = \frac{1}{2\pi\tau} e^{-\frac{V_{TH}^2}{2V_n^2}}$$

- For a zero threshold, it reaches its maximum of $1/2\pi\tau$ which gives for instance a noise hit rate of 8 MHz for a system with τ = 20 ns.
- If the threshold is now raised to a value four times bigger than the noise, the noise hit rate goes down to 2670 Hz!

Dealing with the input noise

- In a system with many channels (millions ?), the number of firing channels because of noise will thus depend on the chosen threshold.

- When looking at a time window where physics data is supposed to be present, those noise hits represent **the noise occupancy**, expressed in percentage.

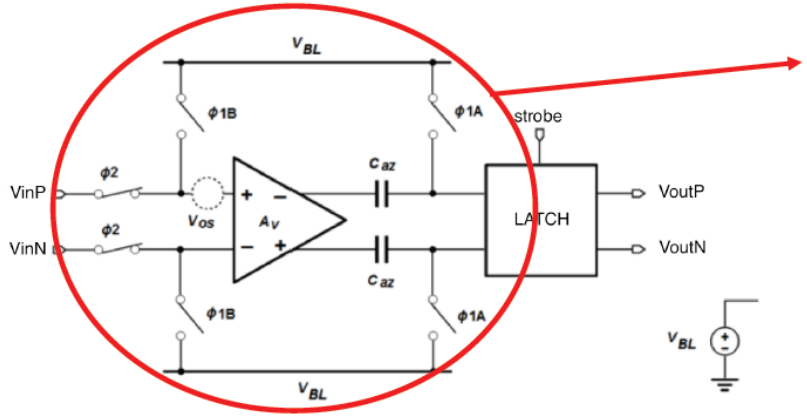
- There is obviously a **trade off** between the sensitivity of the system (lower threshold) and the noise occupancy. However, smart triggering systems may permit relaxing the constraints on the threshold thanks to a powerful rejection capacity based on time coincidences when this is feasible.

- If noise occupancy is too high, it will indeed eventually compromise data transmission capability. Furthermore, in ASIC with a big number of channels, a high noise hit rate may increase the interference on chip caused by the simultaneous switching of many comparators, triggering additional channels and leading to a positive feedback that could make the chip unusable.

Offset dispersion

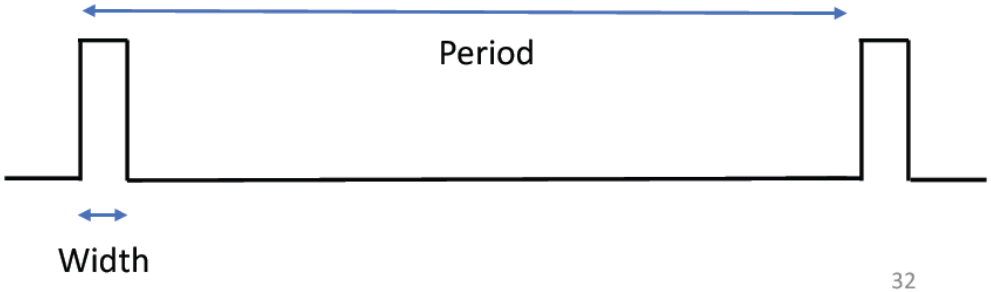
- So far we have assumed that the comparator has zero input offset.
- This is never the case, because of the dispersion existing between the nominally identical transistors that form the decision circuit.
- **An offset can be represented as an additional voltage source in series to the threshold**. Since its polarity is not known, it can either increase or decrease the effective threshold.
- In a multi-channel ASIC, each comparator will flip around its effective threshold. If the same nominal threshold is applied to the full system, **the highest value that guarantees an acceptable noise hit rate in the worst channel** must be chosen, thus **reducing the sensitivity** in the other ones.
- The effect of channel-to-channel threshold variation thus becomes equivalent to that of an additional random noise source, that in many cases **is higher than the intrinsic frontend noise**.
- To keep the threshold adequately uniform, **offset correction techniques** have to be used: by design (but with complexification), by use of compensation capacitors (autozero), by calibration and use of individual channel offsets, …

Autozeroing – How does it work



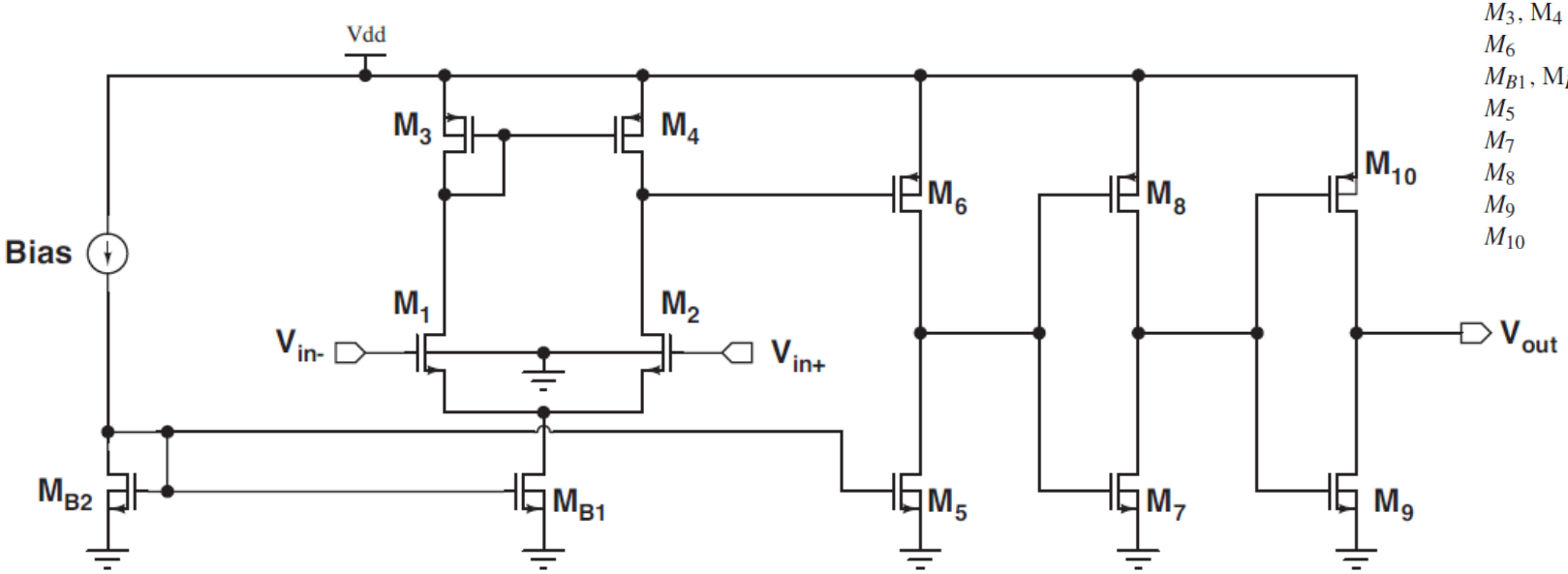
- When the autozeroing global pulse is sent the switches included in the block open (or close) in order to perform the offset compensation
  - In particular, with the rising edge the ϕ_2 group are opened and the ϕ_1 group closed and the opposite with the falling edge
- During this period in each pixels the offset value is stored in the capacitors
- As with time the capacitors tend to discharge due to leakage currents, this operation has to be periodically repeated
- If this is not done, the FE does not work properly

- Before irradiation a width of the autozeroing pulse equal to 400 ns with a period of 80-100 µs is enough
- After irradiation (beyond 200-300 Mrad at cold) width may have to be increased at around 1 µs or a bit more
- Both values are compatible with the abort gap time during the machine operation



Discriminator schematics

- You can see below the scheme of a simple discriminator formed by a two-stage CMOS OTA followed by a two-stage digital buffer..



M_1, M_2	20/0.3
M_3, M_4	3/0.3
M_6	12/0.3
M_{B1}, M_{B2}	10/0.8
M_5	20/0.8
M_7	1/0.2
M_8	4/0.2
M_9	2.7/0.2
M_{10}	10.8/0.2

- The gain provided by the amplifier part of this circuit must be sufficient to guarantee a transition from 0.2 VDD to 0.8 VDD for the minimum signal of interest.
- This corresponds to a range of about 1.5 V for a 0.25 µm technology powered at 2.5 V and 0.76 V for a 130 nm process, normally running at 1.2 V

Bandwidth

- The gain of the first and second stages is respectively given by:

$$A_{V01} = g_{m1}\left(r_{02}//r_{04}\right) = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

$$A_{V02} = g_{m6}\left(r_{06}//r_{05}\right) = \frac{g_{m6}}{g_{ds6} + g_{ds5}}$$

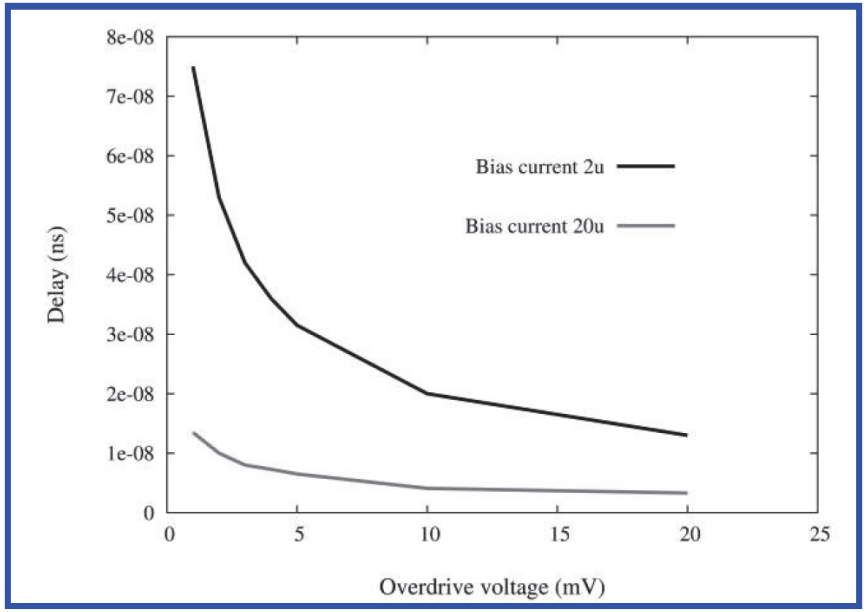
- Each stage contributes with its own dominant time constant to the speed limitation, so the overall transfer function can be written as:

$$A(s) = \frac{A_{V01}A_{V02}}{\left(1 + s\tau_1\right)\left(1 + s\tau_2\right)}$$

- **The strongest cut to the bandwidth is usually introduced by the first stage**, because the Miller multiplication increases the effective value of the gate-drain capacitance of M6.
- Hence, the use of the simple single pole model often yields reasonable simulations

Discriminator behaviour

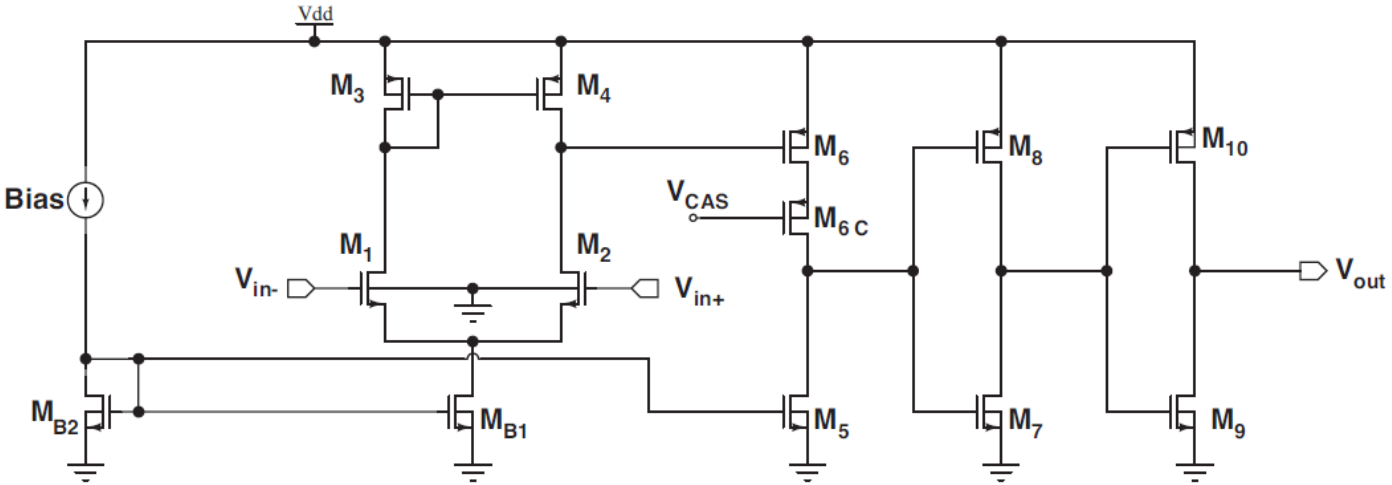
- Let's look at the discriminator delay with two different bias currents: 2 μA and 20 μA
  - 2 μA corresponds to a usual value in circuits for which very low power consumption is mandatory, such as front-end ASICs for hybrid pixel detectors, where thousands of channels are packed together on the same chip.
  - 20 μA corresponds to a more usual value in most applications, still ensuring a reasonable power consumption.
- At 2 μA, the stage gains are AV01 = 18.62 and AV02 = 34.7, leading to a total gain of 646 or 56.2 dB, sufficient to make the comparator flip when the input voltage changes by ±1 mV around the threshold point.
- At 20 μA, the total gain decreases to 538, but it leads to an almost tenfold increase in the bandwidth.
- Note the much higher speed for the higher bias current and the steep increase of the delay for small overdrive voltages.



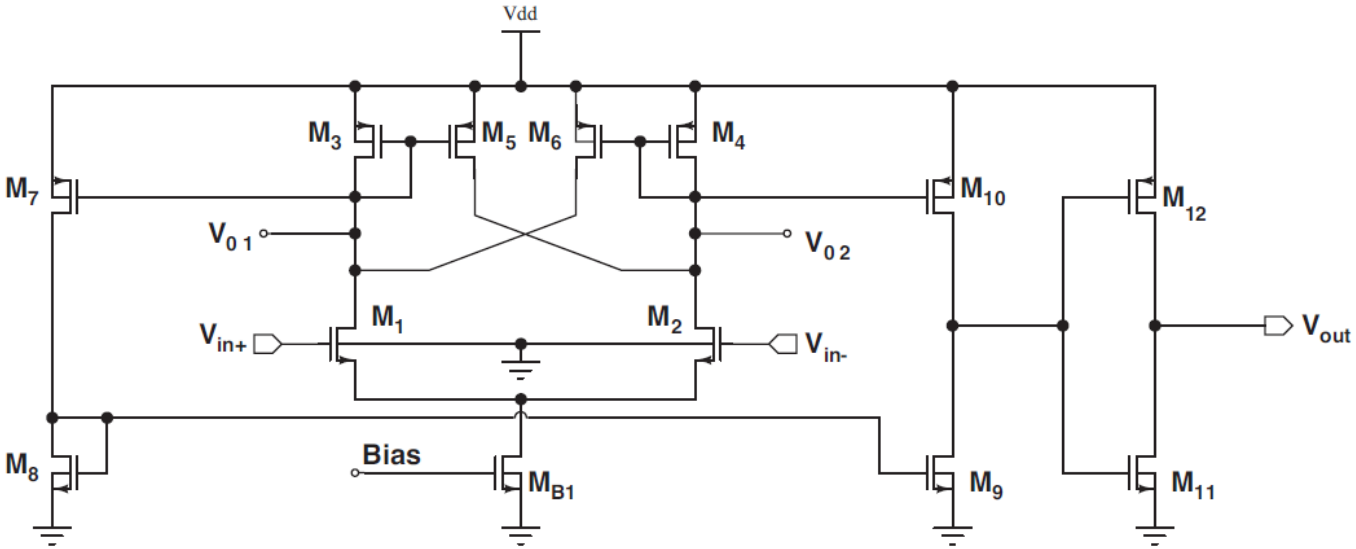
Smarter designs …

- The basic scheme of the comparator can be improved in different manners

- Addition of a cascode (M6C) in the second stage => gain raises to 1500.



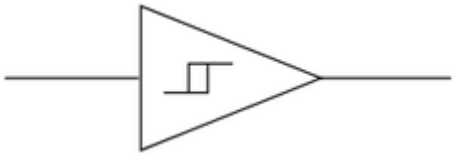
- Use of cross-coupled active loads in the first stage => higher gain and possibility to unbalance to introduce hysteresis.



About hysteresis

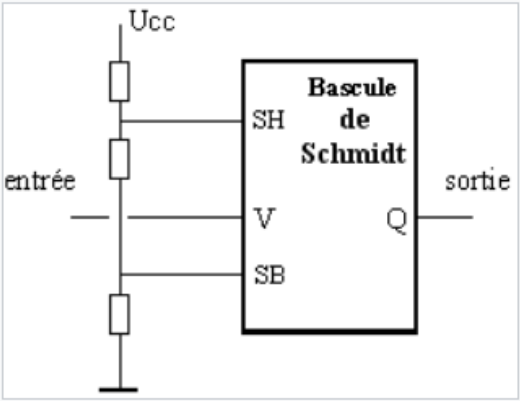
- Hysteresis in electronics is the fact of having **different thresholds for the rising and falling edges of the signal**.
- This permits **rejecting the noise** when the signal crosses the threshold and ensuring **a single transition** at the discriminator output.

Schmitt trigger symbol

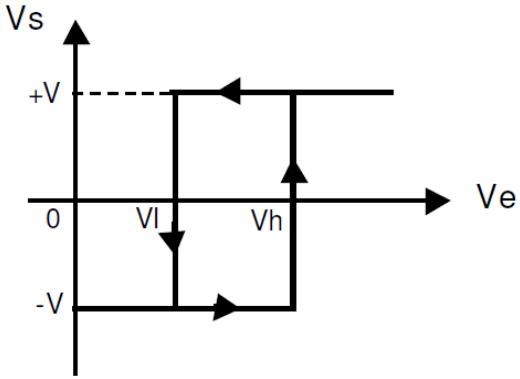


- Such a discriminator is usually called Schmitt Trigger.
- It is **widely used at the input of digital circuits**, like FPGAs.
- But it doesn't permit performing TOT measurement (see later)

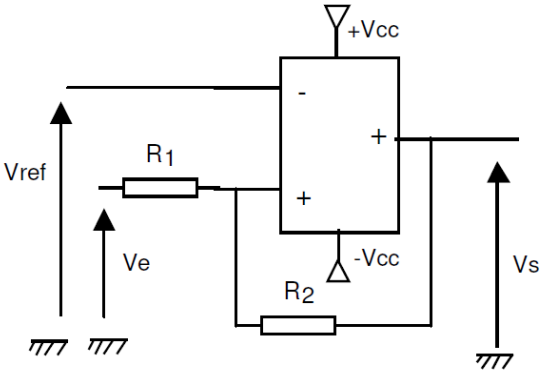
Generic principle



Hysteresis cycle



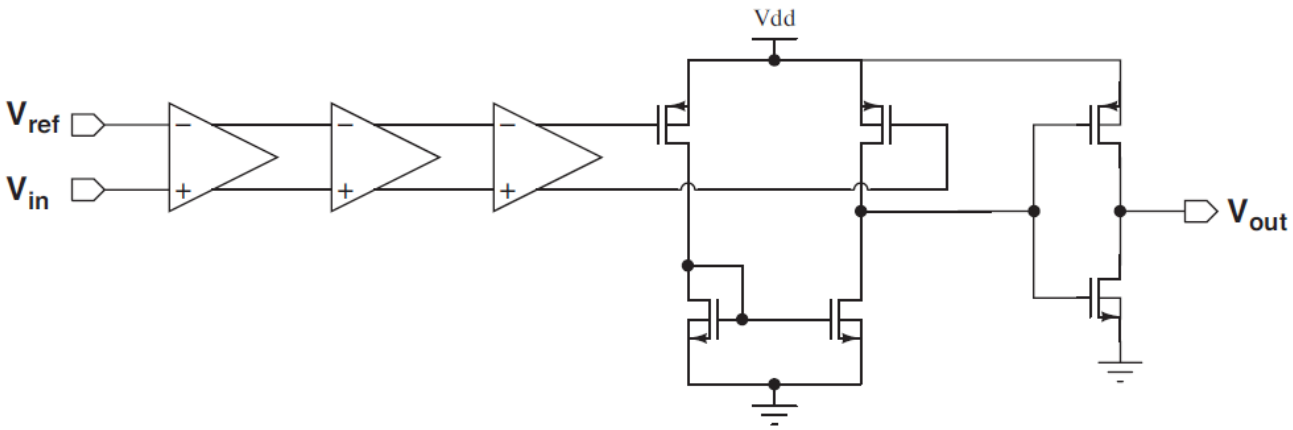
Example of implementation using a standard comparator (can be done on board)



Rules for high speed comparators

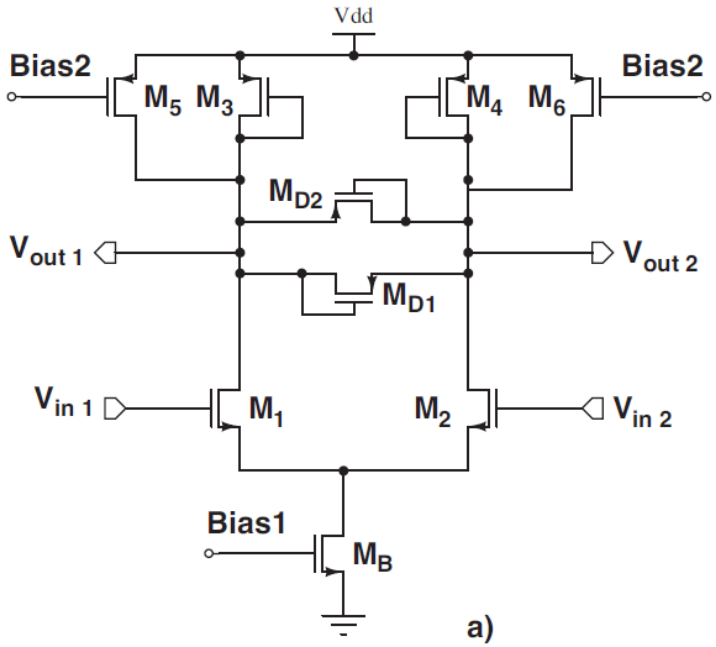
- We have seen previously that to achieve enough gain many stages need to be cascaded.
- In case of first order systems, calculating the optimal number of stages n that reaches the desired total gain A_T with the maximum speed gives $n = 2 \ln A_T$
- For instance, for $A_T = 1000$, n = 14 with a individual stage gain of 1.63! This would lead to a huge power consumption!
- The number of stages is thus a trade-off and usually 3 to 5 are used.
- **General rule**: to maximize the speed, a discriminator must be implemented **cascading low gain cells**.

- The high speed, low gain blocks normally use a fully differential topology and are followed by a final high gain module that performs also the differential to single ended conversion.

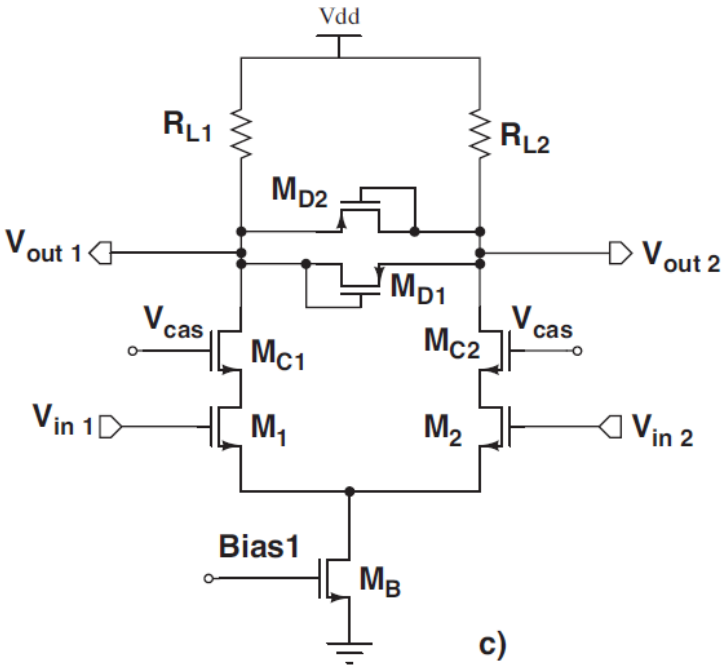


Gain cells for fast discriminators …

- Those are example of fast gain cells:



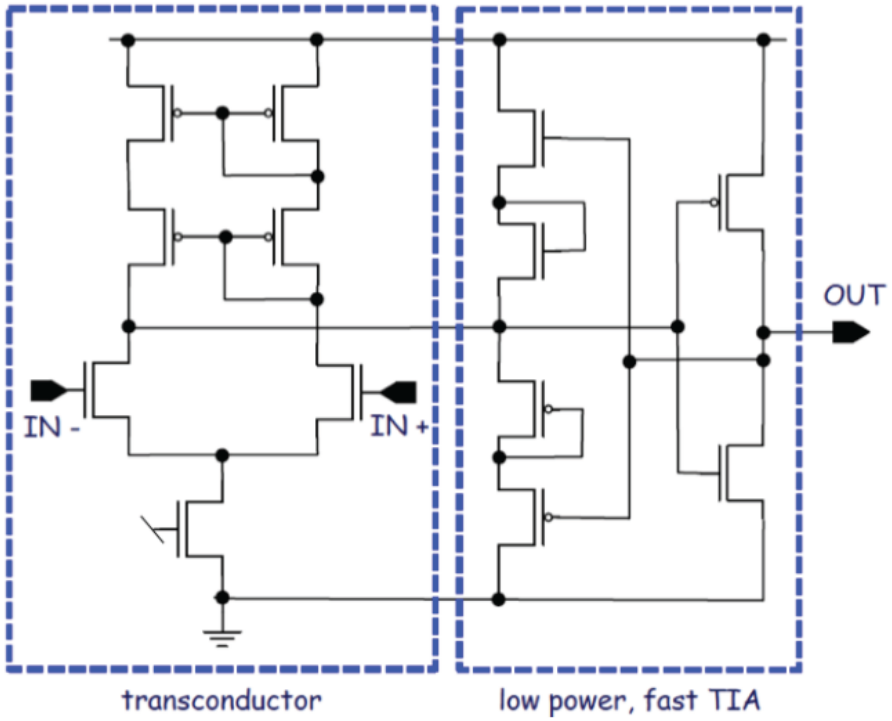
- The baseline topology, reported in a), consists of a differential pair with active diode connected loads.
- M5 and M6 diverge a part of the current and increase the active loads.
- M1 and M2 can be cascoded (as below).



- When high resistance polysilicon film are available, it can be advantageous to implement the loads as passive resistors, that might offer a smaller parasitic capacitance.

Discriminator used in RD53A

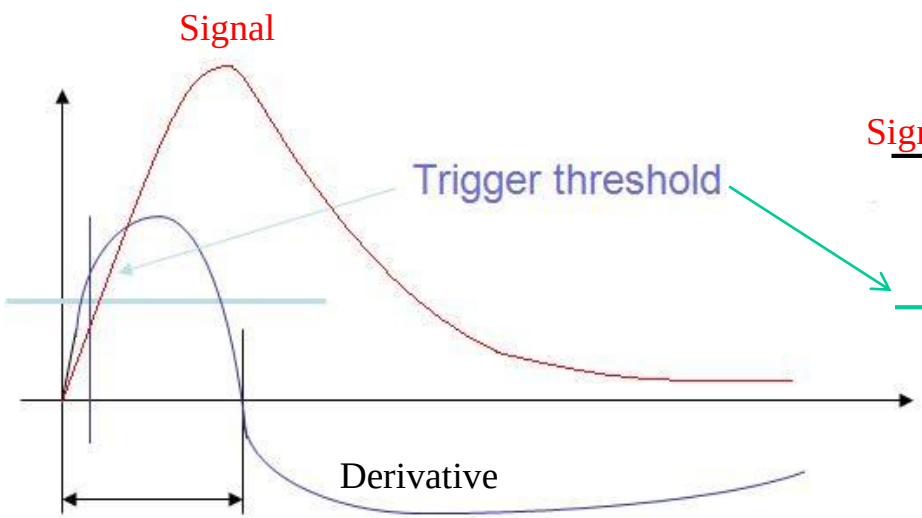
COMPARATOR

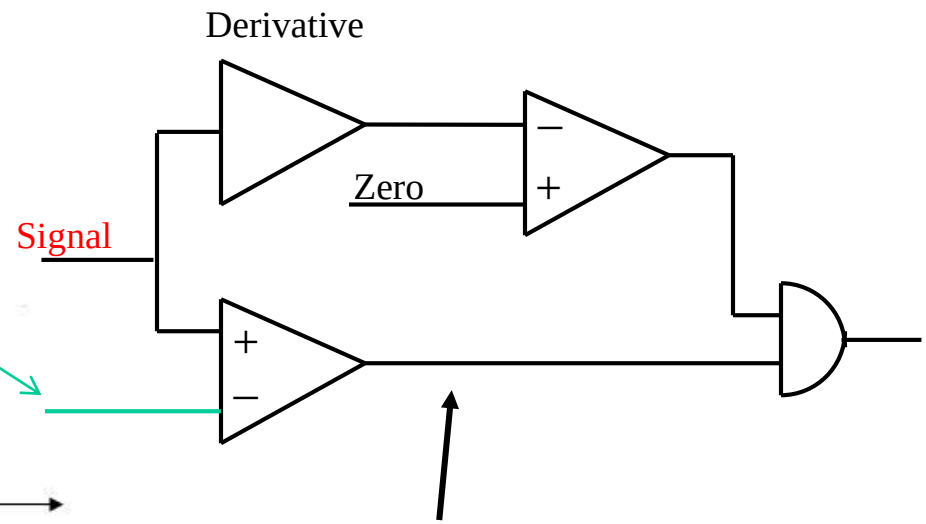


- Low power, **fast discriminator** (~ 1 uA absorbed current) including Gm stage and a transimpedance amplifier providing a low impedance path for fast switching

Zero crossing

- There are many different ways to implement a discriminator.
- For instance, when looking for **the position of the peak of the signal**, the zero crossing of the signal derivative can be used:

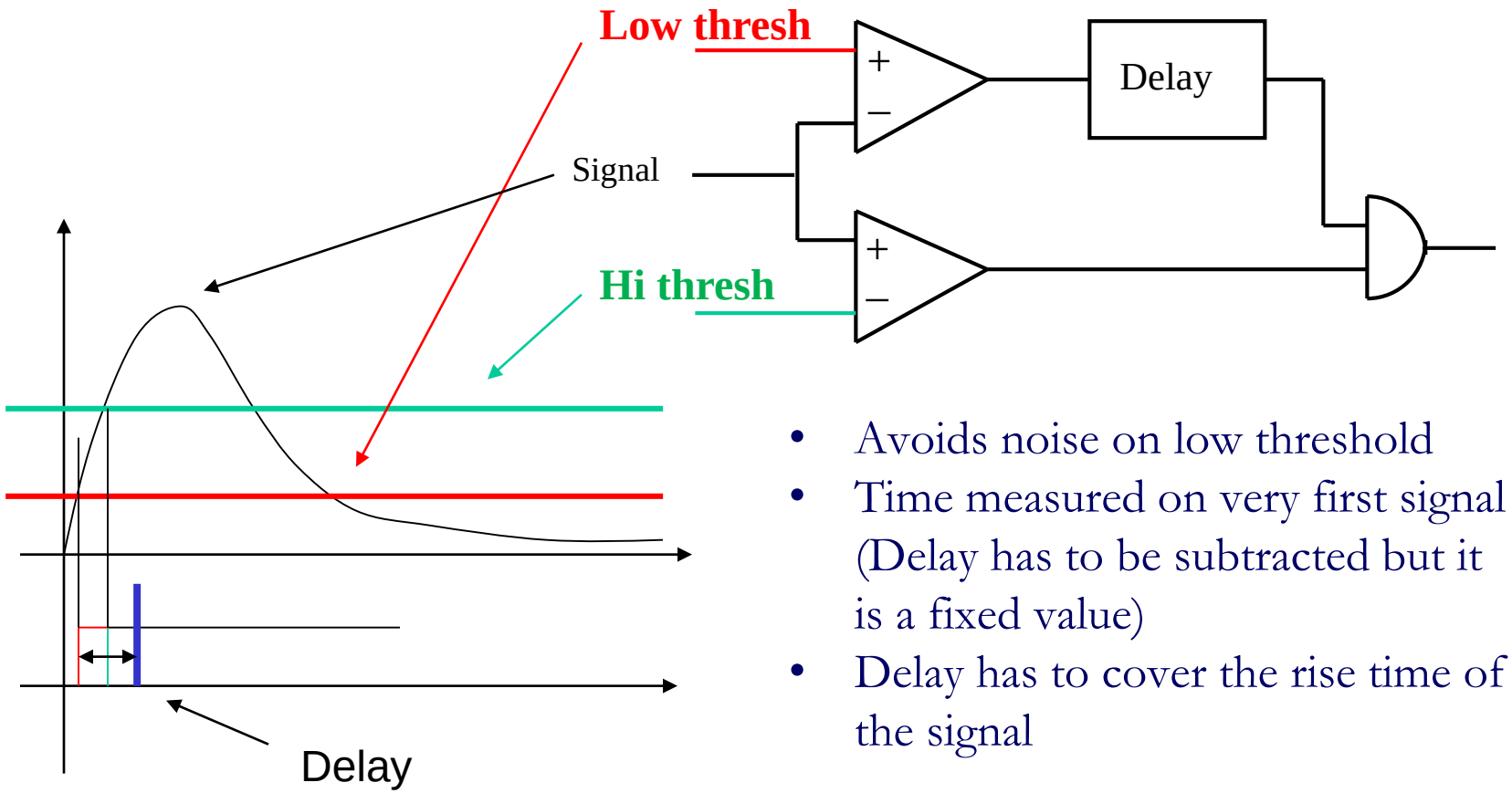




- This branch permits rejecting noise on the derivative
- Zero crossing can trigger only if the signal is above the threshold

Double threshold

- Imagine you want to have a reasonable timing precision but trigger on rather big signals to reject noise => you can use the double threshold method
- Lower threshold will be used for timing but only if higher threshold has also been crossed.

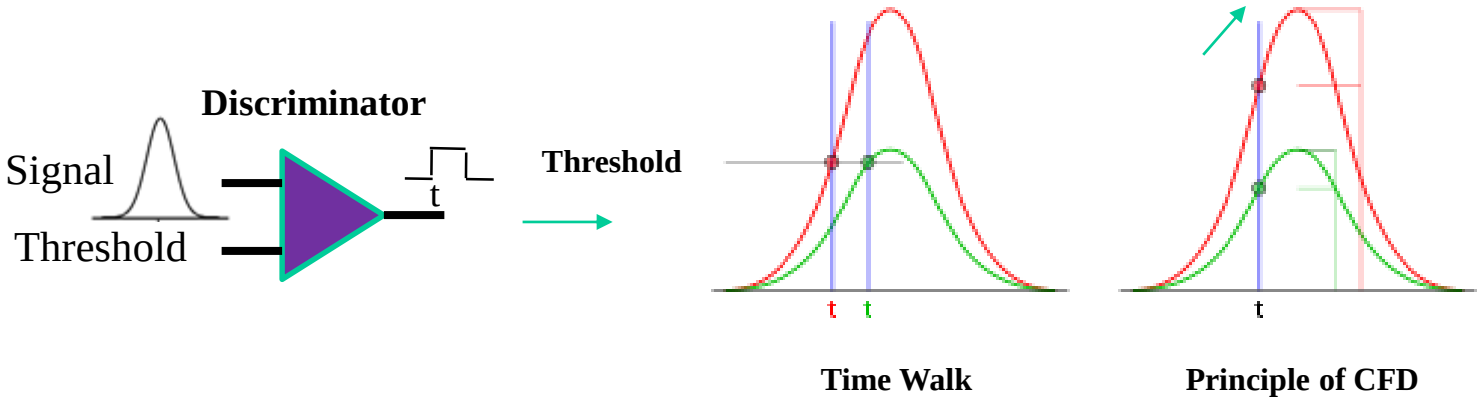


- Avoids noise on low threshold
- Time measured on very first signal (Delay has to be subtracted but it is a fixed value)
- Delay has to cover the rise time of the signal

Time walk

A discriminator translates an analog signal into a digital pulse.

When sending a signal to a discriminator, the time instant "t" of the output level toggle will depend on the amplitude of the signal => "Time Walk" Effect



To avoid this effect, one can use a Constant Fraction Discriminator (CFD)

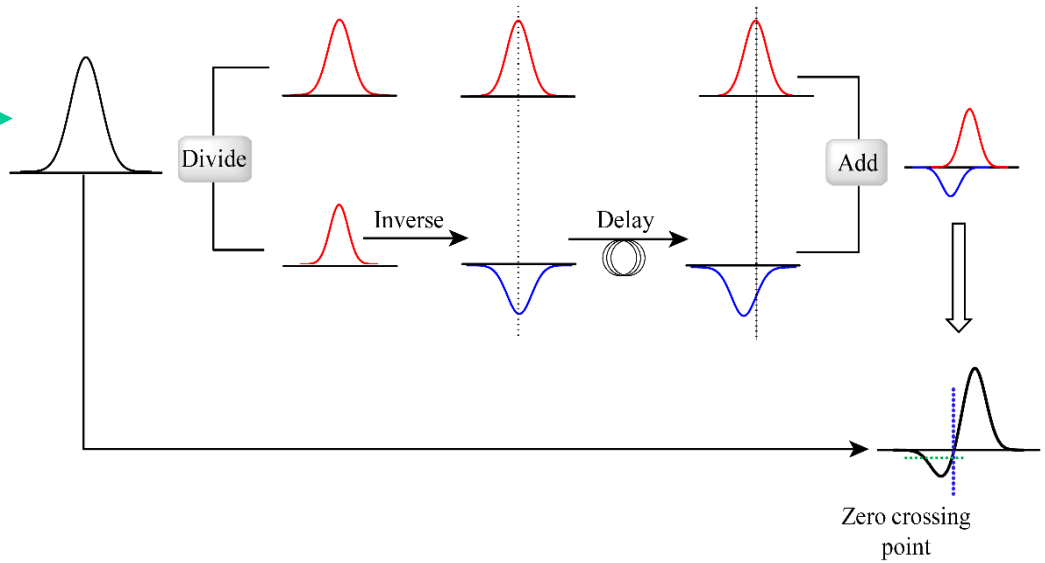
- **Here, the threshold is defined as a constant fraction of the peak**
- **But this implies that you need to know the value of the peak to apply the threshold !**
- **Ok for a firmware or software when the signal has been digitized but harder before…**

Constant Fraction Discriminators

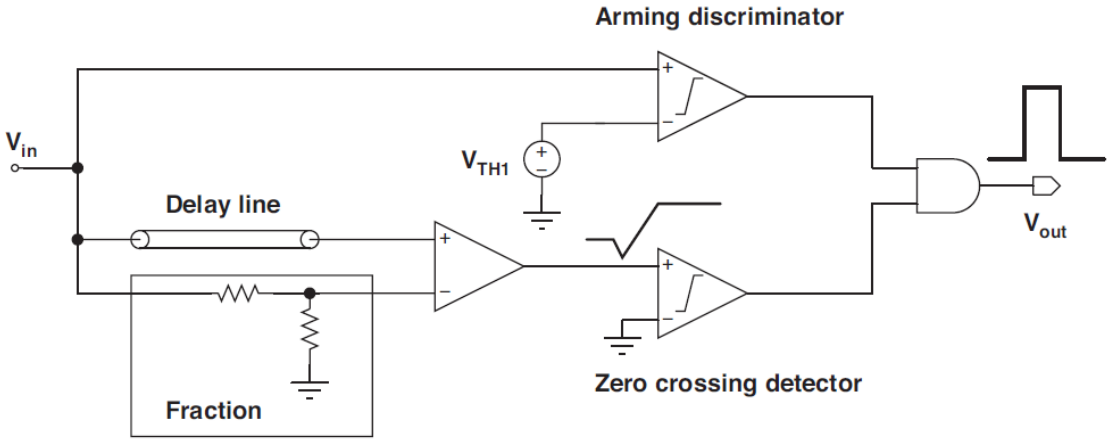
How to make a CFD in an analog way in front of a TDC:

- **but never perfect (there is always a residue of time walk)**
- **hard to integrate in an ASIC because of the delay line (needs inductances)**

=> other options are used but they degrade the performance



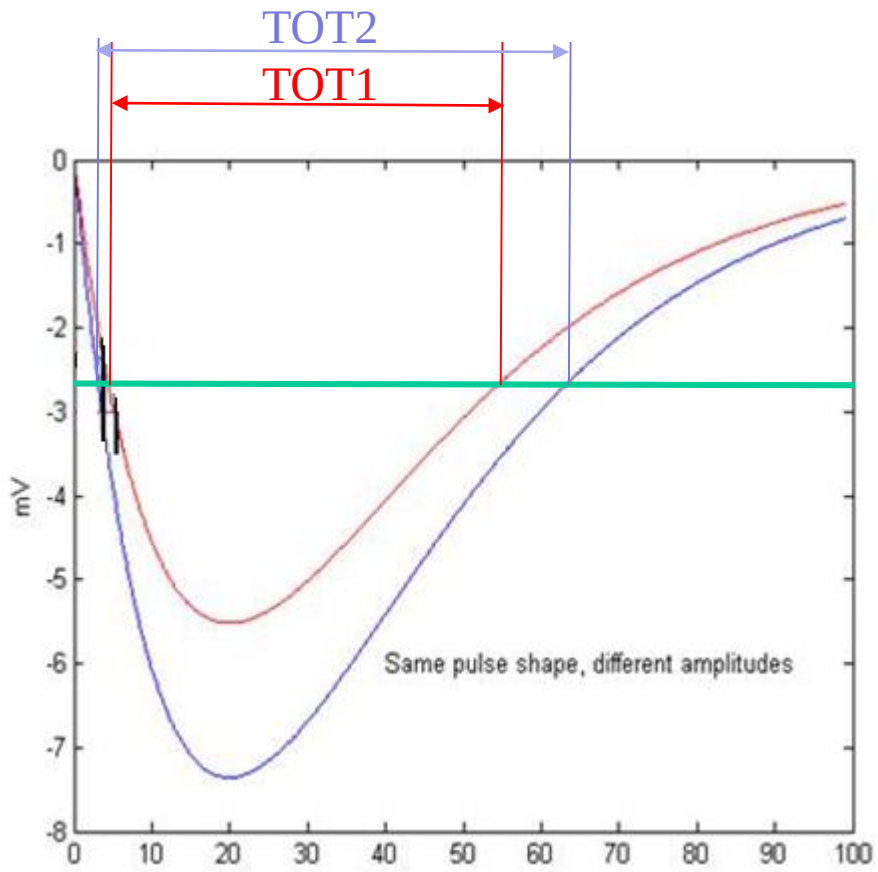
An arming discriminator is required in order to avoid triggering on baseline noise



Single threshold + TOT measurement

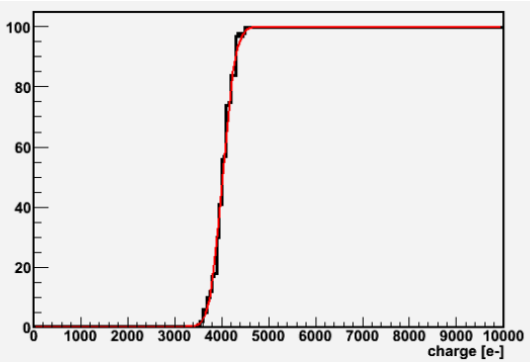
- The time walk of the simple leading edge discriminator can be corrected offline thanks to the **Time Over Threshold** (TOT) measurement.
- Therefore, the signal must have a constant pulse shape, independently of its amplitude

- A calibration of the threshold crossing time and TOT vs the signal amplitude has to be performed
- Both threshold crossing time and TOT will be measured on real data.
- The calibration will be used offline to correct the measured time
- TOT can be a way to measure the signal amplitude with a discriminator and a TDC …

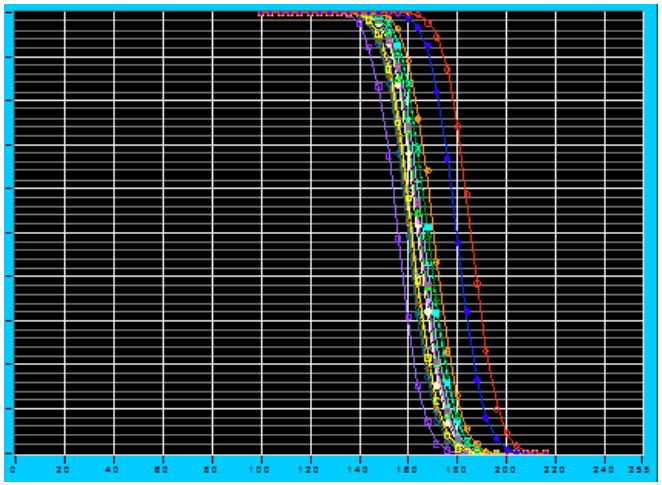


S curve

- When ones wants to characterize a discriminator, an usual way is to measure its **probability of triggering with respect to signal amplitude and threshold**
- Two methods are possible:
  - Fixed threshold and variable pulse amplitude
  - Fixed pulse amplitude and variable threshold (easier)



- The representation of the triggering probability curve of a signal will then be a curve looking like the letter « S » or an inverted « S »
- The spread in abscissa between the 0% and 100% in probability gives information about the noise (including the discriminator)
- The width of the pulse is a parameter which can prevent the discriminator from triggering even if threshold is crossed (if too short)
- A discontinuity in the curve would be a proof of problem in the design



Typical S curves for signals in a multi-channel ASIC

Use of discriminators

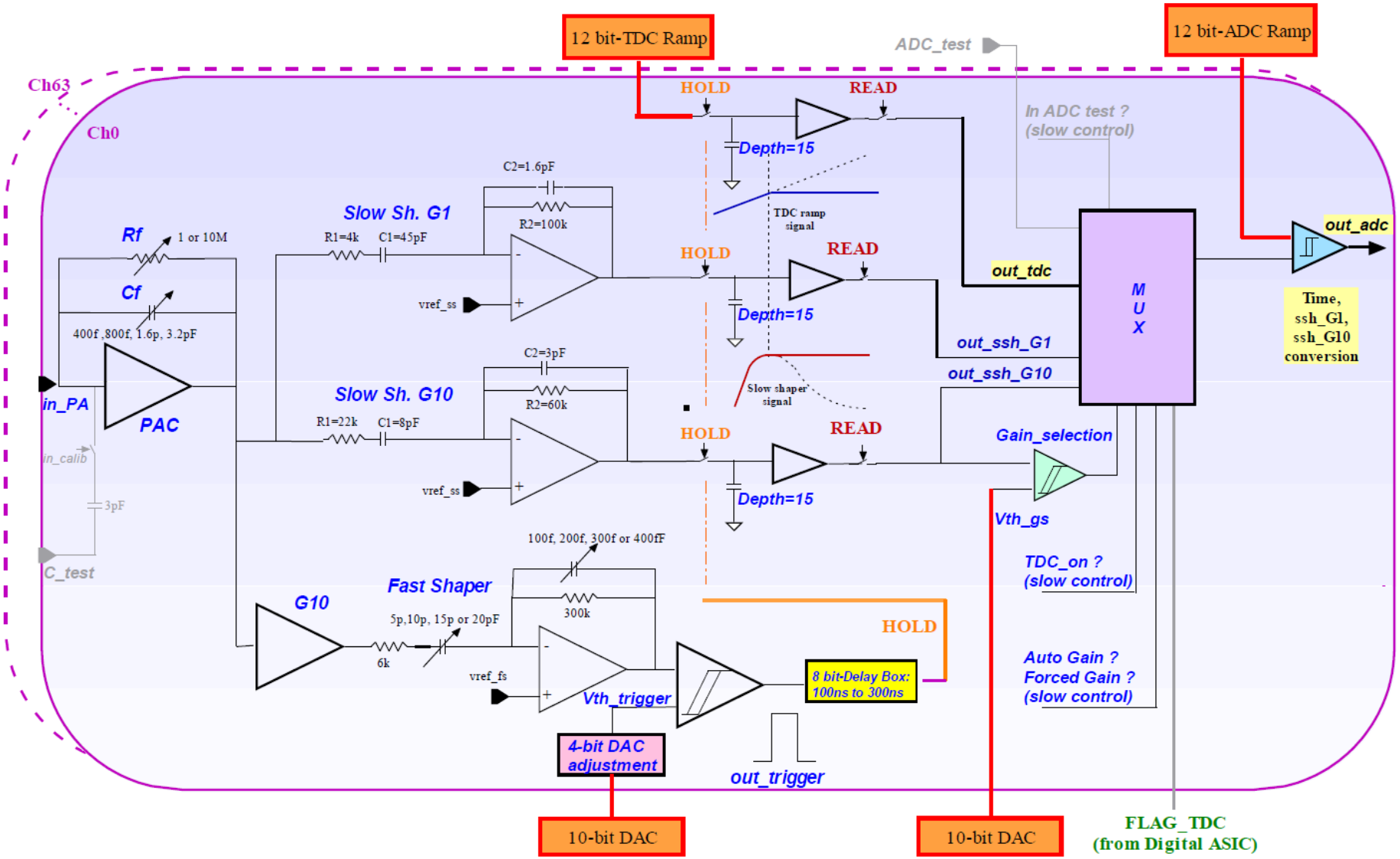
- Now that we have seen how a discriminator is designed, let's concentrate on what it can be used for …

- There are 2 main uses for asynchronous discriminators:
  - **Trigger logics**: it will select the events which will be transmitted to the computers via the acquisition system. Decision is based on digital primitives sourcing in the discriminators… It can sit inside or outside ASICs.
  - **Time measurement**: there is a mandatory need to go from analog to digital in order to measure the arrival time of a signal. The discriminator can be used in 2 different ways:
    - To perform the measurement => classical TDC
    - To flash the signal => WaveForm TDC

- It is important to notice that **an ADC permits measuring the arrival time of a signal** if the sampling frequency is adequate (high enough) because the digitized samples contain all the signal information.

Typical use inside front-end ASICs …

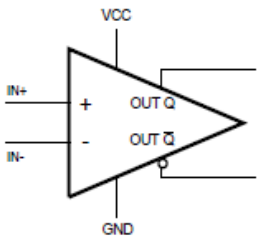
- SKIROC2 : multiple uses of discriminators appear here…

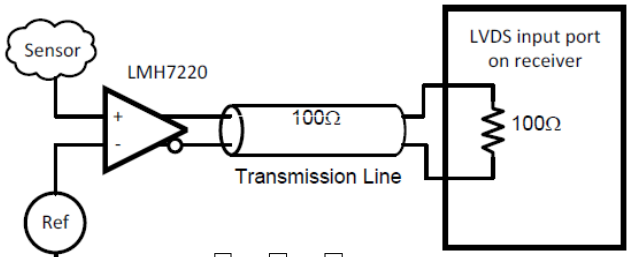


Discrete components

- Discrete comparators are also **widely used on boards, sending digital signals to FPGAs**.
- Here is an example of the one I use very often: LMH7220 from TI

- It has a very small package with 2 options: SOT23 or SOT70.
- It is fast but with a low static power consumption (7 mA)
- Its output is differential current (LVDS) so it introduces very little crosstalk towards the analog world around it and ensures an excellent timing performance
- The only difficulty is that the differential output level is referenced to its lower power rail, which can be a problem when one wants to also cover a negative threshold range (I found ways to overcome it)





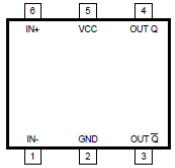
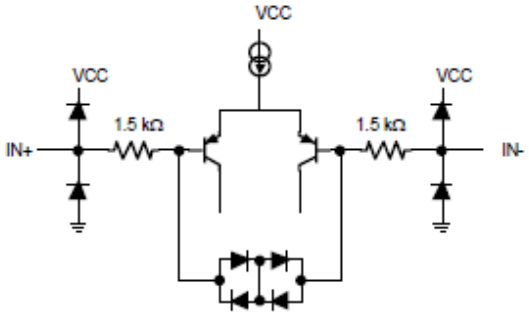
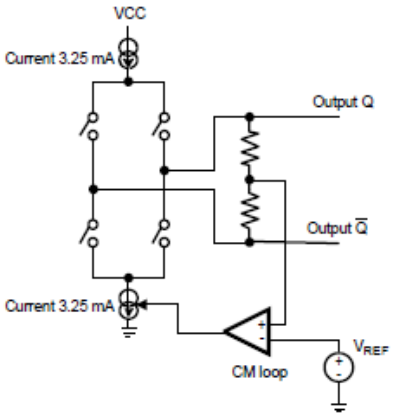


Figure 3. 6-Pin SOT Top View

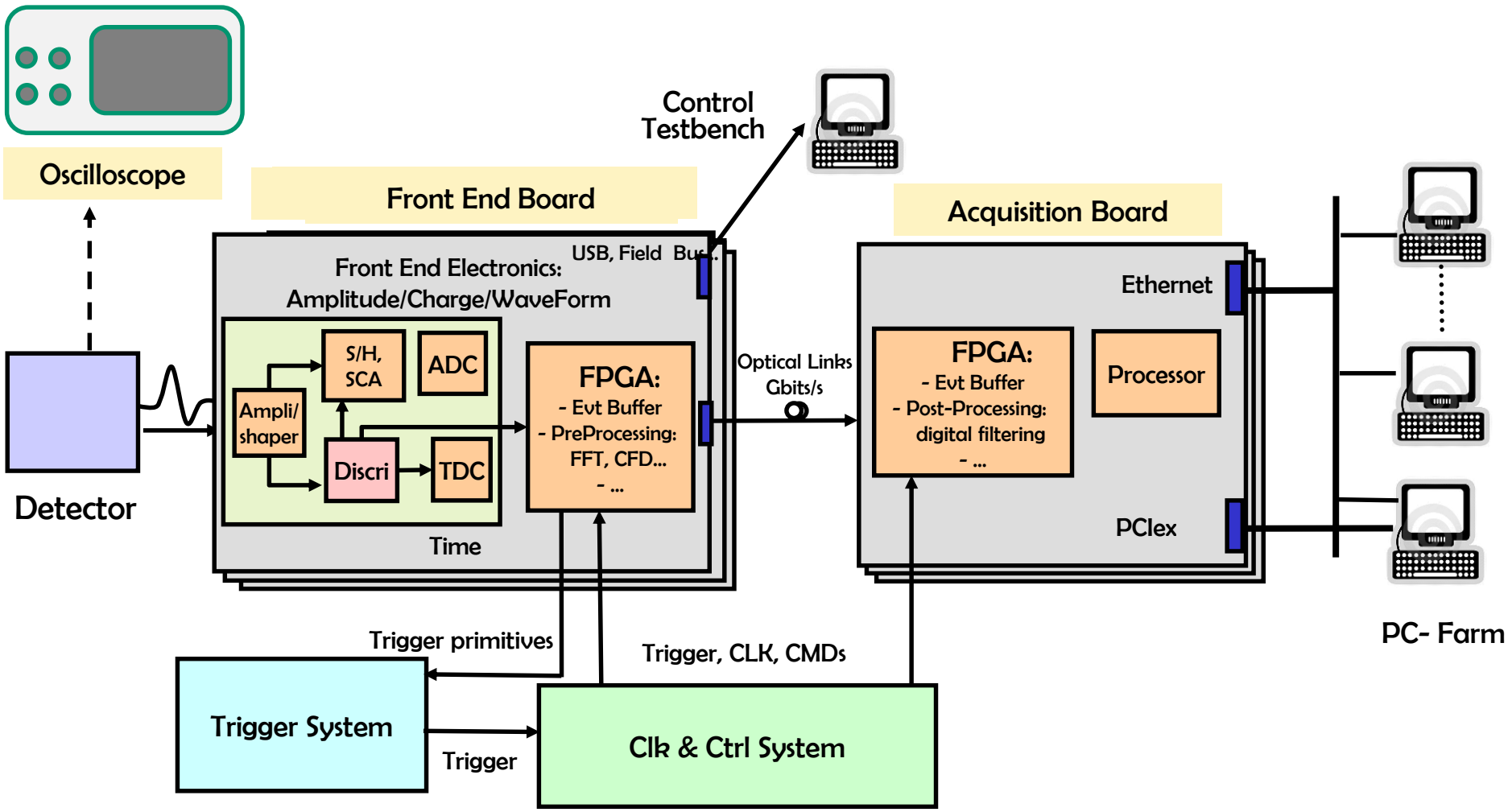


Equivalent Input Circuitry

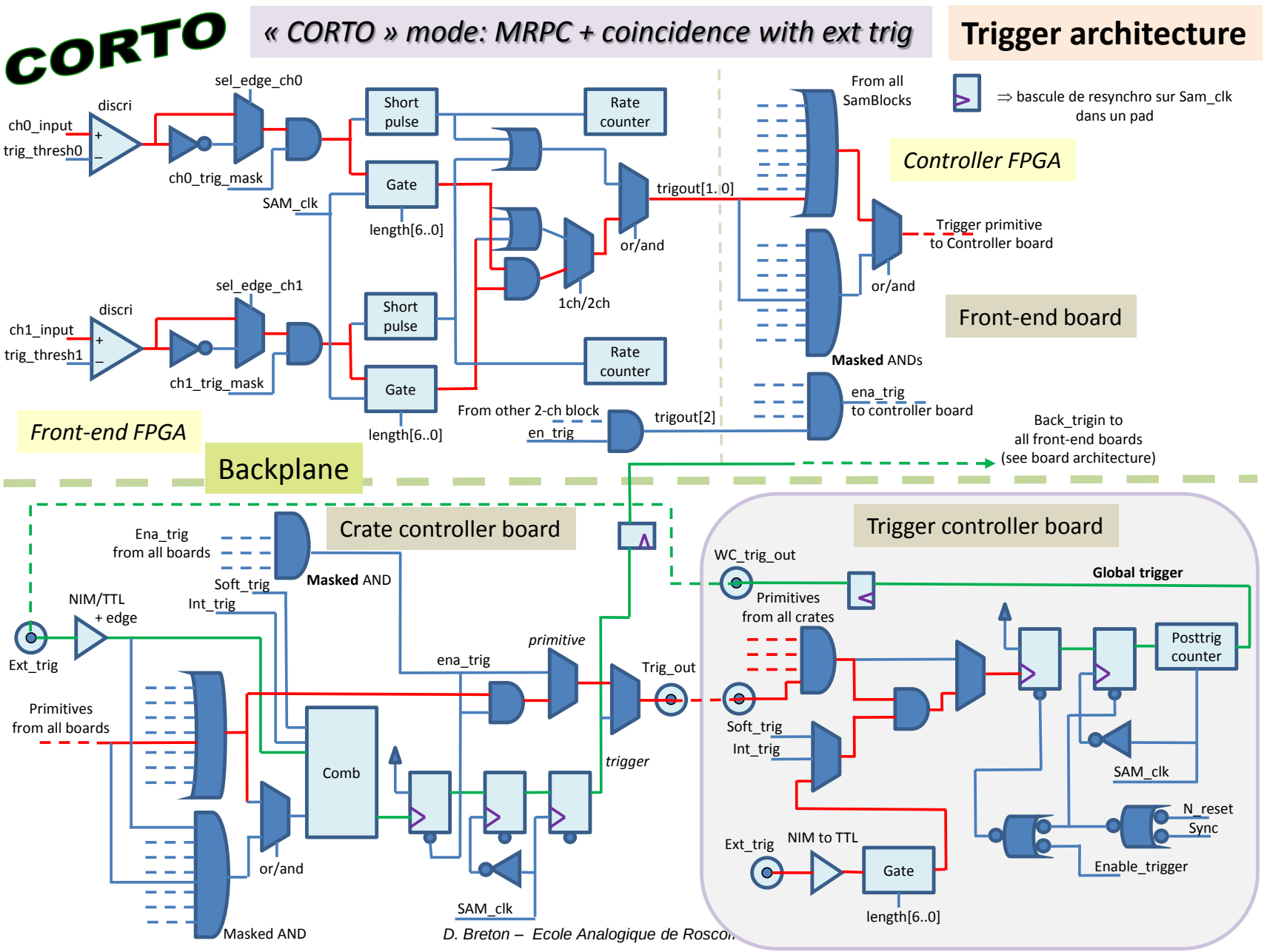


Equivalent Output Circuitry

A typical detector measurement chain …

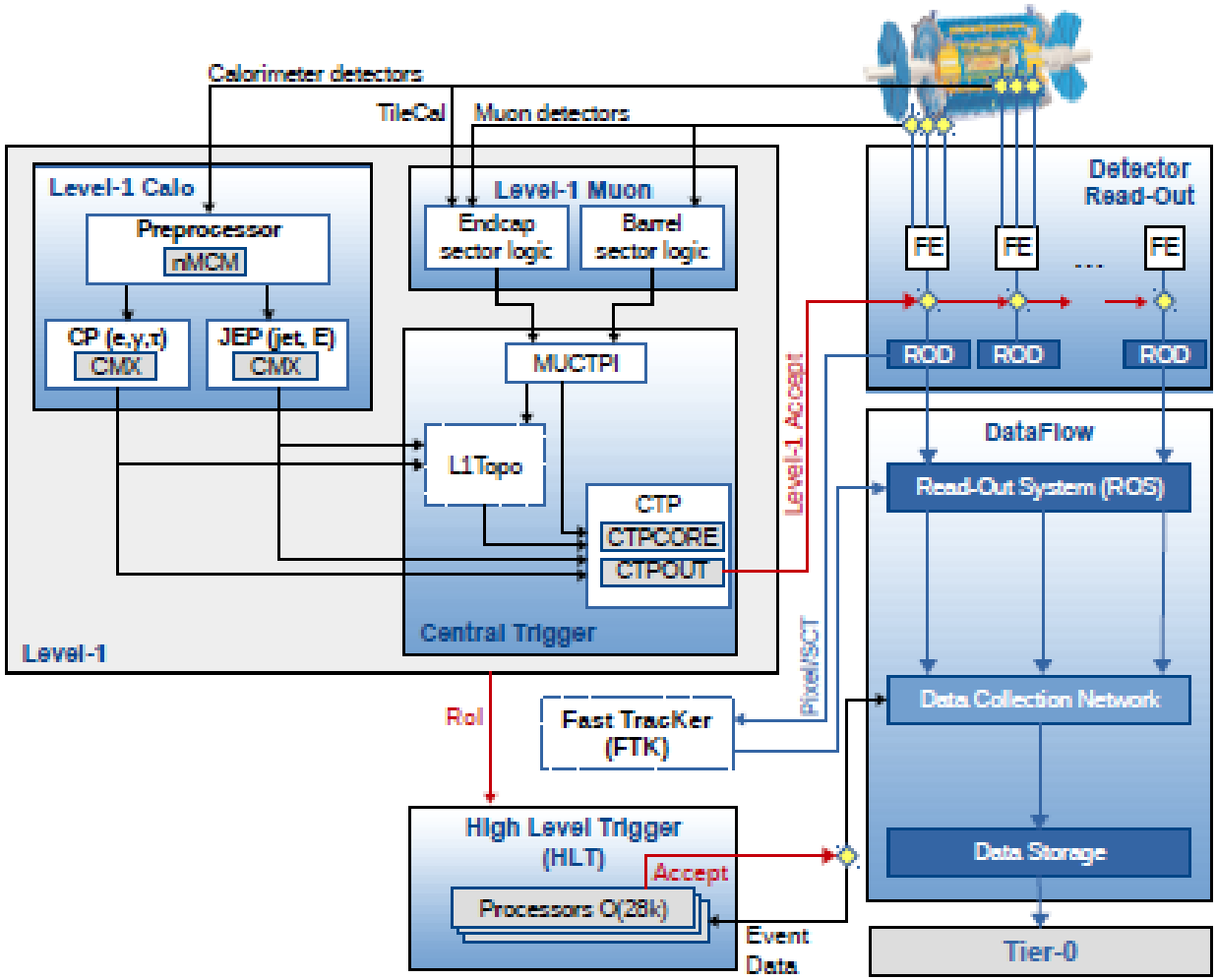


Système de trigger d'un téléscope cosmique : CORTO@LAL



Le système de trigger d'ATLAS au CERN

- Sur la base de discriminateurs à seuil et de sommateurs analogiques rapides répartis dans l'électronique front-end, un système de trigger complexe à plusieurs niveaux est mis en oeuvre.

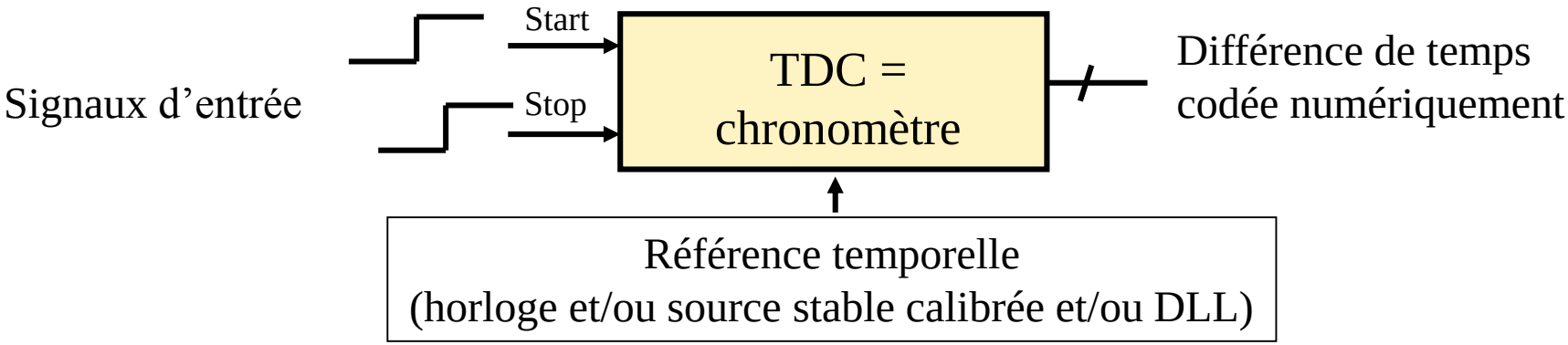


La mesure de temps dans les expériences de Physique

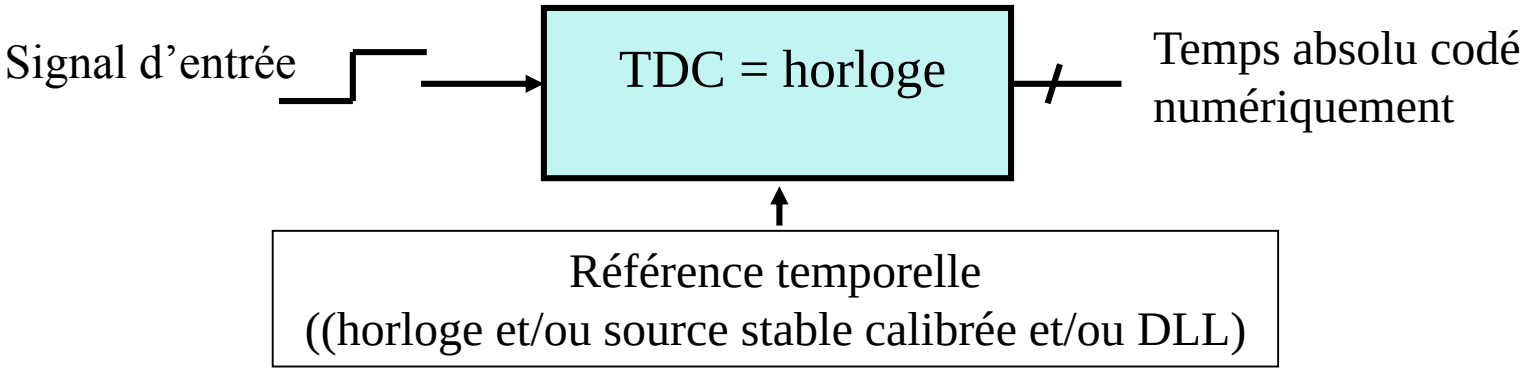
- Dans les systèmes multicanaux :
  - Moyen **d'associer les signaux de différents détecteurs correspondant à un même événement**.
  - Permet de remonter le temps:
    - Pour réaliser des Coïncidences en temps différés
    - Associer des évènements à un trigger => filtrage des évènements.
- Mesure de temps de vol:
  - discrimination de particules (trajectographes).
  - localisation d'interactions entre particules (PET scanners).
  - spectrométrie de masse.
- Mesure de position : chambres à dérive, TPC, strips.
- Mesure « économique » de Charges via la mesure du TOT.
- Mesure de Temps de montée :
  - Reconnaissance de Forme de signal.
- Conversion analogique numérique (ADC Wilkinson….).

Le TDC …

- Il y a deux types de TDCs (Time to Digital Converter) :
  - Celui qui mesure la différence de temps entre deux signaux



  - Celui qui mesure un temps « absolu »



Les paramètres techniques des TDCs.

- Même si les informations d'entrées et sortie sont binaires, le temps est une quantité analogique: le cœur du TDC est un circuit mixte analogique/numérique (nombreuses similitudes avec les ADCs).

- Les principaux paramètres sont similaires à ceux des ADCs:
  - La dynamique de mesure (DR).
  - Le pas de quantification de la mesure (q): $\boldsymbol{\sigma_q} = q / \sqrt{12}$
  - Les non-linéarités de conversion (INL et DNL).
  - Le « bruit » sur la mesure de temps = gigue (jitter): $\boldsymbol{\sigma_t}$
  - Le temps de codage.
  - Le temps mort: incapacité de coder deux signaux proches.

  Contribuent à l'erreur de mesure

- Les dispositifs élémentaires à grande DR ont en général une faible précision et inversement:

  ⇒ Pour avoir les deux : dispositifs composites =>

  ⇒Mesure grossière (compteurs) + interpolateurs analogiques ou numériques (éventuellement multiples).

Asynchronisme

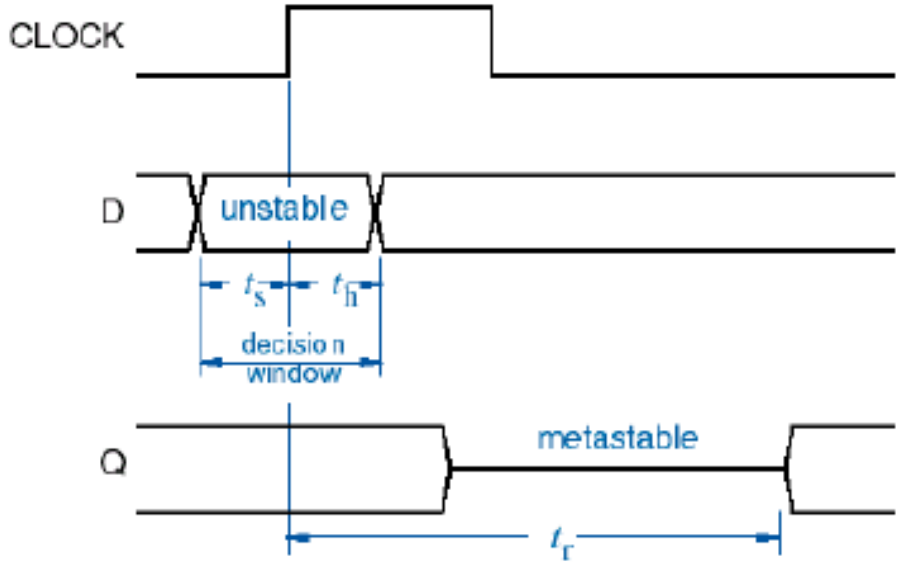
- La plupart des TDCs utilisent comme signaux de référence:
  - Soit un signal d'horloge de référence.
  - Soit un signal de démarrage et/ou d'arrêt.
  - Soit un mélange des deux.

- Le signal à coder peut être:
  - synchrone de l'horloge => codage « évident » (on compte les cycles d'horloge).
  - asynchrone => les ennuis commencent ! Si ce signal est échantillonné par l'horloge ou échantillonne un signal synchronisé par l'horloge:
    - Il est nécessaire de le resynchroniser pour travailler dans un contexte de logique synchrone.
    - Ou vivre avec des risques de **métastabilité** et en être conscient.

Métastabilité….quand la logique devient analogique.

Ce type de fonctionnement peut se produire:

- sur tous les types de points de mémorisation, y compris les bascules D (DFF) et les bascules RS.
- lorsqu'il y a une violation de temps de setup ou de hold sur les bascules :
  - CK bougeant simultanément avec DATA sur DFFs.
  - glitch sur entrées CK (DFF), R ou S (RS)
  - …..



Métastabilité….quand la logique devient analogique.

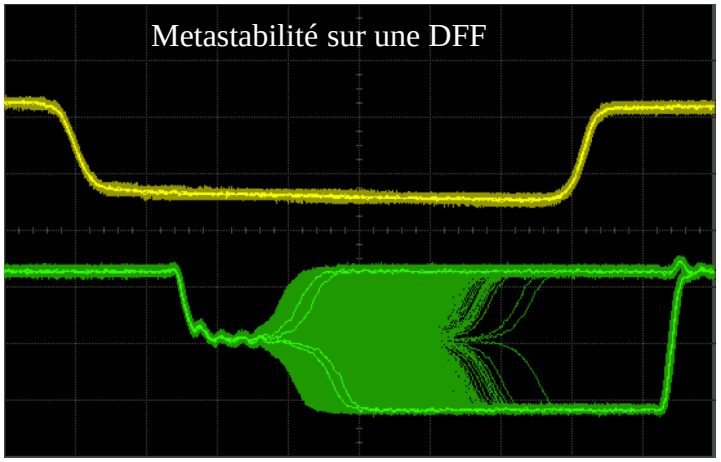
• La sortie de la bascule prend un état… **analogique**, éventuellement oscille et finit par prendre une décision.

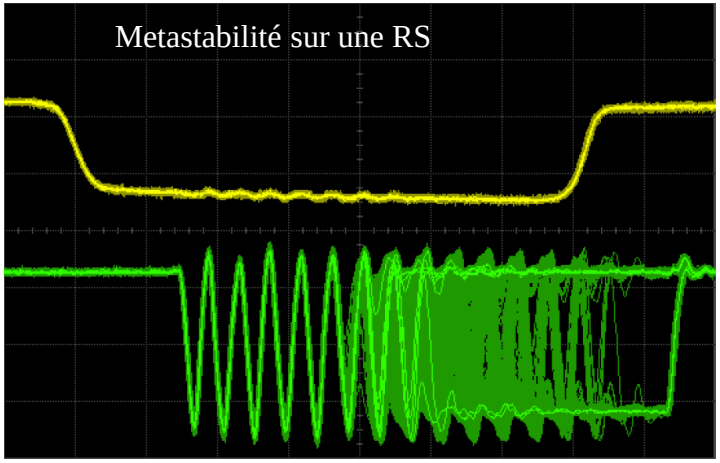
• La probabilité de rester dans un état métastable est en $\mathbf{e}^{-t/tr}$, où $\mathbf{t_r}$ est un temps caractéristique très court

• La propagation de l'état métastable dans la logique de traitement peut provoquer un fonctionnement erratique, des erreurs de codage, des plantages (par exemple 2 soumissions du chip ARS pour ANTARES à l'IRFU).

=> s'il y a risque de métastabilité inévitable, le design doit être « durci » pour vivre avec…

Metastabilité (2)





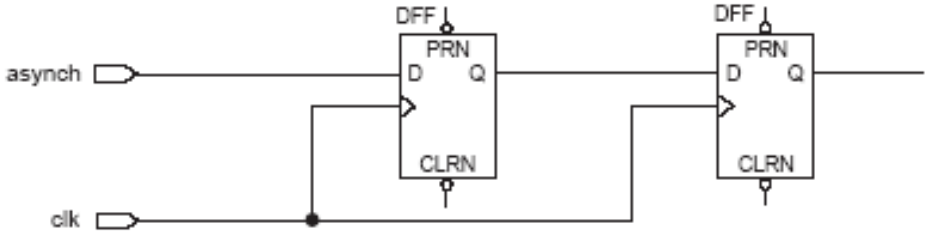
- La fenêtre d'apparition de la métastabilité, donc sa probabilité d'apparition ainsi que le temps caractéristique de récupération t sont d'autant plus faibles que les bascules sont rapides.

  => technologies très fines favorables.

  => RS moins sensible que DFF car plus rapide.
- Fenêtre interdite de l'ordre de quelques dizaines de ps, également dépendante de la qualité de l'alimentation.
- Difficile à voir en simulation (dépendant de l'algorithme de convergence et du simulateur).
- Il existe des bascules « durcies » à la métastabilité.

Resynchronisation

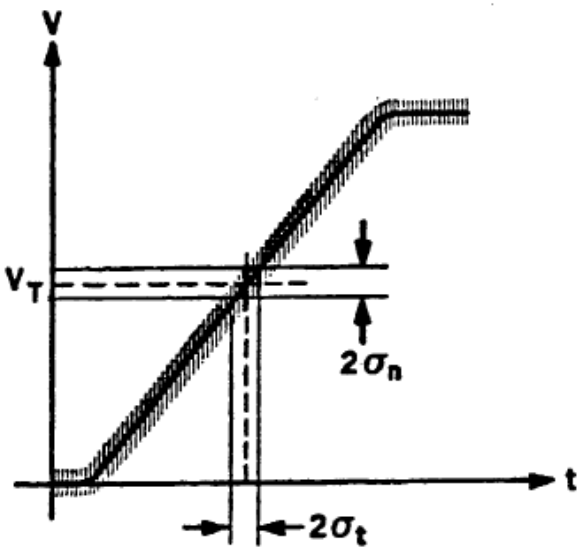
- On ne peut pas éliminer la métastabilité, mais on peut en réduire les effets grâce à un circuit de resynchronisation.



- Si la première bascule a subi une métastabilité, il est très peu probable qu'elle soit encore dans un état indéfini lors de l'échantillonnage par la deuxième bascule.
  - Soit elle est dans le bon état logique => tout va bien
  - Soit elle est dans le mauvais => on prend un coup d'horloge de retard mais c'est pas grave car notre signal était asynchrone
  - Soit elle est dans un état indéfini, et il peut se propager …
- Attention: ce dispositif réduit la probabilité de métastabilité, mais ne l'élimine pas.
- Inconvénient: latence de 1 coup d'horloge sur le signal resynchronisé.

Source de gigue des signaux logiques (Jitter).

- Conversion du bruit en tension en bruit temporel:
  - $\sigma_t = \sigma_n / (dV/dT)$



⇒ jitter σ_t plus fort si signaux lents

⇒ mais bruit σ_n plus fort si plus de bande passante pour un signal très rapide

=> Optimum à trouver en fonction des cas …

- Les modulations lentes des alimentations, modifiant les temps de propagations sont également sources de jitter .

  ⇒ Faible jitter <= Faible bruit <= alimentations et substrat propres…

  <= Structures différentielles ou à bon pouvoir de réjection.

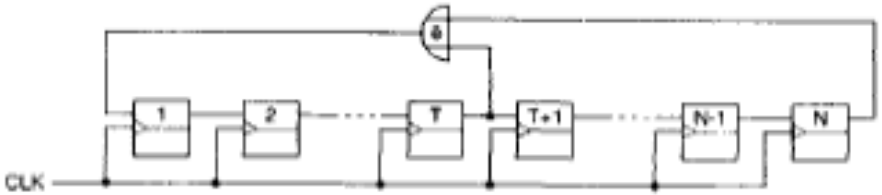
  = Mêmes recettes que pour un bon design analogique…

Compteurs….

- Limitations:
  - Puissance (proportionnelle à la fréquence de comptage).
  - Taille du compteur (nombre de bits).
  - Les compteurs très rapides sont réalisés en **quasi full-custom.**

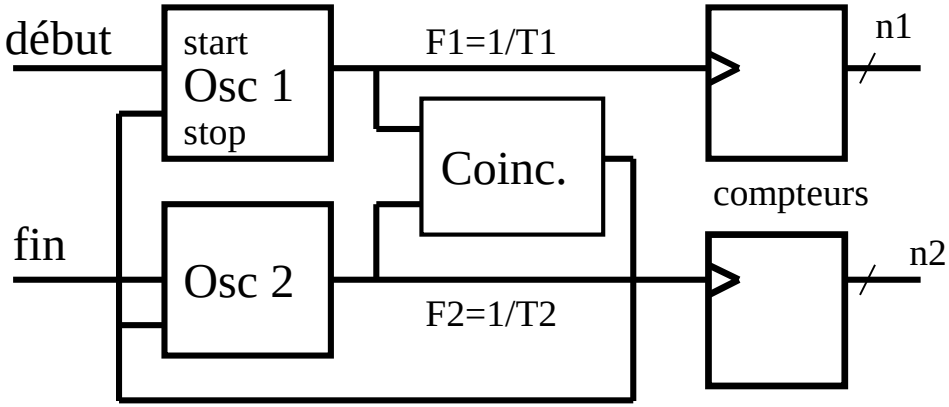
- Pour limiter les transitions => compteurs en **code Gray**
  - Un seul bit change à chaque coup d'horloge
  - Faible consommation, limitent les couplages mais combinatoire interne plus complexe à mettre en œuvre.

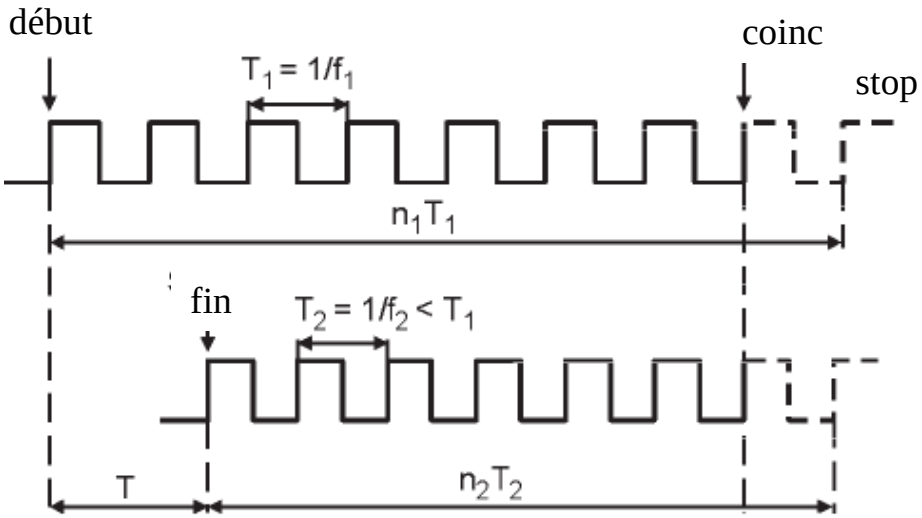
- Autre type de compteur: compteurs basés sur des registres à décalage rebouclés.



  - Avantages : structures synchrones beaucoup plus rapides et plus compactes, faible conso.
  - Inconvénients : nécessitent également un décodage complexe.

Mesures Fines: Méthode du vernier.



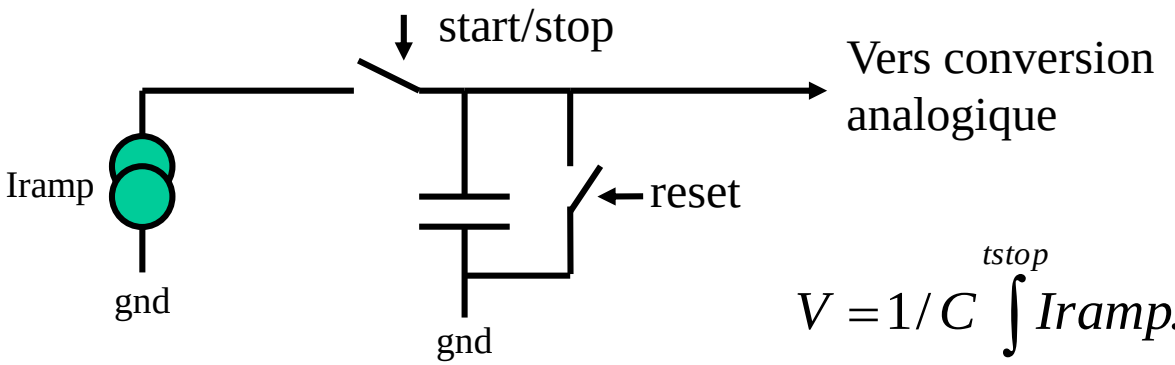


- 2 oscillateurs de fréquences légèrement différentes sont démarrés avec un intervalle de temps T.
- Les nombres de coups d'horloge n1 et n2 nécessaires pour que les deux horloges soient en phase permet de déterminer T avec une résolution T1-T2

  T= (n1-1).T1 - (n2-1).(T2)
- Souvent utilisé dans les FPGAs pour les TDCs start/stop.

Mesure fine par générateur de rampe: le TAC

- Le TAC : Time to Analog Converter.
- Souvent utilisé pour la mesure fine et associé à un compteur pour les poids forts
- Dans sa version la plus simple: intégrateur à capacité commutée



$$V = 1/C \int_{tstart}^{tstop} Iramp.dt$$

- Pas besoin d'horloge, idéal pour les designs purement analogiques
- Non linéarité différentielle naturellement bonne (si l'ADC qui va convertir la tension finale est bon également).
- Peu adapté à un design multicanaux
- Dynamique en temps limitée par le bruit :

$$<\sigma_{vout}>^2 = 1/C^2 \, [\, (A.K.f.t^2) + B.i_n^2 \, .t]$$

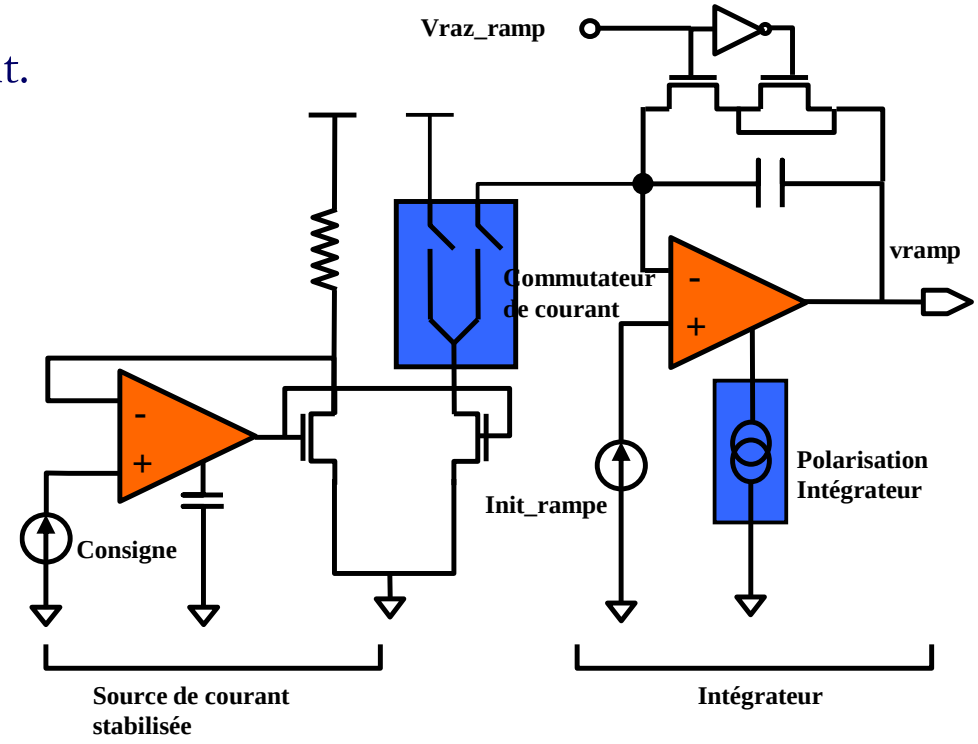
=> **fortes capa d'intégration**.

Exemple de réalisation de TAC

Quelques points critiques du design:

- **linéarité en début de rampe** => switch de courant différentiel.
- **charge injectée** à l'arrêt=> dummy switches.
- **linéarité globale** => intégrateur actif.
- **Variations** avec process et température sur la fonction de transfert

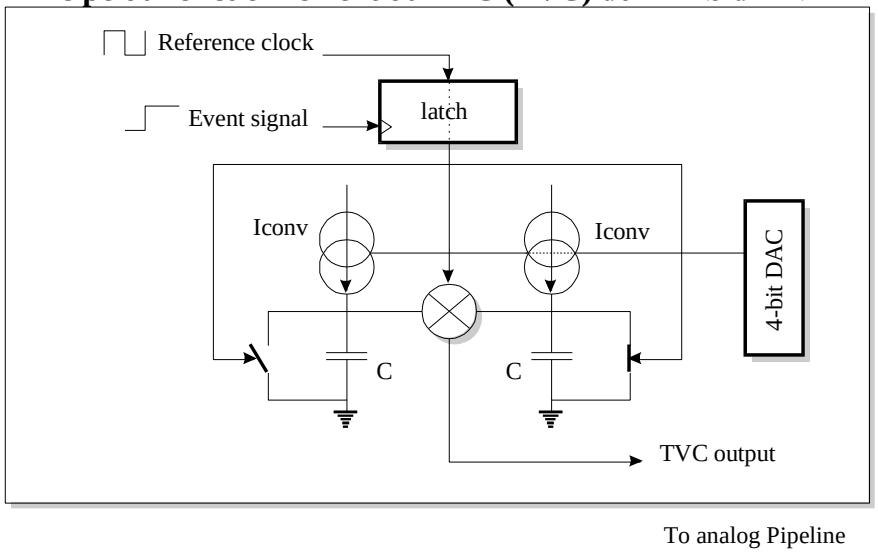
=> calibration ou asservissement.

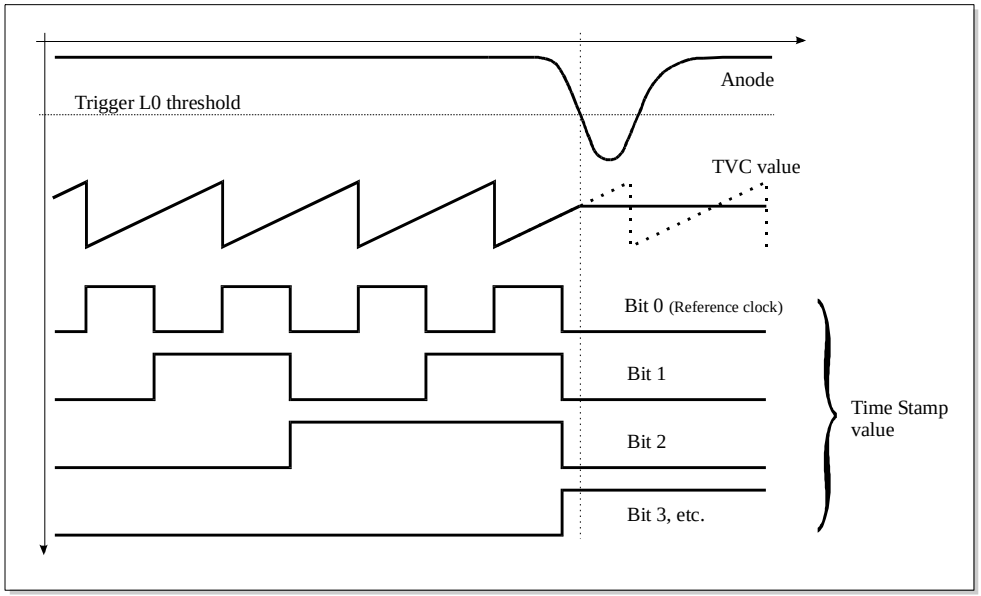


TAC : Compléments.

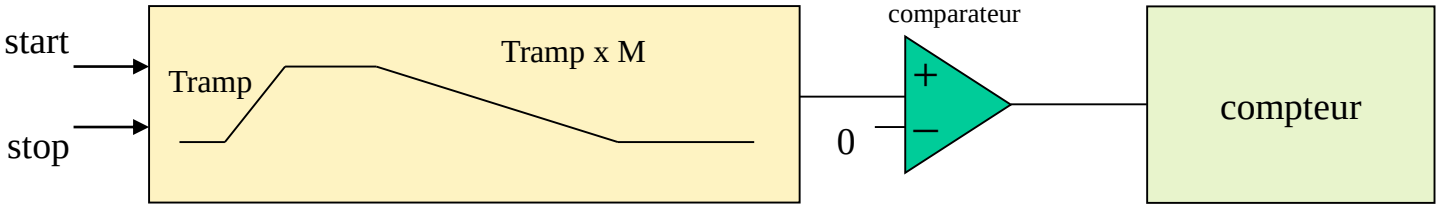
- Un TAC présente du temps mort par principe.
- Celui-ci peut être limité par l'utilisation de deux intégrateurs fonctionnant en permanence + pipeline analogique

Principe du fonctionnement du TAC (TVC) de l'ARS d'ANTARES



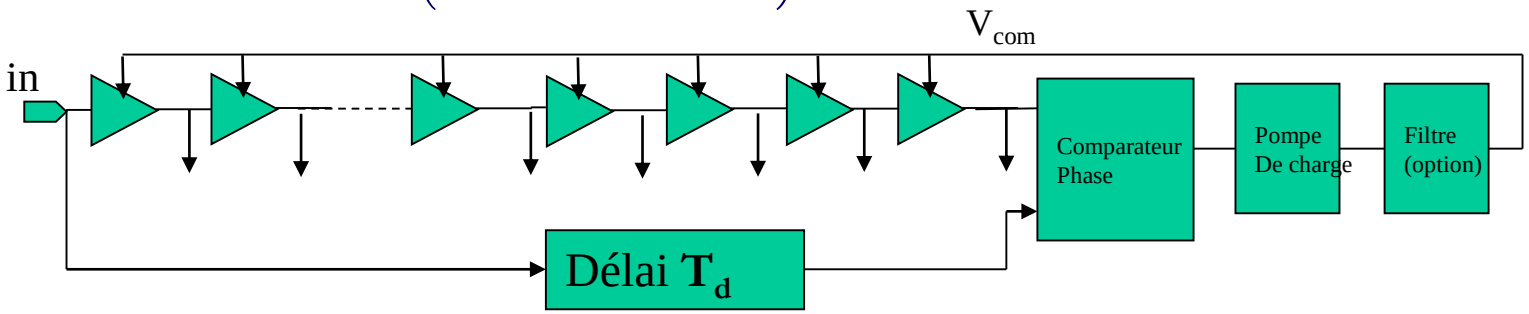


Si ADC de type Wilkinson => expanseur temporel (double rampe)



Types de chaînes de délais : la DLL

- La DLL (Delay Locked Loop) :
  - Une chaîne de retards dont la durée totale est asservie à une durée fixe $\mathbf{T_d}$ => $\mathbf{N.d = T_d}$
  - Usuellement, l'entrée **in** est une horloge et $\mathbf{T_d}$ est sa période
  - C'est la tension analogique $\mathbf{V_{com}}$ qui pilote les retards individuels à travers des inverseurs affamés (starved inverters)



- Le système ne nécessite pas d'inversion de phase.
- Le nombre de délais élémentaires peut-être quelconque.
- Le signal de référence n'est pas nécessairement périodique => peut-être différent de l'horloge (mais attention aux fuites)
- Le système est du premier ordre => filtre après la pompe de charge pas indispensable.
- Le jitter de l'horloge est introduit dans la chaine => horloge très propre

Principe de l'inverseur affamé (1)

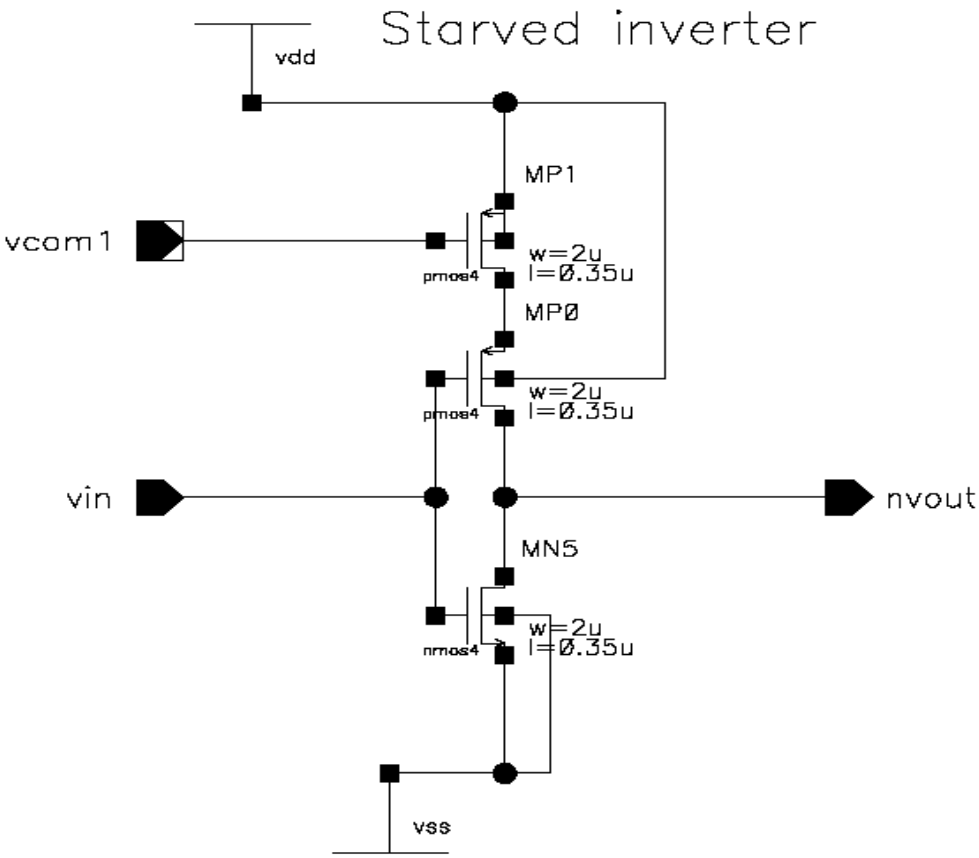
- MP1 limite le courant vers la capa du nœud de sortie lors de la transition montante => au 1er ordre (ultra-simplificateur car MP1 est aussi une résistance en début de commutation et MP0 et MN5 interviennent également).

$$t_p \propto t_r = 2.C_l.Vdd.\frac{L_{MP1}}{W_{MP1}.K_{MP1}.(V_{GS\,MP1} - V_{TH})^2}.$$

- Réalisable uniquement dans les ASICs

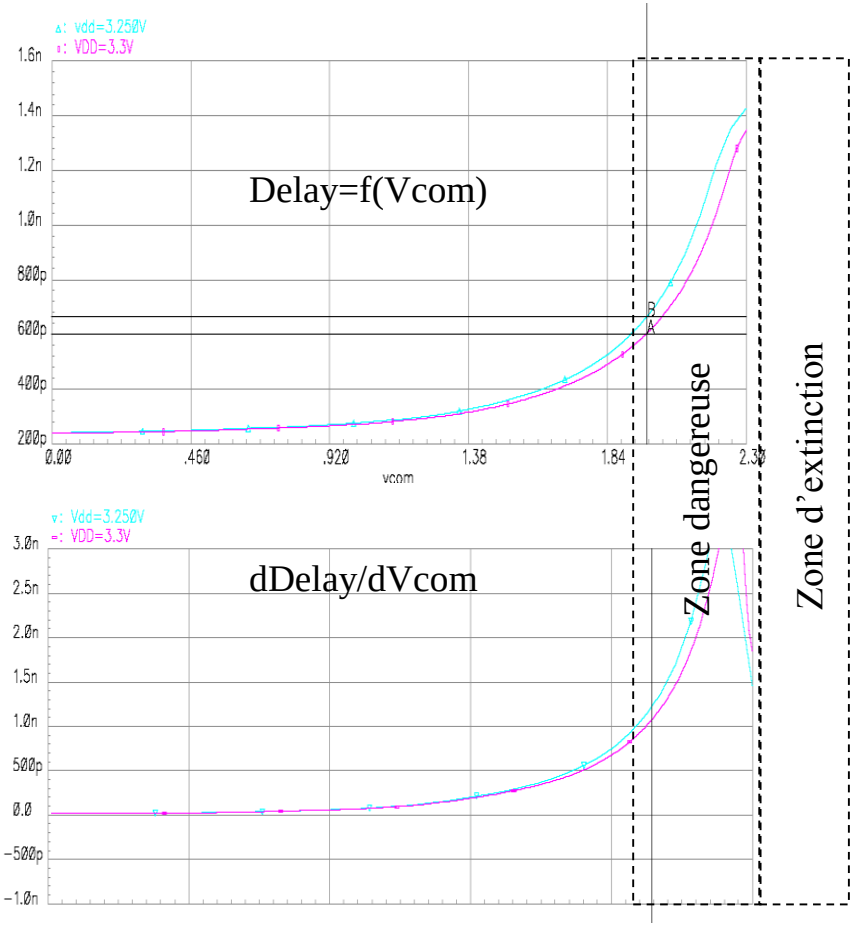
⇒ dans les FPGAs, des chaines de retard sont utilisées pour réaliser des TDCs sur le même principe (en utilisant le signal « carry » dans les additionneurs des cellules logiques) mais sans possibilité d'asservissement

⇒ les retards doivent être calibrés en permanence



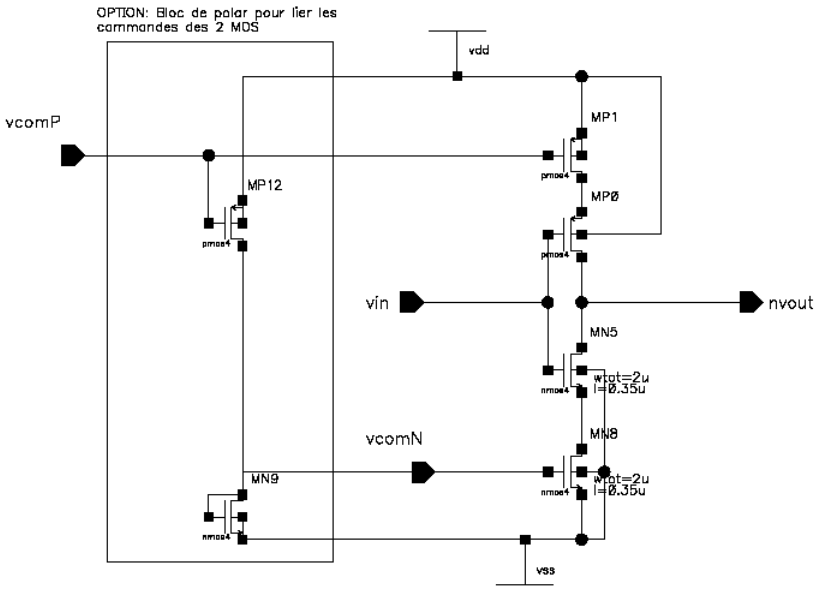
Principe de l'inverseur affamé (2)

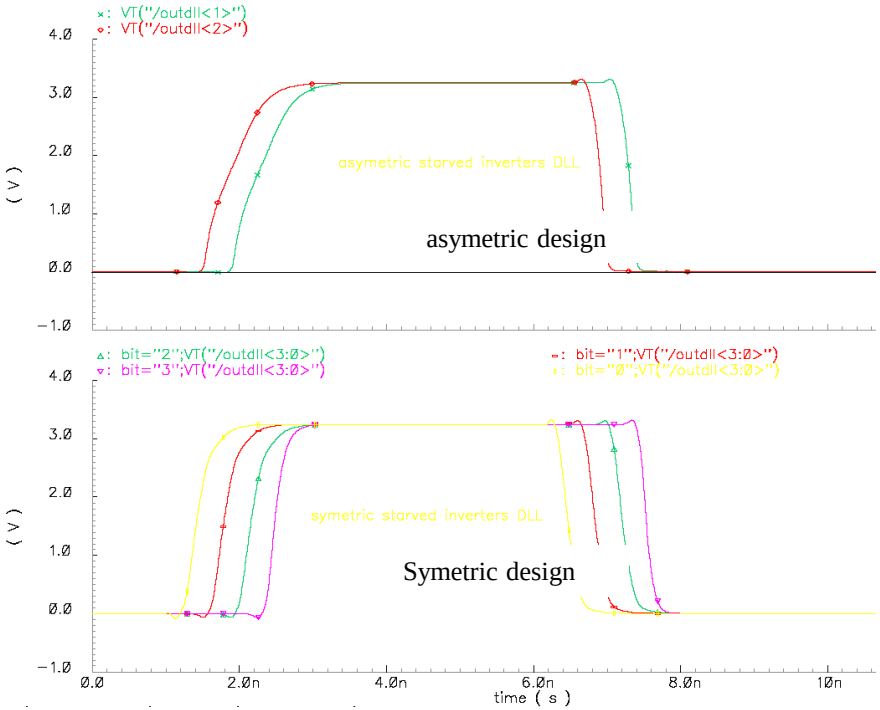
- Plage de réglage très grande (facteur 7).
- Très compact et très rapide.
- Conso indépendante de Vcom.
- Fonction de transfert non linéaire
- Zone à très forte dérivée: dangereuse (jitter), instabilité.
- Zone où le pulse s'éteint=> risque de décrochage.
- Sensibilité à Vdd identique à celle à Vcom
  ⇒ mauvaise réjection (gain) du bruit des alims si Vcom isolé de Vdd
- Délai réalisé uniquement sur la transition montante => dissymétrie de la propagation entre fronts.



Version améliorée de l'inverseur affamé

- Symétrisation : le transistor NMOS peut-être commandé indépendamment par une tension fixe, via le même asservissement que le PMOS, ou via un asservissement spécifique.
- Inconvénient : système + lent.

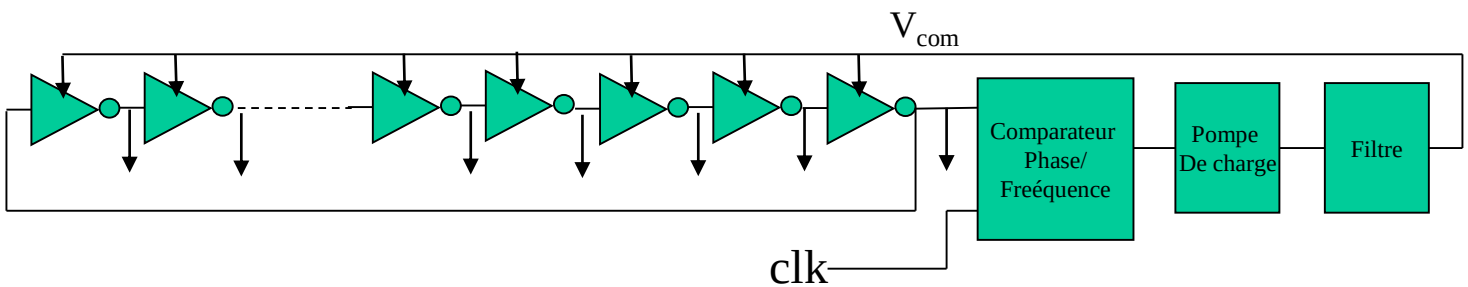




- Avantages:
  - Utilisation de l'inverseur comme délai élémentaire.
  - Permet d'assurer que le pulse ne s'éteint pas (longue DLL).
  - Permet d'utiliser la combinaison inverseur affamé-inverseur standard comme délai élémentaire.
  - Meilleur jitter.

Types de chaînes de délais : la PLL

- La PLL (Phase locked Loop) à oscillateur en anneau :
  - La fréquence de l'oscillateur est asservie => $\mathbf{F_{ck}} = 1/\ 2.N.d$



- Nombre N d'inverseurs nécessairement impair (pour pouvoir faire fonctionner l'oscillateur

=> une sortie sur deux est inversée, ce qui peut introduire des problèmes de dispersion en temps pour l'utilisation des signaux

- Nécessite un comparateur Phase/Fréquence.
- Système au moins du deuxième ordre, nécessite un filtre passe-bas pour assurer sa stabilité .
- Génère son propre jitter (indépendant à haute fréquence de celui de l'horloge)

A few comments about TDCs

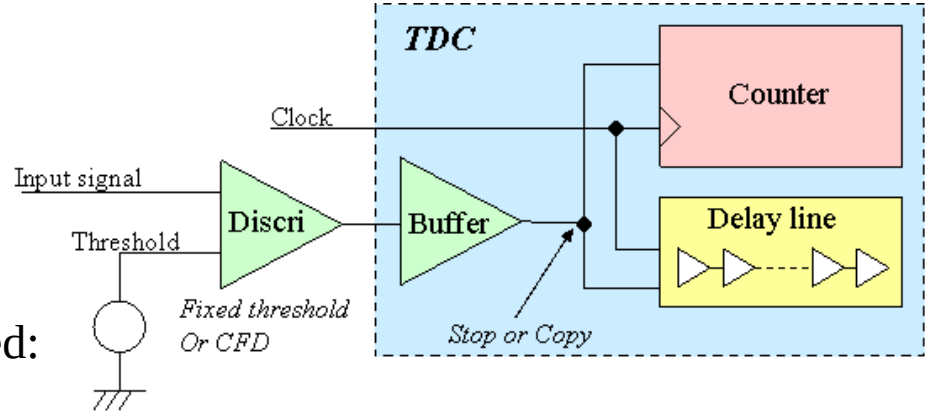
TDCs can be integrated inside ASICs or FPGAs.

- **TDCs** are specifically used for **time measurement**
  - Input counting rate can be very high (>> 40 MHz/ch)
  - Information is concentrated => autonomous channels, reduced dataflow, good for large scale
  - But they do not provide information on waveform, except **TOT**, and they work on **digital signals**

Most **fast TDCs** are using**:**

- **digital counters => coarse timestamp**
- **servo-controlled or continuously-calibrated Delay Line Loops (DLLs) => fine timestamp**

Their resolution is fixed by the DLL step
(or by an interpolation between DLL steps)



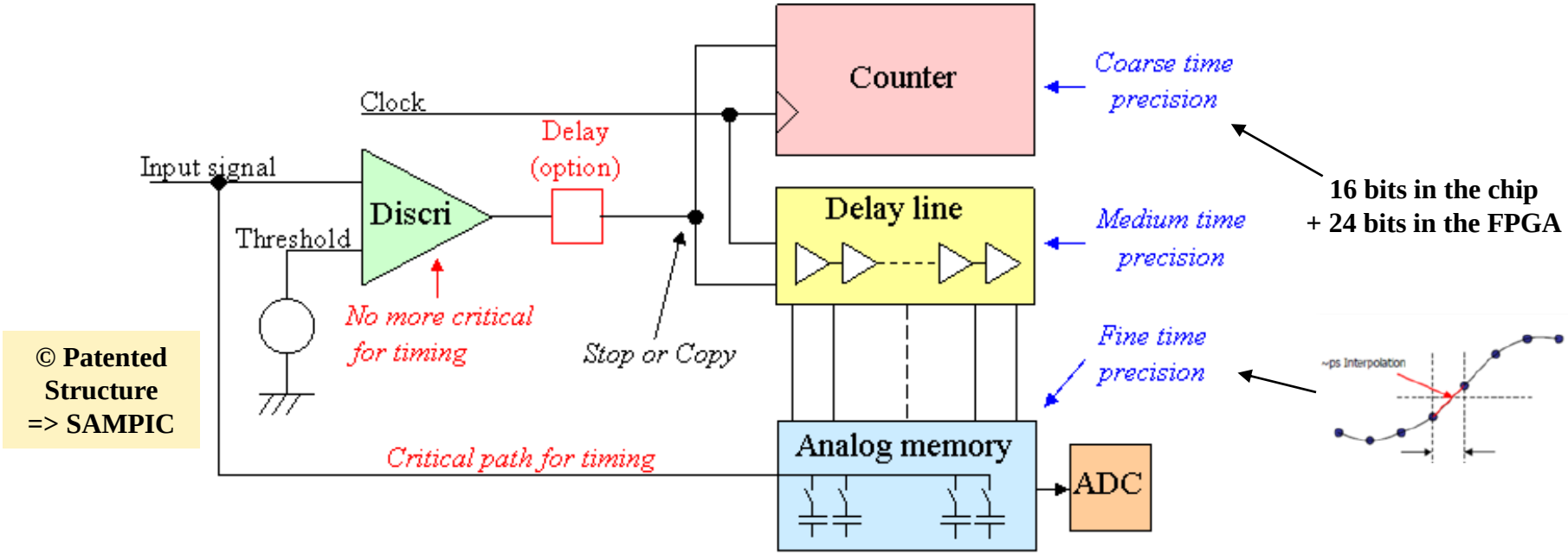
In the timing chain, a **discriminator** is required:

- **critical and often high power**
- Adds **additional jitter** and **residues of time walk** (even with TOT)

Like for ADCs, output dataflow can be a problem at high rates (> Gbits/s /ch)!

The « Waveform TDC » structure

- The **Waveform TDC**: new concept based on a **mix of a TDC and of an analog-memory based Waveform Digitizer**
- Time information is given by association of contributions:
  - **Coarse** = Timestamp Gray Counter (few ns step)
  - **Medium** = DLL locked on the clock to define region of interest (100 ps minimum step)
  - **Fine** = **samples of the waveform** (**interpolation** will give a precision of a few ps rms)
- **Digitized waveform shape and TOT will give access to useful information**
- **Discriminator is used only for triggering, not for timing**

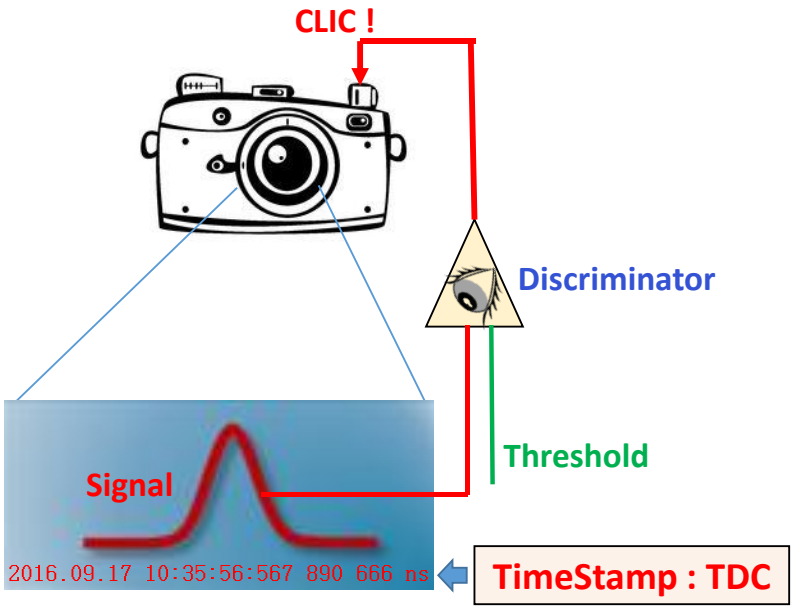


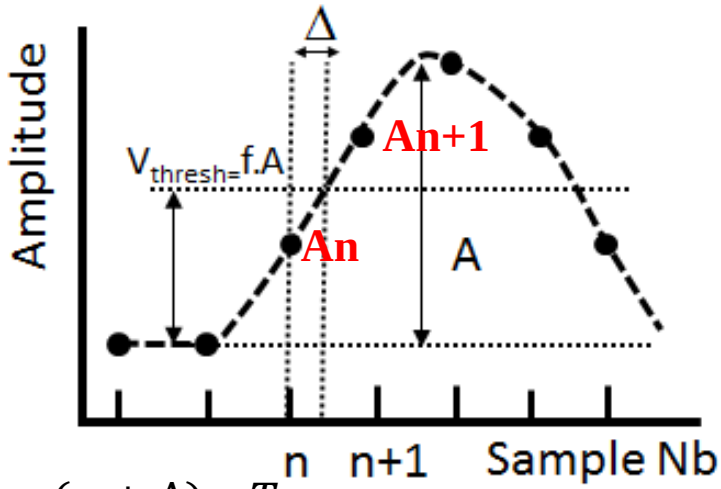
© Patented Structure => SAMPIC

The « Waveform TDC » Concept (WTDC)

WTDC: a TDC which permits taking a picture of the real signal. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of interpolation by a digital algorithm, fine time information will be extracted.





$$t_0 = (n + \Delta) * T_s$$

with $\Delta = \frac{f * A - A_n}{A_{n+1} - A_n}$

- **Advantages:**
  - **Time resolution ~ few ps**
  - **No "time walk" effect**
  - **Possibility to extract other signal features: charge, amplitude…**
  - **Improved dead-time …**
- **But:**
  - **dead-time linked to waveform conversion (200 ns to 1.5µs) and readout doesn't permit counting rates as high as with a classical TDC**

Conclusion

- Discriminators are an important piece of electronics chains
  - They provide the simplest analog to digital conversion of a signal, via its position with respect to a selected threshold
  - They can be simple but also very complex
  - They can be part of ASICs as well as discrete components on boards

- Despite their theoretical simplicity, they can be the source of information for complex trigger systems

- They are also the pillars of the time measurement methods, used there in many different ways

  - I hope you enjoyed following this course… ☺