Technical specifications
AGATA PACE Board

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The present technical specification describes the AGATA preprocessing board (PACE) procurement, assembly, test and delivery. A general overview of the AGATA front-end electronics phase 2 can be found at: https://link.springer.com/content/pdf/10.1140/epja/s10050-023-01045-0.pdf

1. GANIL PRESENTATION

GANIL (« Grand Accélérateur National d'Ions Lourds » "Large National Heavy Ion Accelerator") is today one of the largest research laboratories in the world dedicated to research using ion beams. The fields of research cover applications ranging from radiotherapy, to the physics of the atom and its nucleus, and from condensed matter to astrophysics. In the field of nuclear physics, GANIL has made many discoveries on the structure of atomic nuclei, concerning their thermal and mechanical properties and the so-called "exotic" nuclei that are not found in nature on Earth. GANIL is located in France, in the city of Caen, in Normandy. It is managed jointly, within a Group of Economic Interest (GIE) by the Commissariat for Atomic Energy (CEA/DSM) and by the National Centre for Scientific Research (CNRS/IN2P3). As a national host laboratory, GANIL serves the national, European and international scientific community, by its investigations in fundamental nuclear physics.

2. AGATA CONTEXT

AGATA is a detection unit made of three HPGe detectors in semi-coaxial configuration sharing a common cryostat. Each crystal has a pyramid shape: the front-end features a section shaped like an irregular hexagon but the opposite (rear) end has still a cylindrical shape. The crystals have three slightly different shapes. Their external surface is electrically segmented into 36 parts. Each crystal is mounted in a vacuum-tight capsule. The signal from each detectors is collected in an analogue front-end electronics which sampled into a dedicated module called DIGOPT12. The numerical signal is then transmitted to a processing board (PACE) which provides trigger decision at the first level, calculates the energy deposited by the photons interacting into the crystal, time-stamps the event using the GTS or SMART protocol developed by GANIL, event-builds and readout the collected data to a HPC computer farm. The AGATA collaboration is updating its front-end electronics as part of the AGATA phase 2 MoU project endorsed by a large European collaboration including France with the CEA and CNRS institute. The upgrade of the AGATA front electronics was evaluated by an international review and a dedicated project review at CNRS/IN2P3.

3. THE PACE BOARD DESCRIPTION.

3.1 Bandwidth and FPGA capabilities

The intrinsic characteristic of the digitalized data for AGATA, at the nominal 100Msps sampling rate, requires a 2Gbps readout link, with a total of 76Gbps for the 38 pre-amplifier channels per segmented encapsulated detector.

For the transceivers populating the modern FPGA's, 2Gbps is underrated and, furthermore, there is a strong dependency of the FPGA cost with the number of transceivers. The mid-range FPGAs with 10-20 transceivers has sufficient resources to perform the tasks of the AGATA pre-processing and are one of the characteristic of the PACE board.
On the small-size SOM devices, the number of high speed channels is also critical due to the limited number of connectors available in the mezzanine board. These two reasons are sufficient to consider a

solution to approach the real total bandwidth of this mid-range FPGAs with an AGATA digitized aggregated bandwidth as requested in PACE.

The concept selected to face it is by using a Time Domain Multiplexing link aggregation gearbox, with a 4 to 1 rate. The implementation relies on the commercial Texas Instrument TLK10000 devices. These devices are designed to work in pairs to aggregate data in one of them, send the data through a higher speed network and dis-aggregate data in the receiving second device. Our development adapted this concept to receive the high-speed link in an FPGA with an associated firmware that will recover data, splitting it on the original 4 links. On the AGATA electronics in particular, the JESD204 protocol is used, so this is the protocol use for the development of PACE.

The data arriving from each of the four Digi-Opt12 digitiser boards is sent through a Samtec Firefly 12-line connector that allows flexibility on selecting optical or copper cables. The data a un-multiplexed by the IDM IP-bloc in the firmware to be implemented into PACE.

3.2 PACE FUNCTIONALITIES

The PACE-CAP motherboard takes the IDM in the receiver section and in addition incorporates all functionalities needed for the AGATA Phase 2 electronics. In the board, the aggregation system is implemented with the TLK10002 and the copper firefly are selected to connect to Digi-Opt12. In order to use Firefly cables with the Digi-Opt12 boards it is necessary to use a transceiver-size adaptor called COA to interface the Digi-Opt12 optical socket to Samtec firefly connector.

After passing through the IDM section, the 10 aggregated input data lines at 10Gbps lines are connected to the SOM board Trenz TE0808-05-BBE21-A that houses a Zynq Ultrascale+ XCZU15EG-1FFVC900E.

Correspondingly, 10 GTH transceivers of the FPGA de-serialise the data and the firmware recovers the 38 JESD204 channels, corresponding to the segment and core ADC data, decoded and ready to be processed.

One important task of the PACE pre-processing board is the generation of the local trigger (level 0 trigger), that contributes to the global trigger, as well as the full system synchronisation. This task is taken by the GTS part of the hardware and firmware developed by GANIL and implemented into PACE. The GTS tree has an alignment protocol to ensure that the system clock is distributed synchronously to all the ADCs and pre-processing systems of the array.

The PACE board is connected to the GTS tree through an SFP optical transceiver, where the global clock is received, the triggered events are sent and global trigger replies received. The link provides a common clock to all the system that is cleaned and fine-tuned during the alignment protocol in the PACE Clock & GTS hardware section. This section of the board also provides 3 independent PLL systems, one for the GTS, one for the SOM and one for the aggregator system.

Following the pre-processing on the SOM FPGA, all the events validated by the GTS second level trigger, are sent for readout via the Ethernet STARE board, plugged into PACE-CAP as a mezzanine though an FMC Vita 57.1 four 10Gbps links using the Aurora protocol.

While the slow control commands are passed to PACE-CAP via an IPbus firmware implemented in STARE, the PACE board incorporates two small FPGA Lattice Machxo3 in order to perform the local slow control, monitor and power the rest of the system. One of the small FPGAs is for the slow control and has access to all the hardware bus lines, the other one is for power supply management and start-up of all the system, that is managed autonomously. The latter includes the control of the power supply unit board, in such a way that the power of all the system can be remotely controlled. These two FPGAs have a power supply independent of the rest of the system.

In addition, the board incorporates two Ethernet connections, one for the FPGA fabric, devoted to the IPbus control in case the STARE board is not present. The second one is for the multi-processor system

(MOSOC) present in the Zynq Ultrascale+ FPGA and is used for remote controlling the MPSOC and to perform the GTS alignment software procedure. Furthermore, there is an SD socket for the MPSOC programming, a USB-C for debugging purposes and the JTAG/UART socket.

The embedded pre-processing firmware has three main goals: 1) energy determination and trace construction, 2) local trigger generation and global trigger management and 3) data formatting and readout. All the channels are processed in parallel by a process module called Datapath, that is identical whether it corresponds to a core channel or a segment channel and is synchronous with the 100MHz system clock from the GTS. The data path employs a digital Constant Fraction Discriminator to identify if a signal exceeds the trigger threshold.

Simultaneously, it processes the Moving Window Deconvolution (MWD) trapezoidal filter, which has a maximum length of 20 μs. In the event of a triggering signal, a trigger request is sent to the rest of the PACE system involved and to the GTS, the energy is calculated from the MWD trapezoidal filter and with a linear interpolation the time is extracted using the crossing point of the dCFD within the 10ns width of the samples.

The firmware developed by the AGATA collaboration which is embedded into the PACE board has four data store modules, i.e.:

- Event module: includes a complex memory that stores all the information each time a trigger request is sent from the processing module selected for triggering, normally from the core. It also communicates with the GTS system via the GTS leaf module and, in case the event is validated, the corresponding memory contents are sent to the readout engine in charge. In case of rejection or timeout the memory contents are deleted and the slot is free for a new event. In order to preserve the data during the request-validation/rejection/time-out cycle of the GTS, there is an array of such memories that stores up to eight events. The data sent to the readout engine is packed in standard AGATA Data Frame format (ADF) with 100 samples per channel and event. It is possible to extend the traces sending 200 samples per channel and event. On these packages we also find the calculated energy from the trapezoidal filter of all the channels, the, timestamp, the fine value of event time from the linear interpolator on the core and the type of event sent by the packager

- Long traces module: Long traces are segments of the data stream used for diagnostic or response function calibration. There are two type of long traces, the standard up to 4000 samples (4μs) and the very long trace stored in the DDR memory. The first one is constantly stored for all 38 channels and can be sent, within a single ADF packet, upon request, via the slow control, to the readout engines. The second one is storing constantly the previously selected channels into DDR memory and can be sent to the readout engine in multiple packet protocol.

- Spectra module: its task is accumulating the energy spectra of every channel since the last reset, called by the user via the slow control. The readout of any spectra, in a single ADF packet, can be requested via the slow control.

- The monitor module: This module stores a full memory of the internal selected data. It can be sent to the readout engine in an extended multiple packet protocol.

In order to perform the readout, four readout engines have been created in the firmware by the AGATA collaboration, each one is connected, via one of the 10Gbps Aurora links, to STARE (developed by CNRS/IJClab), that is in charge of sending the data packages via Ethernet. These readout engines can select which of the memory blocks are reading and combine the packets into the readout data flow. As mentioned before, all packages are formatted in ADF or multiple package ADF based. It includes ADF IDLE frame, Error frame and System Off frame that are sent automatically depending on configuration and status of the system.

In order to interact with the GTS tree, validate the local triggered events and recover the system clock, there is a GTS section in the firmware. This section includes a GTS leaf that communicates with the GTS tree and with the firmware event memory section and provides the global validation and rejections, aligns the global timestamp, monitors the counting rates and implements the \lq\lq backpressure\rq\rq control. Backpressure refers to a mechanism used already in phase 0 and 1 which inhibits temporarily the trigger as soon as, for any detector, the data acquisition or data processing is unable, to consume the data from the readout hardware.

The last element of the firmware is the slow control, that is done through the IPbus implemented in STARE via a slow speed differential connection in the FMC. There is also the capability to control PACE in standalone mode by IPbus. There is an IP block on every relevant firmware module with the required set of registers. There exists a specific IPbus module that translates the communication with the slow control FPGA outside to control the Hardware.

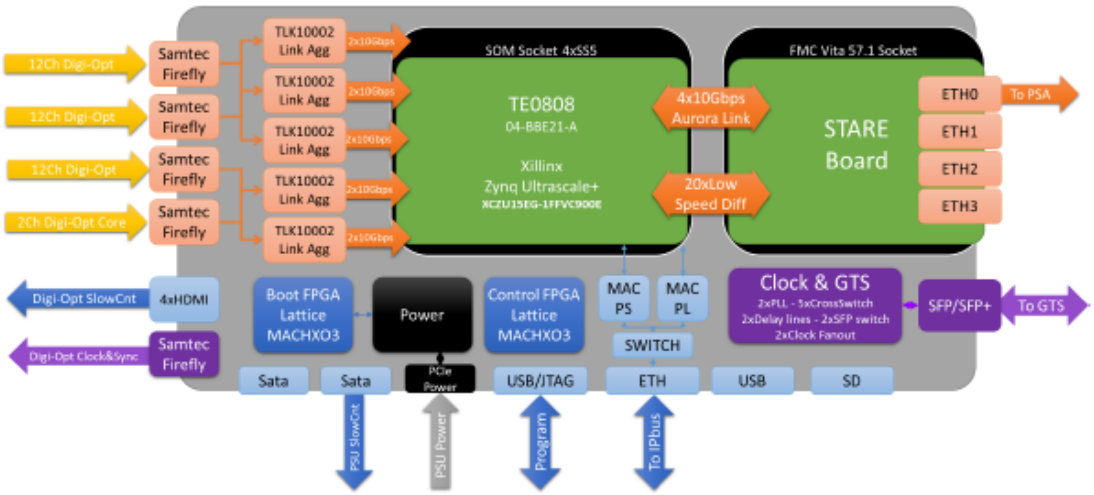

Fig1. Bloc diagram of the PACE functionalities

All these functions (powerful SoM to embedded the developed firmware, I/O links, control and command, clock and trigger interface) must be embedded in a specific motherboard that meets high integration, power consumption and performance requirements. This acquisition motherboard was designed by the University of Valencia (Spain). The construction, routing and cabling plan validated by the AGATA collaboration is referenced: PACE-CAP-v100-t58. The blue print belongs to the AGATA collaboration and provided to the contractor for assembly.

3.3 PACE DESCRIPTION

PCB board description

The PCB board consisted of 12 layers with a 5 with a FR4 core and 2 blocks prepreg+core+prepreg layers based on Rogers RO4003 and RO4450B materials. The stackup and layer definitions can be seen in the following Figure 2.

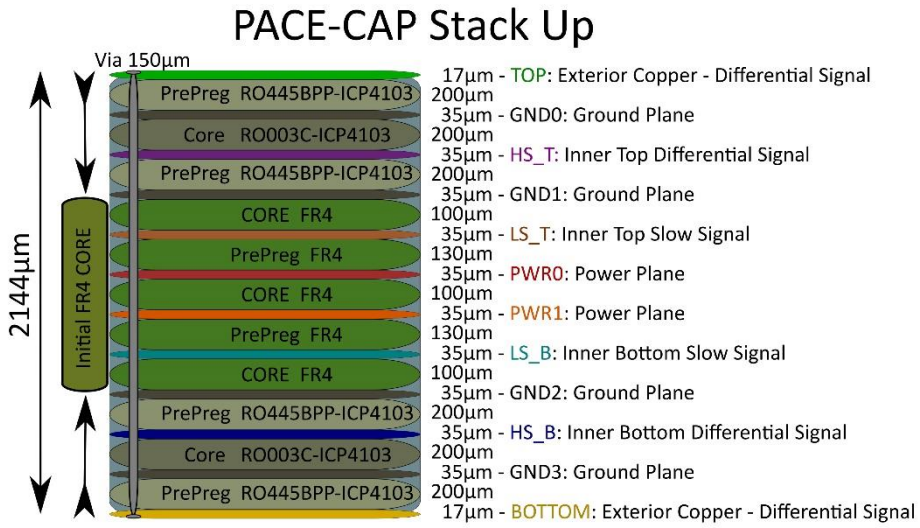

Figure 2: PACE Stack Up and layer distribution

The PCB characteristics are summarized in the following table:

- Size: 294mm x 120mm (accuracy 0.1, dimensions without panel)
- Thickness: 2.144mm
- Layers: 12
- Copper thickness external: 17u
- Copper thickness internal: 32u
- Core PCB material: 6xFR4
- 3 layers prepregg + 3 layers core material: RO4450Bpp/RO4003C
- via: through 0.15 um plated
- differential line impedance 100 Ohm
  - internal: 0.100u width 0.145u gap
  - external: 0.202u width 0.120u gap
- normal line width 0.1u
- power line width 0.3u
- Finish: Au (ENIG)
- paneling: 4 side for mounting purposes

1. Board description

The PACE board (see Figure 3) is the main motherboard within the AGATA pre-processing system. This board handles pre-processing tasks (Energy and Time determination, buffering of the sampled segment and core signals, etc…) and manages the trigger, connecting to the Global Trigger and Synchronization (GTS tree). Furthermore, the motherboard is responsible for the slow control functionality and the distribution of the clock system.

The input data for the PACE board comes from the digitizer boards, referred to as Digi- Opt12, are responsible of the sampling of the incoming differential signals from the detector preamplifiers transferred by the the MDR cable.

Once the pre-processing and triggering process is completed in PACE, the STARE board, connected to the PACE FMC VITA 57.1 connector, receives the processed data from the and transmits it to the workstations using 10Gb Ethernet protocol links. Additionally, STARE facilitates the communication between the PACE Monitoring system and the network, as well as managing all the necessary communications and protocols associated with the Ethernet connection.

Figure 3: PACE board production version

The different sections with the PACE motherboard functionalities are indicated in Figure 4

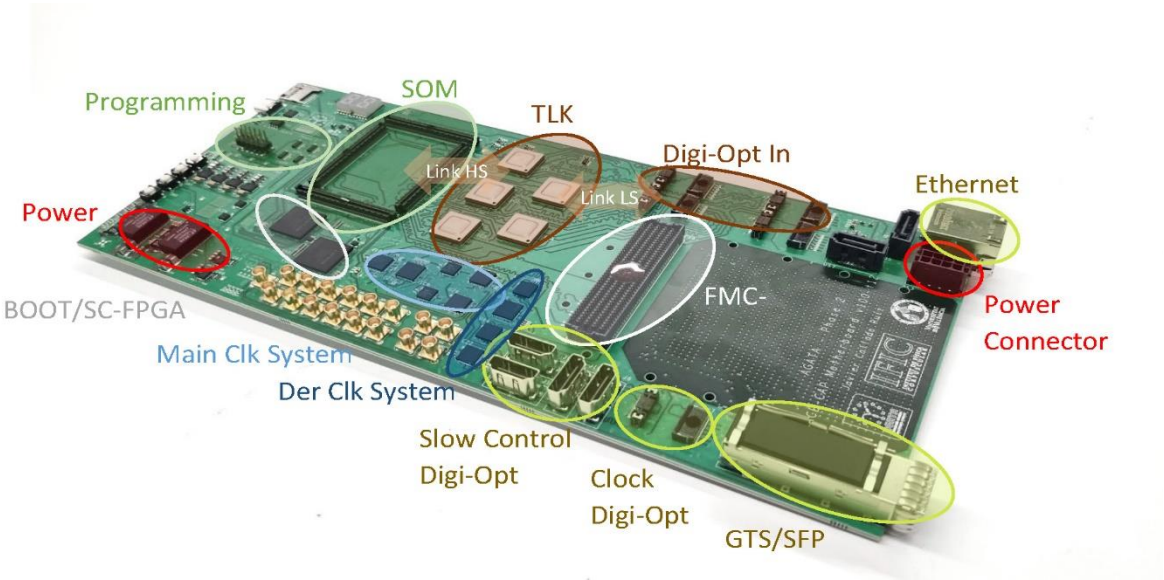

Figure 4 Main functional sections in the PACE motherboard

DigiOpt12 Input

The data from the digitizer is received through Samtec Firefly connectors, which can be mated with both copper and optical cables, for the PACE system, the copper version of the cable has been selected as the primary ADC data input connection. The Firefly connectors consist of two parts: UEC5 and UCC8. The UEC5 is the lower pitch connector with two lines, A and B, each containing 20 pins. These pins connect the GND and 12 differential lines. The differential lines are CML and terminated with a 100 Ohm impedance. The second part, UCC8, is a larger pin connector with 10 terminations. There is a critical requirement regarding the placement of these components on the board since the Firefly copper cabling need to reach the DigiOpt12 boards place closely above the frontal part of the PACE motherboard

The TLK Aggregator

Following the IDM concept, the link aggregator has been build with the TLK10002 integrated circuits from Texas Instruments. The TLK10002 is an Ethernet link aggregator capable of mergingup to four lines into one with four times the bitrate. The maximum output bitrate is 10Gbps. For PACE, the typical configuration is to merge four 2Gbps lines into one 8Gbps line. The integrated circuit can decrypt 8b/10b data and re-encrypt it at high speeds. Each TLK10002 can have up to two output high-speed channels coming from eight lower speed inputs. To merge the 38 optic 2Gbps signals into 10 FMC 8Gbps signals, five TLK10002 are necessary.
The power consumption for this device is considerable due to the highspeed transceivers. Each TLK10002 consumes a maximum of 600mA for each of the four core 1V input lines, along with a few mA for the 1V8 line which powers the I/O and PLL. When the device is fully utilized, the total power consumption reaches 2.5W. The power supply design can support up to four 5A@1V power lines as the device needs four different 1V power supplies. Additionally, the power supply design provides a 1A@1V8. Both power supplies should be designed to supply four times the necessary power. This power capability is designed for power distribution. However, the Link aggregator doesn't operate at its maximum capacity and a lot of this power is required only during startup. The normal operating power consumption is 3A at 1V in total, equivalent to only 3W for the five integrated circuits. The optimal reference clock for Link Aggregators is 200MHz, and it must be derived from the main 100MHz clock of the system.

In Figure 5 are described the interconnections between the Firefly connector receiving the signal of the Digi-Opt12 boards, the inputs of the TLK10002 aggregator and the SOM connector.

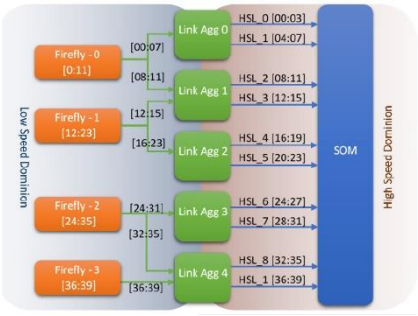

Figure 5 Connection scheme between the Firefly input connectors, the TLK10002 and the SoM inputs

The Boot and Slow Control FPGA
The PACE motherboard houses two compact, low-power and cost-effective Lattice MACHXO3 LCMXO3LF-2100E-6MG121IND FPGA/CPLD units. These devices offer 2100 logic cells, 100 IO connections, one I2C module, one SPI module, one PLL, and 64 Kbits of distributed RAM. They have selfprogramming memory, but the design also includes two external memory modules for programming purposes.
One of the FPGAs is dedicated to autonomous boot and programming (BOOT-FPGA), and the other to autonomous slow control and connection switching (SC-FPGA). The I2C on the BOOTFPGA is configured as a master, while the I2C on the SC-FPGA is configured as a slave. An I2C selector tree, is used to switch between the primary I2C from the SOM-FPGA and the master I2C from the BOOT-FPGA. The BOOTFPGA controls the direction of this switch; during the boot operation, the I2C master from this FPGA is selected, but after booting, the BOOT-FPGA sets the switch to the SOM-FPGA I2C master.

The slow control is performed through the MDIO protocol by the SC-FPGA, in addition to several I/Os for control and address selection. All boot procedures are carried out by the BOOT-FPGA. The system slow control is done from the SC FPGA, but for the programming of the integrated components based on I2C bus there is a specific network to control all the devices. Also, as the SC FPGA is a slave I2C device it can be controlled through several devices. There is a bus distribution system to select the desired device to control. All the slow control operations in the system are carried out through a single I2C bus pair, with the SC-FPGA acting as the slave device that grants access to the system. However, the master device for this I2C bus can originate from three different sources. The default master is the FPGA matrix, which is controlled by IPbus. The second master can come from the PS (Processing

System) and can be controlled through remote SSH/EPICS system debugging. The last master is the BOOT FPGA, which takes control of the system during startup and also provides additional debug control through UART/USB. To enable these three connections, two NXP PCA9541 ICs are used. The first IC selects between the FPGA matrix or the PS as the master. The second IC selects between the previously mentioned signal and the BOOT FPGA. The second bus determines whether the system is in the boot status or the normal status.

The System on Module (SoM) connection

The PACE FPGA is the System on Module (SOM) TE0808-05-BBE21-A from Trenz Electronics, equipped with the Xilinx Zynq Ultrascale+ XCZU15EG- 1FFVC900E chipset. This chipset comprises a FPGA, a quad-core ARM-A53 processor, a GPU, and a dual-core ARM-R5 microcontroller,all encapsulated within the same integrated circuit. The SOM board provides connections for 16 FPGA GTH transceivers, arranged in four banks of four: 228, 229, 230, and 128. The banks 228 and 229 on the SOM board are fully allocated for ADC data from the link aggregator. Meanwhile, Bank 230 is split, with half dedicated to ADC data and the other half to GTS communication. The 128 Bank is fully allocated to the four AURORA 10 Gbps links with the STARE FMC board.

Main clock and GTS Synchronization system

The Main Clock serves as a reference for the entire PACE system, establishing a synchronized 100 MHz clock throughout the AGATA system via the GTS tree. However, this clock can either be generated locally for standalone operation, provided from an external source or from a transceiver recovered clock and PLL cleaned (GTS). In standalone mode, the clock source can be selected from the following options: a local oscillator, SOM FPGA output, an external MCX connector, or the Derived Clock system. In the standard case, with GTS synchronization, the signal is received from the transceiver recovered clock (SOM FPGA output), cleaned by the PLL, and then synchronized with the rest of the GTS tree clocks via two controlled delays. The PLL, in both schemes, is set as a jitter cleaner, with all the outputs remaining common and at 100 MHz. The main 100MHz GTS synchronized clock is distributed to: the four Digi-Opt12 modules as a reference clock, the SOM FPGA as feedback, the derived clock system, the GTS transceivers reference clock, and the SOM PLL clock.

Derived Clock system

The derived clock system generates all clock references for clocks different from 100MHz.
There are two Derived Clocks in the system. The first one generates signals for the SOM FPGA through the SOM Phase-Locked Loop (PLL). The second one serves the remaining devices and is based on a low jitter PLL and two crosspoint switches that allow for the selection of input and each output. The outputs served by this second derived clock include the two derived FMC (FPGA Mezzanine Card) signals, the reference clock for the Link Aggregators, and a secondary reference for the Aurora FMC interconnection.

Clock for the Digi-Opt12 Digitizer boards

The primary reference 100MHz clock for Digi-Opt12 is served from the MC-A fan-out. This clock is sent to a backplane installed on the Digi-Opt12 via a copper cable. In order to guarantee low jitter and delay consistency among different Digi-Opt12 modules, the connection is based on a Samtec Firefly copper cable, which utilizes Twinax cable technology. The backplane is specifically designed to ensure controlled impedance and jitter.

The FMC Vita 57.1 STARE Connection

The FMC selected is the Samtec's 400-pin ASP-134486-01. The STARE side is designed with a 134488-01 or equivalent, which is its counter-side part. These FMC connectors are fully compliant with the VITA57.1 FMC standard, which is extensively used in Xilinx-based Mezzanine designs. The primary function of this connector will be to facilitate four 10Gpbs capable connections, some slow control connections, and power supply. Samtec's FMC provides 10 full-duplex 10Gbps differential lines and 82 standard speed differential lines. It also reserves lines for JTAG and I2C. Power supply through the FMC is handled by four 3.3V lines capable of up to 3A, two 12V lines up to 1A, and four Vadj lines at 1.8V up to 4A.

The data connection between PACE and STARE is established via 4x 10Gbps differential lines using the AURORA 64 Protocol, through DP0-3 Tx (M2C) and Rx (C2M) (refer to Annex 2). There are also 20 differential lines from LA00 to LA19, they are mainly used for slow control transmission from STARE to PACE. The system's clocks are supplied by the PACE motherboard, derived from the GTS system, PACE requires two clocks: the 156.25 MHz reference clock for the AURORA 64 signals from PACE to STARE, and the 100 MHz reference clock for the system. These clocks are supplied by CLK2 BIDIR and CLK3 BIDIR, respectively. As they are permanently C2M signals, CLK DIR is pulled up. The feedback clock from STARE is received through CLK0 M2C as a 156.25 MHz reference clock.
The FMC Vita 57.1 Standard provides a maximum of 2A at 12V, 4A at 3.3V, and 4A at Vadj (usually set to 1.8V, but configurable via the EEPROM). However, for design reasons associated with PACE-PSU, the CAP will not supply 12V. Note that the production version of AGATA's STARE module does not use the 12V supply, with the exception of the version equipped with a fan. Instead, the 12V supply will be provided by the CAP main board's 5V supply. The 3.3V supply is generated through a dedicated DC-DC converter, which features an enable signal.

Programming section

The entire system contains four FPGA devices that require programming. These devices are connected in a JTAG chain, as illustrated in Figure 6. The main JTAG chain is established using the TE0790-02 XMOD FTDI JTAG Adapter board. This board is specifically used for programming the FPGAs and can be removed in a production setting. It provides a USB2 interface with one channel dedicated to JTAG and the other channel serving as a serial interface. The adapter board is properly configured for Xilinx debugging and programming, as well as for the SC-FPGA and BOOTFPGA. The design of the adapter board is based on TEBF0808. There are also two secondary JTAG chains for programming different devices. The first chain is dedicated to the lattice devices, while the second chain is intended for the Xilinx devices. A switch allows for the selection of the desired programming route. This switch can be accessed physically on the backplane or remotely via the SOM FPGA.

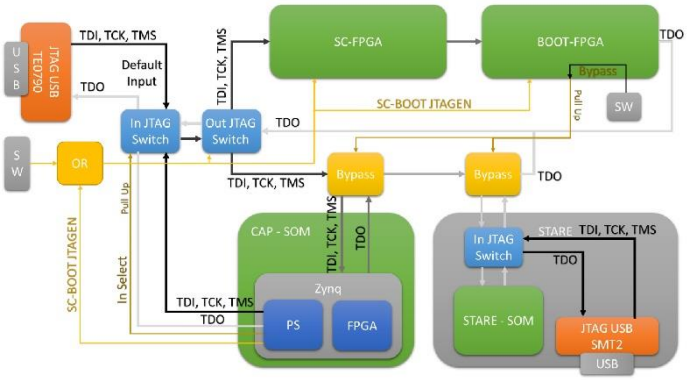

Figure 6: JTAG Chain Scheme

The Digi-Opt12 Control

The connection to Digi-Opt12 slow control lines is done through mini HDMI (Type C) cables. Each board requires of the two I2C lines, an extra for SPI (Shares two lines with I2C) and the Reset board signal. This signals are connected to the SC FPGA.

Processor and FPGA Ethernet

There are two Eth 1Gb PHY installed on the board along with one double 1Gb Ethernet connector. The first PHY and connector (Upper) and are dedicated to SOM FPGA matrix and its dedicated to IPbus control. The second (Lower) are reserved for the processor system in the SOM FPGA and is dedicated to Linux control and EPICs. Both PHYs are a Marvel 88E1512-A0-2I000 IC.

Processor USB

The PACE has a USB-C port located on the front panel. This USB-C connection is controlled by the SOM FPGA processor and is specifically implemented for debuging purposes.

Programming double SD bridge
The PACE motherboard has two SD card readers for automatic system boot up. It includes the load of the firmware, the Linux system and software. One of the SD cards is the main firmware source and the second is a fast backup if the system fails. The SD card requires a bridge from 1.8V to 3.3V to communicate with the SOM board, the selected device is TXS02612RTWR. The device should be inserted in each line connected to the SD.

3.4 Factory Functional Test

The objective of the full test is to ensure the electrical and functional test before the product departs from the manufacturing company, the key features are:

- Conductivity test.
- Preparation.
- Electrical test: short circuits, power, voltages and critical test points.
- Functional test.

Conductivity test: Before the programming of the FPGA, a conductivity test is done to ensure no shortcuts are on the board. The files provided with the connectivity will determine the critical points to test. The primary important are the 12 Voltages+ ground between them. The secondary critical points are SOM board power and the TLK10002 (IC1-5) power.

Preparation for power up: The first step is to prepare the board to work in the test mode.

1. Connection to Power Supply:
The test bench provides a PACEPSU, connect the device using the PCI-E cable JX from the power supply to the JX port of thePACE. The XLR connector of the PACE-PSU should be supplied with 48V@2A via the PACE-PSUTestCable. In case there is no PACE-PSU available, the test is still possible, use the PCI-E-PT test cable on the JX. Ensure a stable power supply by providing:

   – 5V with a minimum of 17A to the red cable.
   – 3.3V with a minimum of 1A to the green cable.
   – Ground the system using the black cable.

2. Switch Configuration:
To ensure the board operates correctly with the test bench and in functional mode, configure the board’s switches as follows: SW0(00000000), SW1(00000000), SW2(00000000), SW3(00000000), SW4(00000000).

3. Lattice FPGA Programming:

Set the SWX switch to ”0000” for programming the Lattice FPGA devices, Machxo3. Then Connect the lattice programming board to socket J12. Using a computer with the Lattice Diamond programmer software installed, connect a USB mini-A cable to the board. Upon connection, the programmer will display a specific image. For programming, set both devices to ”NVCM Erase,Program,Verify”.

For the first device, select ”boot fm.jed”, and for the second device, select ”sc fm jed”. This will program the boot FPGA and slow control FPGA, respectively. Once programmed, the power up must show 0F on the 7 segments of the board and basic functional LEDs must be on. The 12 primary Voltages and the SOM,IC1-5 voltages must be measured to ensure is working on stable conditions. The I2C port and MDIO test ports are ready to perform a ping scan to ensure working on every devices.

The electrical test: The electrical test must show the following values in the inspection points:

- PSU 5V - 5V (Coord: 23.95, 37.4 TOP/BOTTOM)
- PSU 3V3 - 3.3V (Coord: 8.7 , 4.6 TOP/BOTTOM)
- P3V3 - 3.3V (Coord: 10.3 , 3.2 TOP/BOTTOM)
- SOM 3V3 - 3.3V (Coord: 46.75, 27.2 TOP/BOTTOM)
- FMC 3V3 - 3.3V (Coord: 8.7 , 3.2 TOP/BOTTOM)
- P2V5 - 2.5V (Coord: 64.7 , 6.5 TOP/BOTTOM)
- LA P2V - 2.0V (Coord: 12.95, 26.25 TOP/BOTTOM)
- P1V8 - 1.8V (Coord:103.35,104.0 BOTTOM)
- FMC VADJ - 1.8V (Coord: 10.3 , 4.6 TOP/BOTTOM)
- SOM 1V8 - 1.8V (Coord: 53.65, 94.5 BOTTOM)
- P1VD - 1.0V (Coord: 15.1 , 64.8 TOP/BOTTOM)
- P1VD2 - 1.0V (Coord: 22.65, 64.8 TOP/BOTTOM)
- P1VA - 1.0V (Coord: 30.15, 64.8 TOP/BOTTOM)
- P1VA2 - 1.0V (Coord: 37.5 , 64.8 TOP/BOTTOM)

The functional test: The test bench is formed by:

- Slow Control Ping
- Low Speed Lines Test
- High Speed lines Test

Slow Control Ping: Once programmed from chapter 2.3, insert the SD card and power on the PACE-SC. Connect the Ethernet cable to the second socket and enter through ssh to the IP address assigned. Execute the *pacetb.sh* with the command *ccping.*Wait until the prompt shows „AllOk“. This test will verify all I2C and MDIO devices on the board.

Low Speed Lines Test: Connect the PACE-TB (Test Bench) board to the TEBF0808 FMC socket, connect the Samtec Firefly ECUE cables to the FMC socket and to the PACE device under test (DUT) sockets. Power the TEBF0808 board with an standard ATX power supply and power up PACE DUT from the PSU. Press the push button S2 on to start the FPGA and processor. The TEBF0808 has the proper firmware programmed in the SD card. In case of failure the bit file can be programmed manually ruining the pacetb.bat(windows) orpacetb.sh(linux).This firmwa restarts a Linux on the board that can be accessed through the USB/SC, insert the SD card and power on and connect by ssh to the system. Execute the pace-tb.sh with the option − low. Wait until the prompt shows „All Ok“. Once in the command line execute the pace-tb.sh on /home/root (default). To start the test write pace-tb.sh -start and to stop pace-tb.sh stop. Set pace as in Slow Control Ping test and execute the pacetb.sh with the command −slow. Wait until the prompt shows „All Ok“. This will perform a test of all the TLK and ADC reception channels.

High Speed Lines Test: Connect the PACE-TB (Test Bench) board to the PACE DUT in the FMC socket. Power up and set pace as in Slow Control Ping test. Execute the pacetb.sh with the option −high.Wait until the prompt shows „AllOk“. This test bench will perform a loopback test of all the FMC 10Gbps lines.

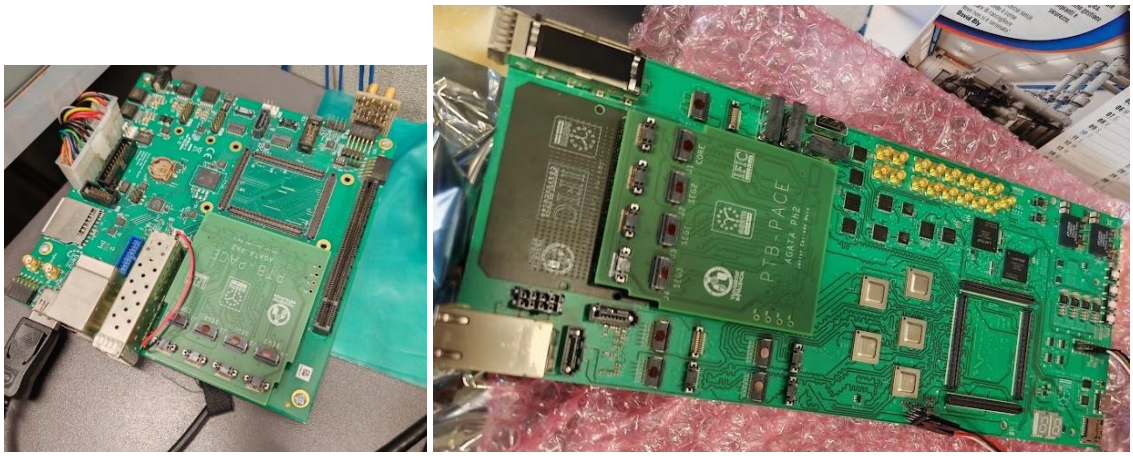

Figure 7. Left: Low Speed Lines Test Bench. Right: High Speed Lines Test Bench

4.TIMING

4.1. DELIVERY:

Within 12 months after the signature of the ordering.

4.2 ACCEPTANCE:

The AGATA acceptance test will consist of a customer acceptance test (CAT). The CAT has to be finished within two months after delivery.

4.3 WARRANTY:

The manufacturer has to provide a full warranty for a minimum of two years starting with the CAT.

5. CUSTOMER ACCEPTANCE TESTS:

Delivery : Emmanuel CLEMENT, GANIL, Grand Accélérateur National d'Ions Lourds Bd H. Becquerel F-14000 Caen – France clement@ganil.fr +33 2 31 45 49 08

The CAT will be performed using a test bench of the AGATA Collaboration located at the IFIC – University of Valencia –Spain after the Factory Functional Test (see previous section)

Any non-compliance observed during CAT has to be justified by the customer as not related to a defect test bench. These tests will be carried out within 2 months of the board being received.

To map out the Customer Acceptance Tests a CAT report will be provided by the customer to the provider as well as operating conditions.

1. Contacts

For any further information, bidders are asked to contact:

a) Regarding the technical part:

- **M. Emmanuel CLÉMENT** **Tel: +33 (0)2.31.45.49.08**
  Mail: emmanuel.clement@ganil.fr

b) Regarding the commercial part:

- **M. Emanuela INDRIES** **Tel: +33 (0)2.31.45.49.59**
  Mail: emanuela.indries@ganil.fr

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