Pierre Auger Observatory

Surface Detector Electronics Upgrade DEVELOPMENT PLAN

Abstract:
The SD electronics, will be upgraded to increase its functionalities, capabilities and reliabilities This document describes the development plan proposed for the upgrade.

Document written by:	P. Stassi Project System engineer	*Agreed by:*	T. Suomijärvi Task leader
Date:	*14 October 2016*	*Date:*	*14 October 2016*
Local Reference:	ATRIUM-2217	*Project Reference:*	*WP10LPSC02L*

Table of Content

ACRONYMS

ADC	Analog to Digital Converter
BGA	Ball Grid Array
CAD	Computer Aided Design
CPU	Central Processing Unit
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
ER	Environmental Requirement
FPGA	Full Programmable Gate Array
FR	Functional Requirements
Fs	Full scale
FTE	Full Time Equivalent
GPS	Global Positioning System
H/W	HardWare
ICD	Interfaces Control Document
IFL	InFrastructure and Labor costs
IR	Interface Requirements
LED	light-emitting diode
Msp/s	Mega samples per second
n/a	non applicable
OR	Operational Requirements
OS	Operating System
PAO	Pierre Auger Observatory
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PMT	PhotoMultiplier Tube
PR	Physical Requirements
QR	Quality Requirements
RD	Reference Document
RDA	Research and Development Array (Auger North)
RF	Radio Frequency
SD	Surface Detector
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronics Upgrade
SR	Support Requirements
S/W	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UB	Unified Board
UC	Upgrade Committee
USB	Universal Serial Bus
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VM	Verification Matrix
WBS	Work Breakdown Structure
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
02	A	14 Jan. 2013	P. Stassi	DRAFT for approbation
02	B	14 Jan. 2013	P. Stassi	2nd DRAFT for approbation
02	C	21 Jan. 2013	P. Stassi	Minor modifications
02	D	13 Feb. 2013	P. Stassi	Minor modifications
02	E	14 Feb. 2013	P. Stassi	Minor modifications
02	F	23 May. 2013	P. Stassi	Risk analysis removed, references doc. added
02	G	10 Sep. 2013	P. Stassi	Text and Ref. update after Lisbon meeting
02	H	05 Feb. 2014	P. Stassi	Minor corrections
02	I	10 March 2014	P. Stassi	Contributors added
02	J	27 Nov. 2014	P. Stassi	Update after col. Meeting of Nov. 2014
02	K	03 June 2015	P. Stassi	Update after col. Meeting of 2015
02	L	14 Oct. 2016	P. Stassi	Update for Auger Prime CDR

1. INTRODUCTION

The actual studies and results of the experimental data produced today at the Pierre Auger Observatory suggest new needs for capabilities, especially for the SD Electronics (SDE).

This document will propose the plan to organize the development of the upgraded SD electronics, including work packages, resources, risk and schedule.

The electronics system, concerned by the present document can be defined in reference to the present design of SD Electronics (RD1) as:

- Unified Board
- Front End
- LED Flasher
- GPS System

The 3 PMTs units used in the present SDE version are not considered in this document because not upgraded.

This upgraded set up will be designed and labeled in the present document "**SDEU**", Surface Detector Electronics Upgrade.

1.1. Reference Documents

RD1 The Pierre Auger project, Technical Design Report, September 2004

RD2 SDEU technical specification document, *WP10LPSC03_SDEU_Specification.*

RD3 SDEU Project Risk Analysis document, *WP10LPSC06_SDEU_Project_Risk_Analysis.*

RD4 AugerPrime WBS SDU document.

RD5 AugerPrime General Schedule document.

2. PRODUCT BREAKDOWN STRUCTURE (PBS)

The SDEU as defined in the specification document (RD2) is described below with 10 sub-products, identified as follow:

- **1-The PMTs signal Conditioning**
  - Amplifiers, filters, signal conditioning
- **2-The PMTs signal Digitizing**
  - ADCs
- **3-The Storage and Trigger construction**
  - Trigger algorithm in FPGA (firmware)
- **4-Event Building and Processing**
  - CPU, memories, OS and software
- **5-The Slow Control management**
  - Environmental sensors reading, PMTs high voltages control and voltage and current monitoring, solar power system monitoring. Dedicated software
- **6-Calibration management**
  - light generators and light generators management
- **7-The Time Tagging**
  - Commercial GPS and time tagger in FPGA (firmware)
- **8-Communication links management**
  - Serial, Ethernet, USB, external detectors digital interface
- **9-Power supplies management**
  - DC converters, filters and protections
- **10-Mechanics**
  - Housing, front panel, cables and connectors

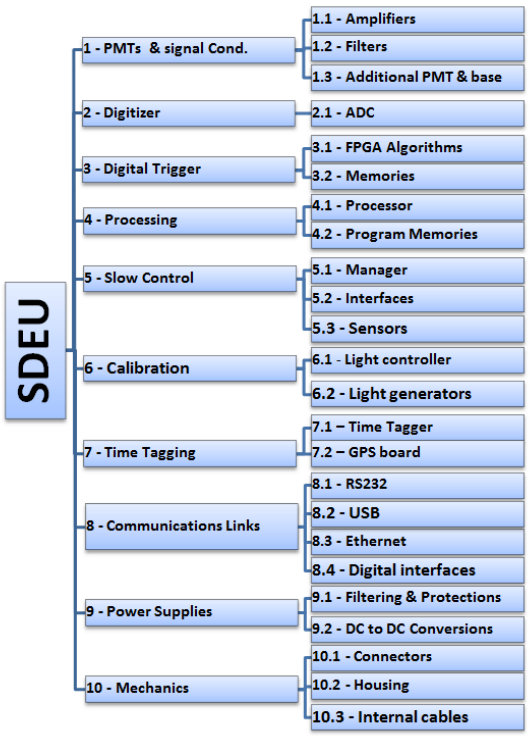

Figure 2.a - SDEU product breakdown Structure

3. GENERAL ACTIVITIES BREAKDOWN STRUCTURE

The tasks needed to achieve the development of the SDEU described in the previous chapter and are defined below with 10 items:

#	*Names*	*Comments*
AB1	**Management**	Organization and coordination
AB2	**Studies & Simulations**	Concerns H/W and S/W
AB3	**Designs**	Concerns H/W and S/W
AB4	**Tests definition & Test Benches**	Concerns H/W and S/W
AB5	**Validation of designs and performances**	Concerns H/W and S/W
AB6	**Procurement**	For tests benches and production
AB7	**Production**	Concerns final product
AB8	**Assembly, Deployment and Validation**	On site, concerns final product
AB9	**Maintenance**	On site
AB10	**QA, PA and Documentation**	Concerns all project

Table 3.a – Activity Breakdown Structure

4. WORK PACAKGES DEFINITION

The work packages needed for the complete development are defined below:

#	*Names*
WP1	**Analog PMTs signal processing**
WP2	**Trigger development**
WP3	**Time Tagging development**
WP4	**Slow Control development**
WP5	**UUB H/W Design & Integration**
WP6	**UUB S/W development**
WP7	**Calibration & Control tools development**
WP8	**Assembly, Deployment and Validation**
WP9	**Simulation and Science Validation**
WP10	**Project Management**

Table 4.a – Work Packages

The tasks previously listed in chapter 3 are partially or totally included in the Work Packages.

4.1. WP1 – Analog PMTs signal processing development

Studies to be conducted:

- *Anode to Dynode signal ratio and dynamic range optimization*
- *PMT signal interface optimization*
- *Accuracy of the Nyquist filter*
- *Optimization of ADC (sampling frequency, dynamic range, noise level)*

Electronics design
Procurement for this work package
Test board & test bench realization for this WP.
Firmware drivers design which can be in VHDL (or Verilog)
Prototype production participation
Tests and validation of the design
Documentation and test reports

Inputs:	***- Sciences and technical requirements*** ***- Existing design*** ***- Simulation (WP9) results.***
Deliverables:	***- Analog design to be integrated in the UUB Hardware design*** ***- Documentation***

4.2. WP2 – Trigger development

Studies to be conducted:

- *Present trigger adaptation and optimization*
- *New triggers possibilities*
- *Adding multiple trigger capabilities*

VHDL (or Verilog) code design (firmware)
Tests and simulation of the code
Test board & test bench realization
Tests and validation of the design
Documentation and test reports

Inputs:	***- Sciences and technical requirements*** ***- Existing code***
Deliverables:	***- VHDL (or Verilog) design to be integrated in the UUB FPGA design*** ***- Documentation***

4.3. WP3 – Time Tagging development

Studies to be conducted:

- *Time tagging algorithm adaptation and optimization to modern GPS*
- *Evaluate and select the most suitable commercial GPS board*

VHDL (or Verilog) Time tagging code design
GPS board procurement management
Test board & test bench realization for this WP
GPS Board characterization
Tests and validation of the code design
Documentation and test reports

Inputs:	***- Sciences and technical requirements*** ***- Existing code***
Deliverables:	***- GPS boards tested and characterized*** ***-VHDL (or Verilog) Time tagging code to be integrated in UUB FPGA design*** ***- Documentation***

4.4. WP4 – Slow Control development

Studies to be conducted:

- *Optimization of the existing design,*
- *Eventual addition of new parameters and sensors*
- *Inclusion of monitoring and alarms capabilities*
- *Adding failure detection and diagnostics capabilities*

Hardware design including eventual new sensors
Software design code
Procurement for this work package
Test board & test bench realization for this WP
Prototype production
New sensor procurement and production (if any)
Tests and validation of the complete design
Documentation

Inputs:	***- Sciences and technical requirements*** ***- Monitoring requirements*** ***- Existing design***
Deliverables:	***- Hardware design to be integrated to UUB design*** ***-Hardware design for new sensors*** ***-Micro-Controller Software design*** ***- Documentation***

4.5. WP5 – UUB Hardware Design & Integration

Studies to be conducted:

- *General architecture optimization*
- *Evaluate and select the most suitable components*
- *Addition of diagnostics and failure detection mechanisms*
- *Reliability optimization*

Electronics design and integration of the other work package designs
Procurement control responsibility for complete UUB boards
Test board, test bench & test software realization
Tests and validation of the design
Prototypes, pre-production, production
Performing stress and aging processes
Documentation

Inputs:	***- Sciences and technical requirements***
	- WP1 to WP4 design and documentation
	- WP6 to WP9 design and documentation
	- Existing design, including RDA design
Deliverables:	***- UUB board, prototype and final production***
	- Test benches
	- Documentation

4.6. WP6 – UUB Software development

Studies to be conducted:

- *OS9 to Linux migration of present UB Software*
- *Software and firmware optimization*
- *Addition of diagnostic mechanisms*
- *New software capabilities, new compression algorithm*

Software design
Test board realization
Tests and validation of the software design
Documentation

Inputs:	***- Sciences and technical requirements***
	- WP5 design and documentation
	- Existing design, including RDA design
Deliverables:	***- UUB Software to be integrated in UUB Hardware***
	- Documentation

4.7. WP7 – Calibration & Control tools development

Studies to be conducted:

- *New light generator controllers*
- *Mechanical and optical design*
- *Addition of new software capabilities*

Hardware design for light generator controller
Software design which can be in VHDL (or Verilog)
Procurement for this work package
Test board & test bench realization
Prototype production
Tests and validation of the design
Documentation

Inputs:	***- Sciences and technical requirements*** ***- WP2 and WP9 design and documentation*** ***- Existing design***
Deliverables:	***- Hardware design to be integrated to UUB Hardware design (controller)*** ***-Software design and/or VHDL code to be integrated in UUB Software and/or FPGA design*** ***- Documentation***

4.8. WP8 – Assembly, Deployment and Validation

Studies to be conducted:

- *New front panel*
- *Assembly process optimization*
- *End to End test process optimization*

Complete procurement of mechanics and cables
Assembly of the UUB
Final tests and validation
Deployment of the UUB assembled, on site
Product and deployment tracking
Maintenance on site
Documentation

Inputs:	***- Sciences and technical requirements***
	- WP5 design and documentation
	- UUB board and final production
	- Existing assembly and deployment processes
Deliverables:	***- Assembled upgraded SD Electronics operational on site***
	- Documentation

4.9. WP9 – Simulation and science validation

Studies to be conducted:

- *Simulation of different analog design configuration*

Validation of simulation results compared to sciences requirements
Validation of prototype test results compared to science requirements
Report and documentation

Inputs:	***- Sciences and technical requirements***
	- WPs design and documentation
Deliverables:	***- Simulation reports***
	- Documentation

4.10. WP10 – Project Management

Organization of the project
Tasks coordination
System engineering
Budget and funding report
Final validation and tests
Quality Assurance and Product Assurance
Documentation control

Inputs:	***- Sciences and technical requirements***
	- All work packages documentation
Deliverables:	***- General reports***
	- Documentation

5. RESSOURCES

5.1 Institution involved and contact people

#	Acronyms	Names	Country
1	BUW	Bergische Universitat Wuppertal	Germany
2	CNEA B	CNEA, Bariloche	Argentina
3	ITEDA	Intituto de Tecnologias en Detección y Astroparticulas, Buenos Aires	Argentina
4	CWRU	Case Western Reserve University, Cleveland	USA
5	FNAL	Fermi National Accelerator Laboratory, Chicago	USA
6	INFN Le	Istituto Nazionale di Fisica Nucleare, Lecce	Italy
7	INFN To	Istituto Nazionale di Fisica Nucleare, Torino	Italy
8	IPNO	Institut de Physique Nucleaire d'Orsay	France
9	KIT	Karlsruher Institut für Technologie	Germany
10	LPNHE	Laboratoire de Physique Nucléaire et Hautes Energies, Paris	France
11	LPSC	Laboratoire de Physique Subatomique et Cosmologie, Grenoble	France
12	MTU	Michigan Technological University, Houghton	USA
13	OSU	Ohio State University, Columbus	USA
14	PAO	Pierre Auger Observatory, Malargue	Argentina
15	LOD	Lodz University	Poland
16	SU	Siegen University	Germany
17	FZU	Institute of Physics of the Czech Academy of Sciences	Czech rep.

Table 5.1.a – Institution involved

#	Acronyms	Names	Email
1	BUW	Karl-Heinz Becker	becker @ physik.uni-wuppertal.de
2	CNEA B	Xavier Bertou	bertou@gmail.com
3	IREDA	Alberto Etchegoyen	alberto.etchegoyen@iteda.cnea.gov.ar
4	CWRU	Corbin Covault	covault@hippolyta.phys.cwru.edu
5	FNAL	Paul Mantsch	mantsch@fnal.gov
6	INFN Le	Giovanni Marsella	Giovanni.Marsella@le.infn.it
7	INFN To	Antonella Castellina	castelli@to.infn.it
8	IPNO	Tiina Suomijärvi [1]	tiina@ipno.in2p3.fr
9	KIT	Matthias Kleidges	matthias.kleifges@kit.edu
10	LPNHE	Hervé Lebbolo	herve@lpnhe.in2p3.fr
11	LPSC	Patrick Stassi [3]	Patrick.Stassi@lpsc.in2p3.fr
12	MTU	David Nitz	dfnitz@mtu.edu
13	OSU	James Beatty [2]	beatty@mps.ohio-state.edu
14	PAO	Ricardo Sato	rsato@auger.org.ar
15	LOD	Zbigniew Szadkowski	zszadkow@kfd2.phys.uni.lodz.pl
16	SU	Peter Buchholz	buchholz@hep.physik.uni-siegen.de
17	FZU	Martina Bohacova	bohacova@fzu.cz

Table 5.1.b – Contact persons

1 – Task leader
2 – Co-Task leader
3 – Project System engineer

5.2 Man Power and Facilities

Find below the man power in **FTE** needed and available for each work package, estimated for 4 years:

#	Names	FTE			
		Year 1	Year 2	Year 3	Year 4
WP1	Analog PMTs signal processing	2	2	2	2
WP2	Trigger development	0	0.5	0.5	0
WP3	Time Tagging development	2	2	2	2
WP4	Slow Control development	0.5	0.5	0.5	0.5
WP5	UUB H/W Design & Integration	3.5	2.5	2	1.3
WP6	UUB S/W development	2	1.5	1.3	0.8
WP7	Calibration & Control tools development	2	2	2	0.5
WP8	Assembly, Deployment and Validation	0	0.5	3	3
WP9	Simulation and Science Validation	1	1	0.2	0.2
WP10	Project Management	0.7	0.7	0.7	0.7

Table 5.2.a – Man Power in FTE

Find below the especial facilities needed and available for each work package:

#	Names	Facility
WP1	Analog PMTs signal processing	PMTs, measurement instrumentation, thermal chamber, FPGA development system, CAD system
WP2	Trigger development	FPGA development system, measurement instrumentation, thermal chamber.
WP3	Time Tagging development	0.1 m3, computer controlled thermal chamber, FPGA development system
WP4	Slow Control development	CAD system, FPGA and micro controller development system,
WP5	UUB H/W Design & Integration	FPGA development system, S/W development licenses, CAD system, measurement instrumentation, thermal chamber
WP6	UUB S/W development	S/W development licenses, FPGA development system
WP7	Calibration & Control tools development	CAD system, FPGA and micro controller development system, thermal chamber
WP8	Assembly, Deployment and Validation	PAO facilities
WP9	Simulation and Science Validation	Software simulation tools
WP10	Project Management	n/a

Table 5.2.b – Facilities

5.3 Work packages responsibility and participation

A work package can be done by several institutions and one institution can contribute to several work packages. Only one institution is responsible for a work package.

	WP1	WP2	WP3	WP4	WP5	WP6	WP7	WP8	WP9	WP10
BUW, Wuppertal - Germany				Resp.	Part.	Part.				
CNEA, Bariloche - Argentina					Part.	Part.		Part.		
ITEDA, Buenos Aires - Argentina					Part.			Part.		
CWRU, Clevland - USA			Resp.		Part.	Part.				
FNAL, Chicago - USA					Part.			Part.	Part.	Part.
FZU, Prague - Czech Republic					Part.					
INFN, Lecce - Italy	Resp.	Part.			Part.	Part.				
INFN, Torino - Italy	Part.				Part.	Part.	Resp.			
IPNO, Orsay - France	Part.				Part.			Part.		Resp.
KIT, Karlsruhe - Germany					Part.		Part.		Resp.	
LOD, Lodz - Poland		Part.			Part.					
LPSC, Grenoble - France				Part.	Resp.	Part.		Part.		Part.
MTU, Houghton - USA		Resp.	Part.		Part.	Part.	Part.		Part.	
OSU, Columbus - USA	Part.	Part.			Part.	Resp.		Part.		Part.
PAO, Malargue - Argentina					Part.			Resp.	Part.	
SU, Siegen University					Part.			Part.		

Table 5.3.a – Work Packages responsibilities and participations

5.4 Funding

The number of tanks in the field is 1660. If about 20% spares are produced this would yield a total production of about 2000 units.

- Total cost estimate for UUB production (without IFL costs) is **2 876 000.00 US$**
- UUB cost estimate is about **1440 US$** per unit.
- Design and development cost is included.
- Test benches and deployment costs not included

5.4.1 Detailed budget

Find below funding budget needed for production, including test benches and Small PMT:
(For more detail see the RD4 WBS document).

Pierre Auger Observatory Upgrade – Cost Estimate – Prototype Design — 07 September 2016 — 8.0

WBS	Activity	Total Cost[2] with Contingency and Infrastructure cost (IFL)		Contingency Part	Infrastructure cost Part (IFL)	Total Cost[3] with Contingency only (No Infrastructure cost, IFL)		Infrastructure cost[4] only (IFL)	
	Currency[1] >	US $	€	%	%	US $	€	US $	€
1.2	Surface Detector Electronics	4 115 021	3 740 928	11.7%	5.3%	3 897 979	3 543 618	217 041	197 310
1.2.1	Upgraded Unified Board Production	3 063 620.50	2 785 109.55	11.7%	4.2%				
1.2.2	Small PMT	997 977.20	907 252.00	11.0%	0.0%				
1.2.3	Test Benches Production	53 423.00	48 568.36	21.3%	12.8%				

Table 5.4.a –Detailed Budget

6. SCHEDULE

(More details can be found in the RD5, General schedule document).

6.1. Schedule per WP and project milestones

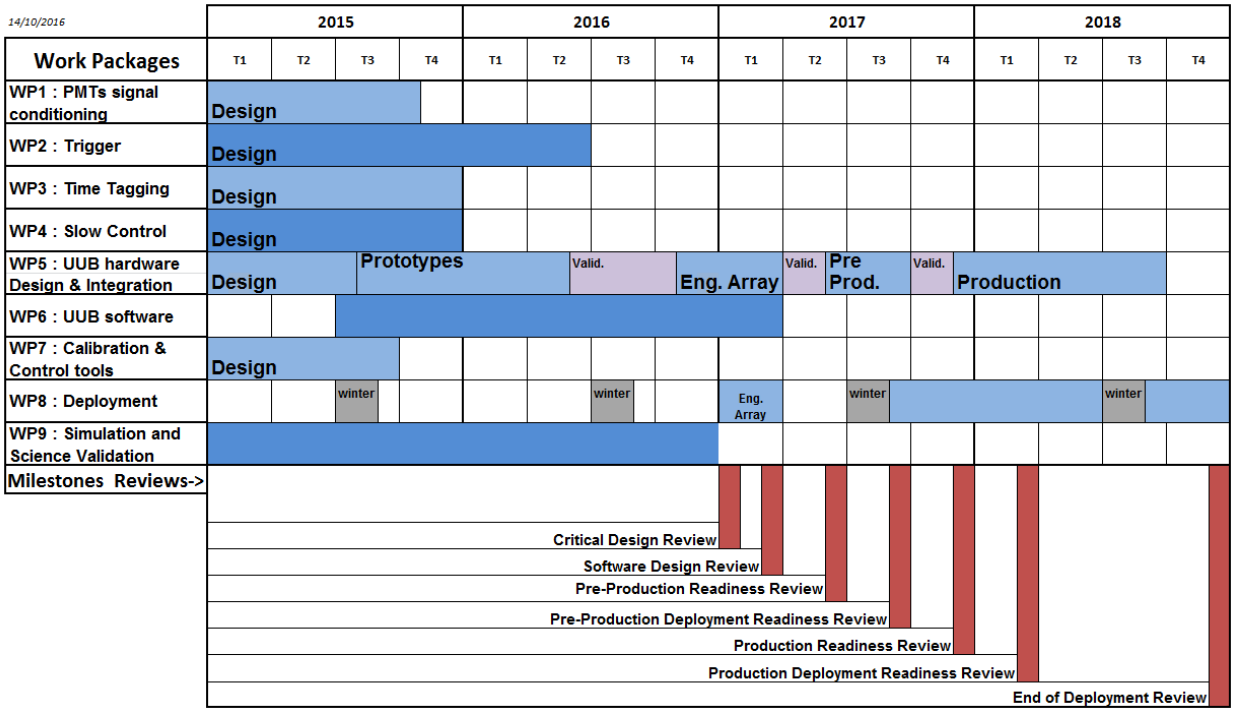

Figure 6.1.a - SDEU Schedule per WP

7. PRODUCTION AND TEST PLAN

The diagram below show the foreseen production and test plan:

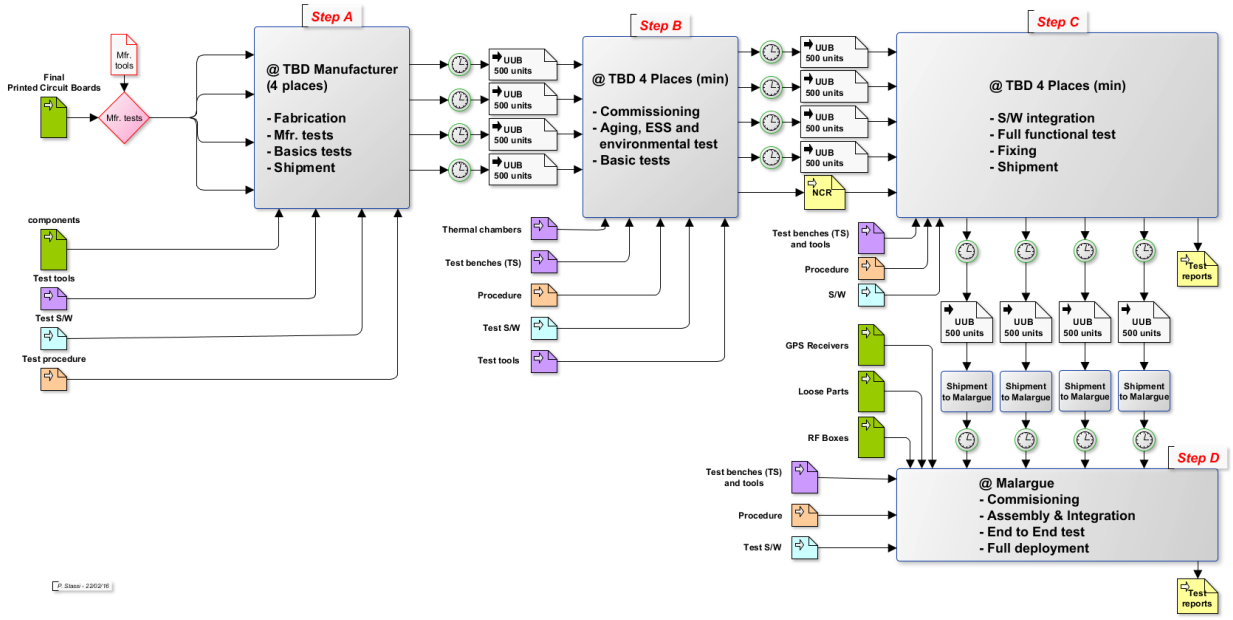

Figure 7.a - SDEU UUB Production and Test Plan

The production and test plan can be described in 4 steps:

- Step A, board manufacturing. Several places are foreseen, depending of the contribution policy in the collaboration. However one unique manufacturer (subcontractor) is recommended. Only one manufacturer for the PCBs is foreseen.

- Step B, several place are foreseen for the commissioning, ageing and environmental tests. These places are chosen within the institutes of the collaboration.

- Step C, several place are foreseen for the S/W integration and full functional tests. These places are chosen within the institutes of the collaboration.

- On institute is responsible for the UUB shipment to the PAO site

- Step D. PAO Site, commissioning, integration, end to end tests and deployment.

8. PROJECT RISKS ANALYSIS

For more detail see the RD3, Project risk analysis document.
The identified project risks are listed below:

N#	Risk Description	Occurrence	Impact severity on schedule	Impact severity on resource	Impact severity on performance	Global impact severity (average)
1	Risk of instability of the need for the project: (Change of priorities, instability of demand, insufficient strategic analysis).	2	2	2	2	2
2	Risk of problems associated with the project partners (abandonment, non-priority project, regulations and different standards, economic and social situation, political instability, fiscal instability).	2	3	2	1	2
3	Funding risk: change of research policy medium/long term, alternative funding, unfavorable budgetary arbitration, absence or discount in question of multi-year funding.	2	2	3	1	2
4	Risk of poor expression or lack of understanding of the scientific need.	1	2	2	2	2
5	Risk of evolution of the scientific need after the start of the project.	3	3	3	2	2.6 (3)
6	Risk of missing, incomplete, insufficiently accurate specifications.	2	3	2	2	2.3 (2)
7	Risk of innovative technical solutions, not validated in the laboratory or industrial.	3	3	2	1	2
8	Risk of technical solutions used to boundaries (insufficient margins), or non-mature (no feedback) or exotic.	3	3	2	1	2
9	Risk of uncontrolled material production, reception, testing, maintenance.	3	3	2	2	2.3 (2)
10	Risk associated with the transport of components, subsystems or system.	3	3	1	1	1.6 (2)
11	Risk of non-implementation of the quality assurance by the manufacturer (traceability, monitoring, non-conformity management, change management).	2	2	1	2	1.6 (2)
12	Risks related to the internal interfaces of the project: lack of definition, requirements volatility, poor or no coordination..	3	2	2	2	2
13	Risk of wrong announced date of one or more phases of the project, consequences: a) Interference between several phases of the project (e.g. R & D and production). b) Interference with other projects.	2	2	1	1	1.3 (1)
14	Risk on the sustainability of human resources: retirement, mobility project of people having knowledge not easily replaceable.	3	3	2	1	2

Table 7.a – Project Risks Analysis matrix

Find below the criticality matrix, showing the global criticality of the risks, deduced from the table 6a.

Likelihood					Color = Risk Index
Occ=4		*CP*	*CP*	*CP*	High
Occ=3		7 risks	1 risk	*CP*	Medium
Occ=2	1 risk	5 risks		*CP*	Low
Occ=1		1 risks			Very Low
	S1	S2	S3	S4	Global Severity

Table 7.b – Global criticality matrix (case tagged with red CP, are in the critical path)

No identified risks are in the critical path. Major risks are mostly related to possible lack of human resources or funding (RD3).

End of document