WP3: Time-Tagging Development: Photos showing sse of Vivado logic analyzer tools applied to debugging time-tagging module

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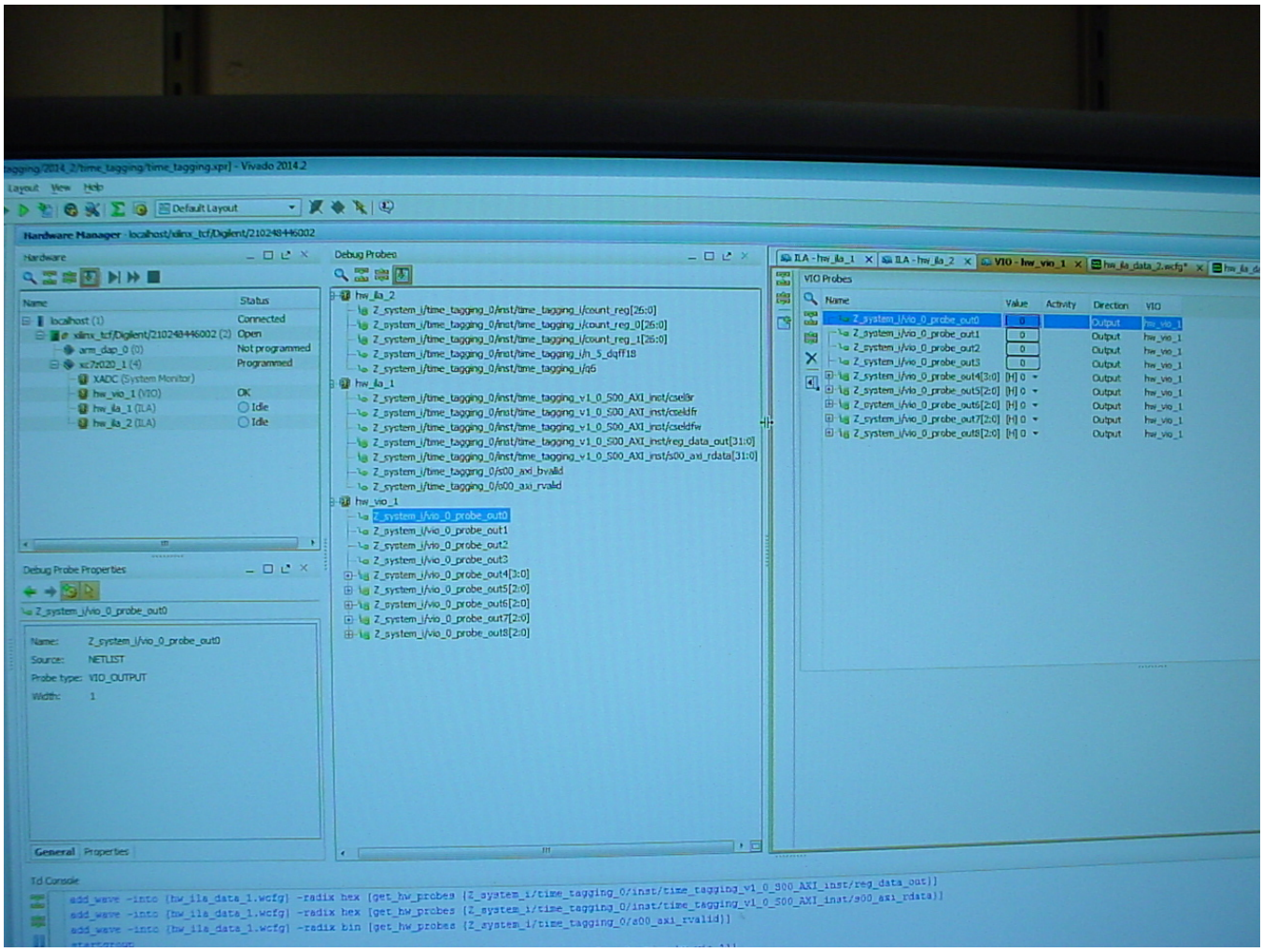

Figure 1: This photo shows the Vivado screen when running the hardware manager. There are two logic analyzer cores (one for each clock domain, and one Virtual I/O core running.

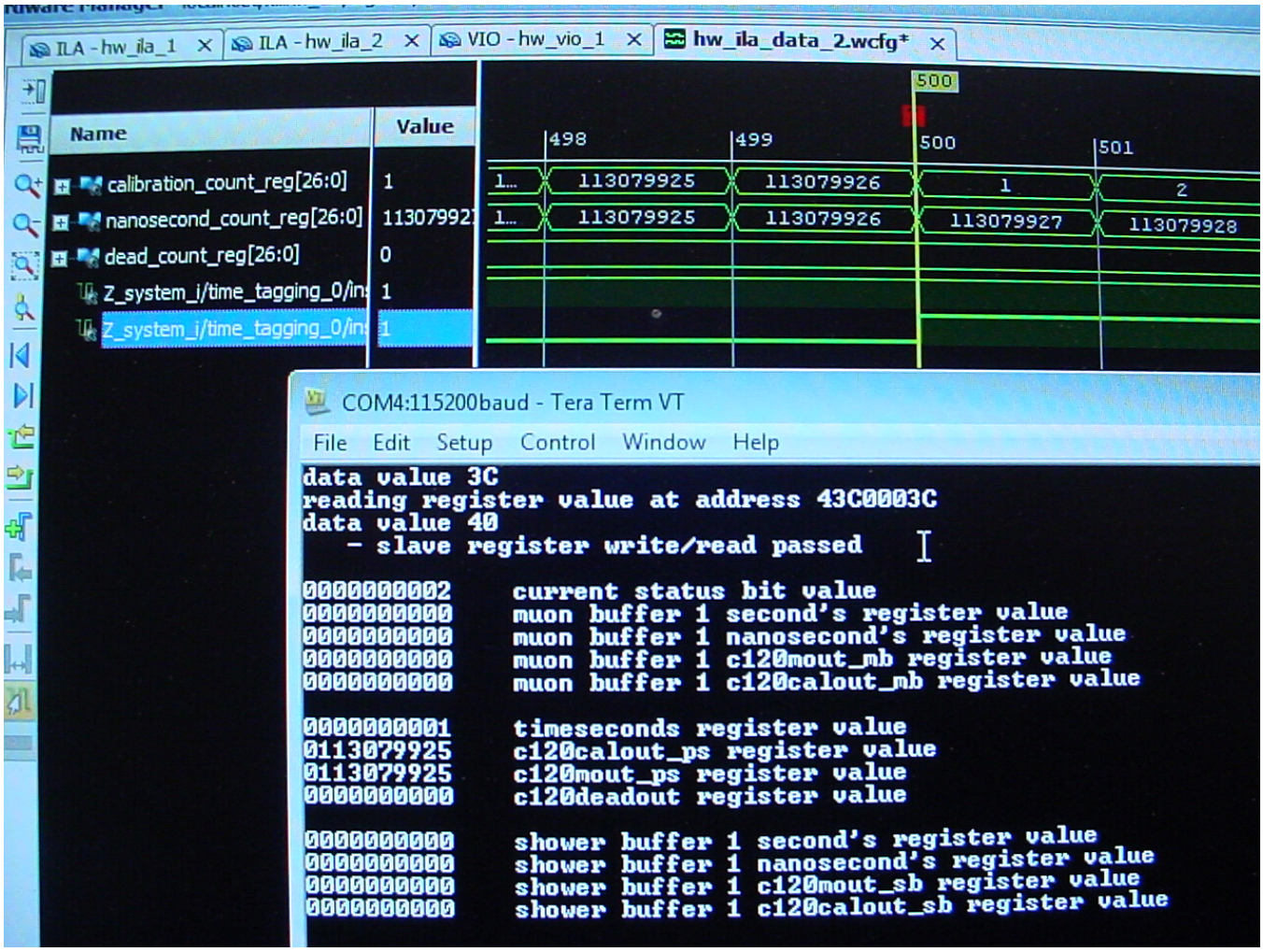

Figure 2: This photo shows the capture of the calibration counter (`c120calout_ps`) data and the capture of the nanosecond counter (`c120mout_ps`) values on the assertion of "pps" through VIO. Note how the calibration counter intentionally restarts at 1 instead of 0 value. Match up waveform value with the terminal value captured in C.

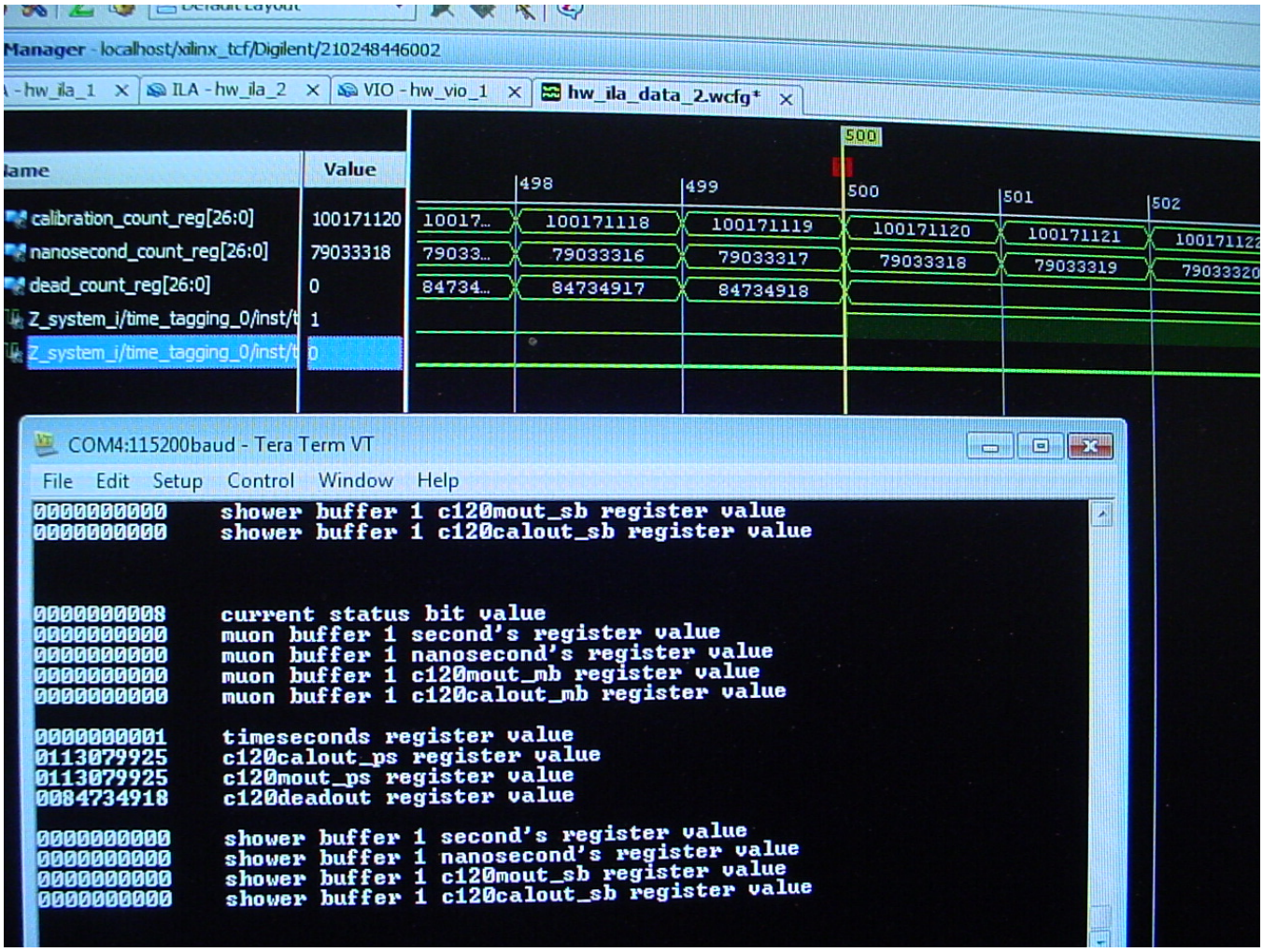

Figure 3: This photo shows the capture of the dead counter value on the de-assertion of "dead" through VIO. Match up waveform value with the terminal value captured in C.

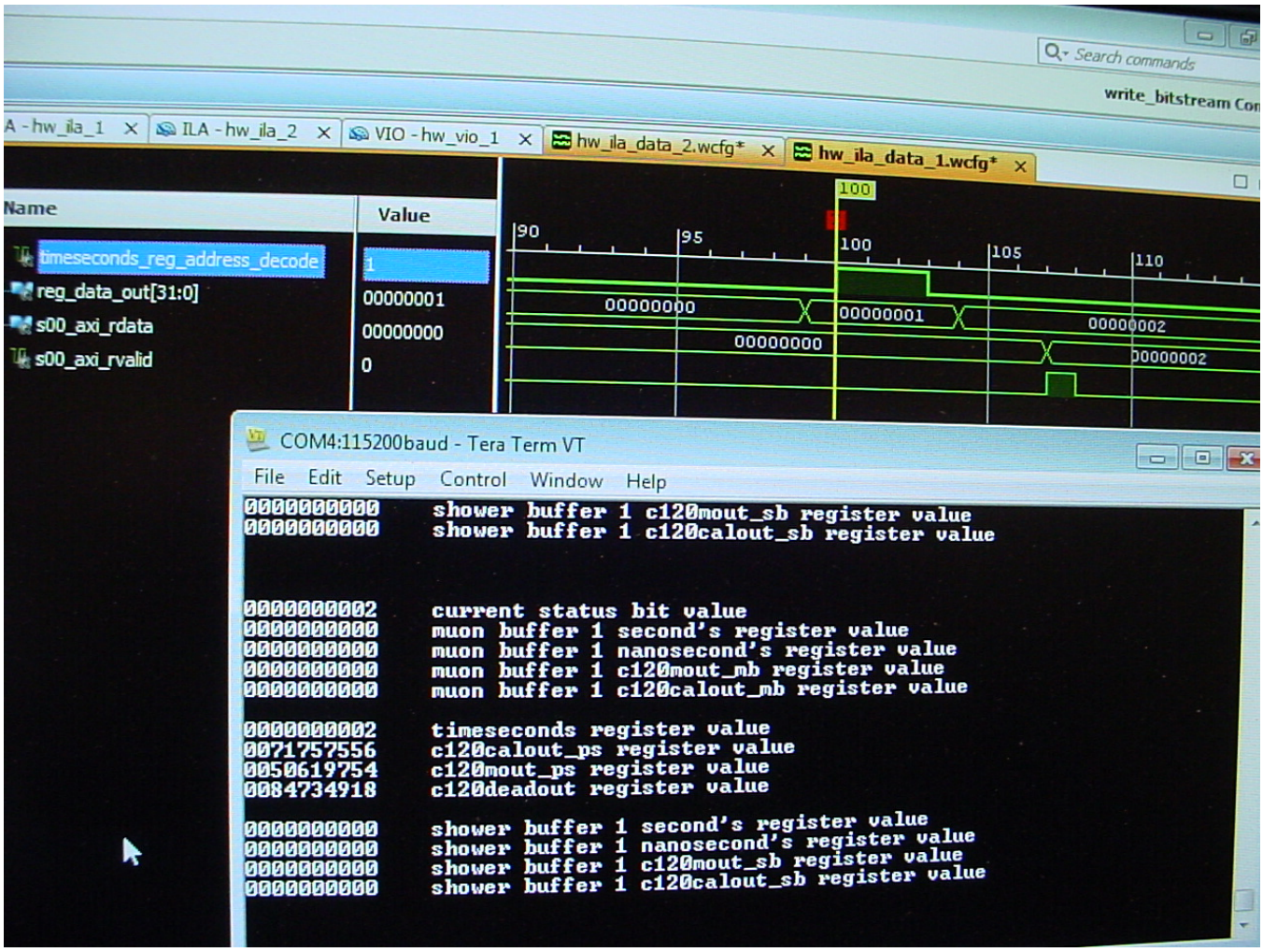

Figure 4: This photo shows the capture of the timeseconds counter on the assertion of "pps" through VIO. Match up waveform value with the terminal value captured in C.On the waveform, note how the "`axi_rvalid`" handshake is delayed to allow the register value to catch up, first stage at "`reg_data_out`" and finally at "`s00_axi_rdata`". "`s00_axi_rdata`" is also a vector, (I forgot the brackets in the name.)