Pierre Auger Observatory

Surface Detector Electronics Upgrade Critical Design Review

WP7 Calibration and Control tools
Technical Design Document

Purpose
This document supports the SDEU CDR for the evaluation of the WP7 readiness

Scope
This document describes requirements, goals, design implementation and status of the WP7 project of the SD Electronics Upgrade

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Acronyms

CDR = Critical Design Review
CR = Configuration Requirement
EA = Engineering Array
FR = Functional Requirement
GPS = Global Positioning System
LED = Light Emitting Diode
PAO = Pierre Auger Observatory
PMT = Photo Multiplier Tube
PPS = Pulse Per Second
SD= Surface Detector
SDE = Surface Detector Electronics
UB = Unified Board
UUB = Upgraded Unified Board

Table of Contents

System requirements

The upgraded system for calibration and control of the Surface Detector (SD) array ([1]) will:

1. Measure the linearity of the SD photomultipliers over the full dynamic range (FR63 in [2])
2. Cross calibrate the different readout channels of the SD tanks in their overlapping range (FR16-17-64 in [2])
3. Create artificial extended shower events on the SD array with arbitrary topology for verification of the acquisition and reconstruction chains (FR65 in [2])

The system is intended as a control tool to check operations of the SD detectors and electronics and to support calibrations.
The system does not implement regular SD calibrations for science data acquisition, and in particular it will not perform physics calibration of the SD tanks; these require dedicated acquisition of shower events in specific hardware configurations to measure the detectors performance (Vertical Equivalent Muon (VEM) signal, signal distribution and asymmetry, rates in different threshold and trigger conditions).

Design concept

These Work Package (WP) requirements can be met with a system of two Light Emitting Diodes (LED) that can simultaneously and independently flash light pulses inside the tank.
The light intensity must be high enough to sample the PMT linear and dynamic (requirements 1 and 2), and the LED trigger must be controlled with GPS time-accuracy (~4ns) with programmable delays (1ms max) to flash different tanks with arbitrary patterns to simulate extended showers (requirement 3).

This can be achieved with the existing LED system, which has been successfully used for measuring the linearity of the field PMTs, with some modification on the control electronics.
This represent a significant advantage as the existing LED system is installed and working on ~93% of the array, and the modifications to the control electronics can be integrated into the new Unified Board. We provide a brief description of the existing LED system below and describe in the following section details of the implementation.

Description of the existing LED system

The existing LED system ([4]) is based on pairs of Light Emitting Diodes (LED) mounted on a dedicated plastic head and installed on the SD through a dedicated window located at the centre of each tank.
The power and control cables are routed to the outside of the tank and into the Unified Board (UB), where a controller card plugged on the UB drives the trigger line to the LED pair as well as the bias voltage used to set the light intensity.
The shape of the light pulses is ultimately determined by a passive driver circuit connected the LEDs inside the plastic mount, and by the light reflections inside the tank. The LED signal shape is close to that of a cosmic-ray muon crossing the tank.

Design implementation

System components

The existing LED heads, including two LEDs, two driver circuits, the surrounding plastic mount and the cables to the UUB will remain in the upgraded system.

The current controller card will be replaced by a similar, upgraded circuit integrated to the main UUB printed circuit board, that represents the only change to the existing LED system.

New LED controller design

The new controller duplicates the existing circuit controlling the voltage to flash the LEDs, with the old 8-bit DAC (MAX520AEWE) replaced by an IC with at least 10 bits (AD5316ARU or AD5696). The maximum DC level flowing to the LED (A24V line) was increased to the maximum voltage available from the battery at any time, and limited to 24V, in order to provide enough light output to sample the extended dynamic range.

The new controller includes new circuitry for locking the LED trigger to a predefined GPS PPS signal via a hardware gate started by the enable PPS signal (EN_PPS line). This circuit is intended to provide a common trigger to all SD stations whose timing with respect to the GPS-PPS is controlled by dedicated hardware.
The synchronisation to the GPS-PPS will also be implemented as a software trigger in the FPGA (ASY_TRIG line); this trigger will include a programmable delay for generating arbitrary patterns over the array. The jitter of this trigger with respect to the GPS-PPS, with a delay set to null, will be compared to the hardware synchronised GPS locked trigger.

All control signals will be driven via the I2C bus common to the Slow Control (WP4) and the main UUB FPGA (WP5).
The list below summarises connections between the LED controller and other UUB sections:

1) EN_PPS (INPUT) : Enable PPS signal from Slow Control (WP4)
2) PPS (INPUT) : GPS PPS signal directly from GPS
3) ASY_TRG (INPUT) : software trigger from UUB FPGA
4) FLG_TRG (OUTPUT) : LED trigger flag to UUB FPGA

The LED controller uses a number of DC lines to power various IC, namely +5V, +3.3V, +12V, all taken directly from the main UUB power bus.
An unregulated DC line, limited to 24V, provides the maximum bias to the LED and is regulated via the main controller DAC

Software implementation

The DAC controlling the LED bias will be driven via I2C linux drivers loaded on the UUB FPGA, developed following WP6 prescriptions.

Prototype test board design

The LED controller for the prototype board is identical to the final one, but some flexibility was kept in the design to allow testing of:

1. two different options for the DAC controlling the LED bias voltage: the pinout of the DAC is compatible with the tested DAC AD5316ARU (10 bits) as well as with DAC AD5696 (16 bits)
2. timing of the LED trigger pulses with respect to the GPS PPS either via FPGA timing (through the ASY_TRIG input to the controller coming from the FPGA) or via a hardware gate generated by the dedicated circuit around a GPS-PPS with no delay

Test report and results on prototype

The principle of operation of the system is demonstrated by the existing LED system, by the modified LED controller for RDA [5], which implement the hardware synchronisation circuit with the GPS-PPS, and by field test with the SmallPMT that ensure that the full dynamic range can be probed with the existing LEDs when biased at 19V.

The actual implementation of the new controller will be tested in the lab on the first available UUB prototypes. We will perform:

- basic functional tests of the electrical connections
- verify control of the bias DAC
- run full linearity tests without PMTs

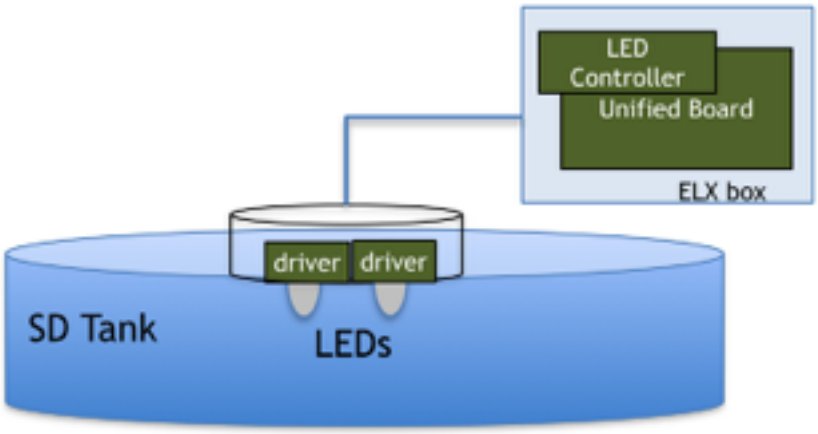
We will then perform full test of the system with PMTs in the Laboratory.

Field tests on the Engineering Array will assess full operation, including timing of the signals, and robustness of the system in the field.

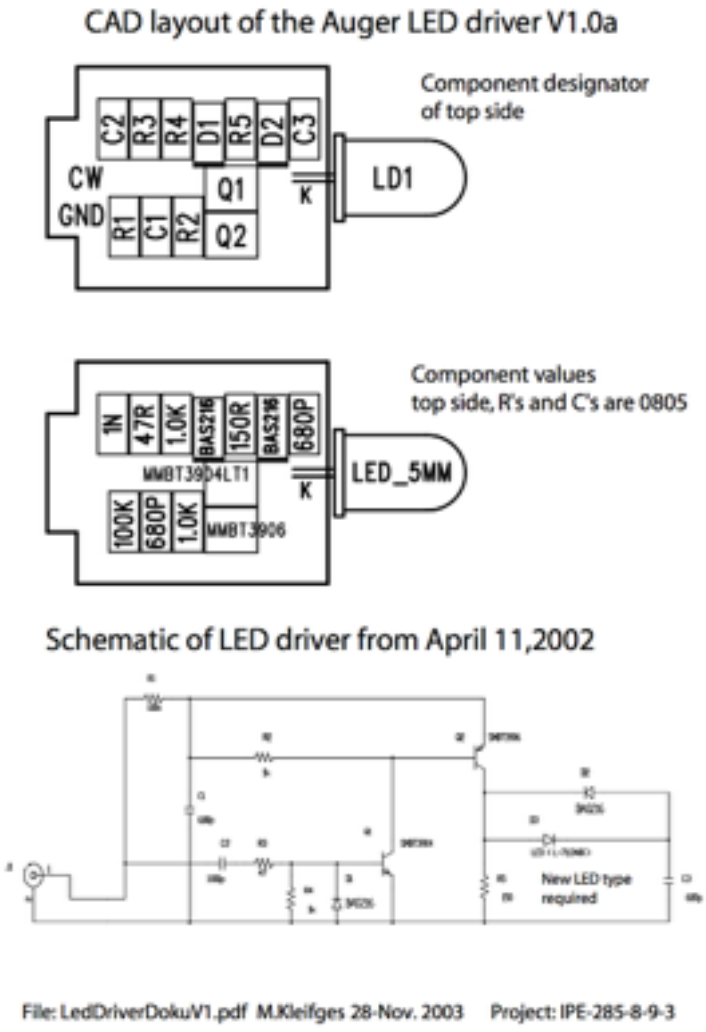
Design Status

The LED system design is completed and has flown down to the main UUB board design.
The final WP5 layout, including the new LED controller and its connections, needs to be distributed to the project and reviewed by all WPs.
Software development just started on the ZedBoard platform.

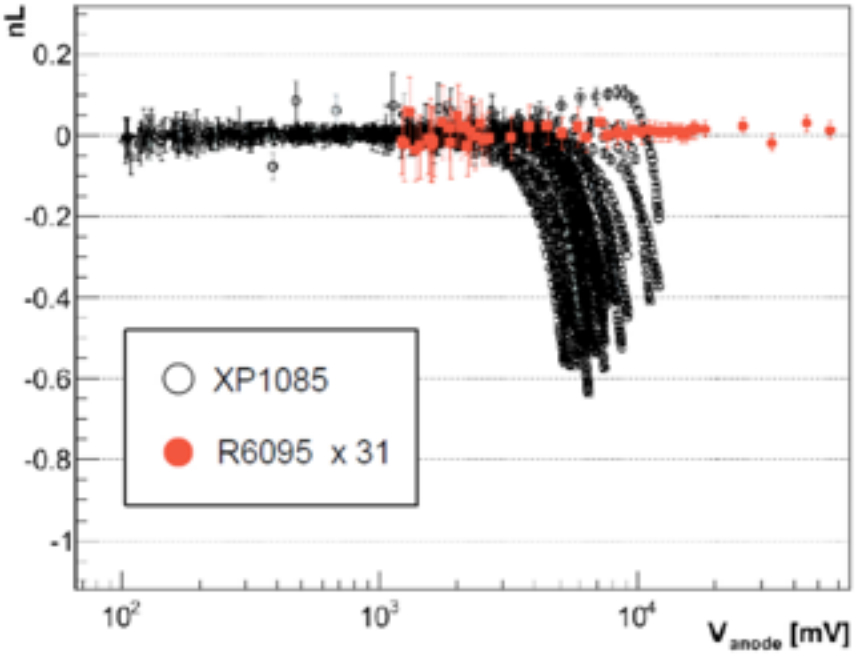
Figures



Schematic diagram of the LED system components

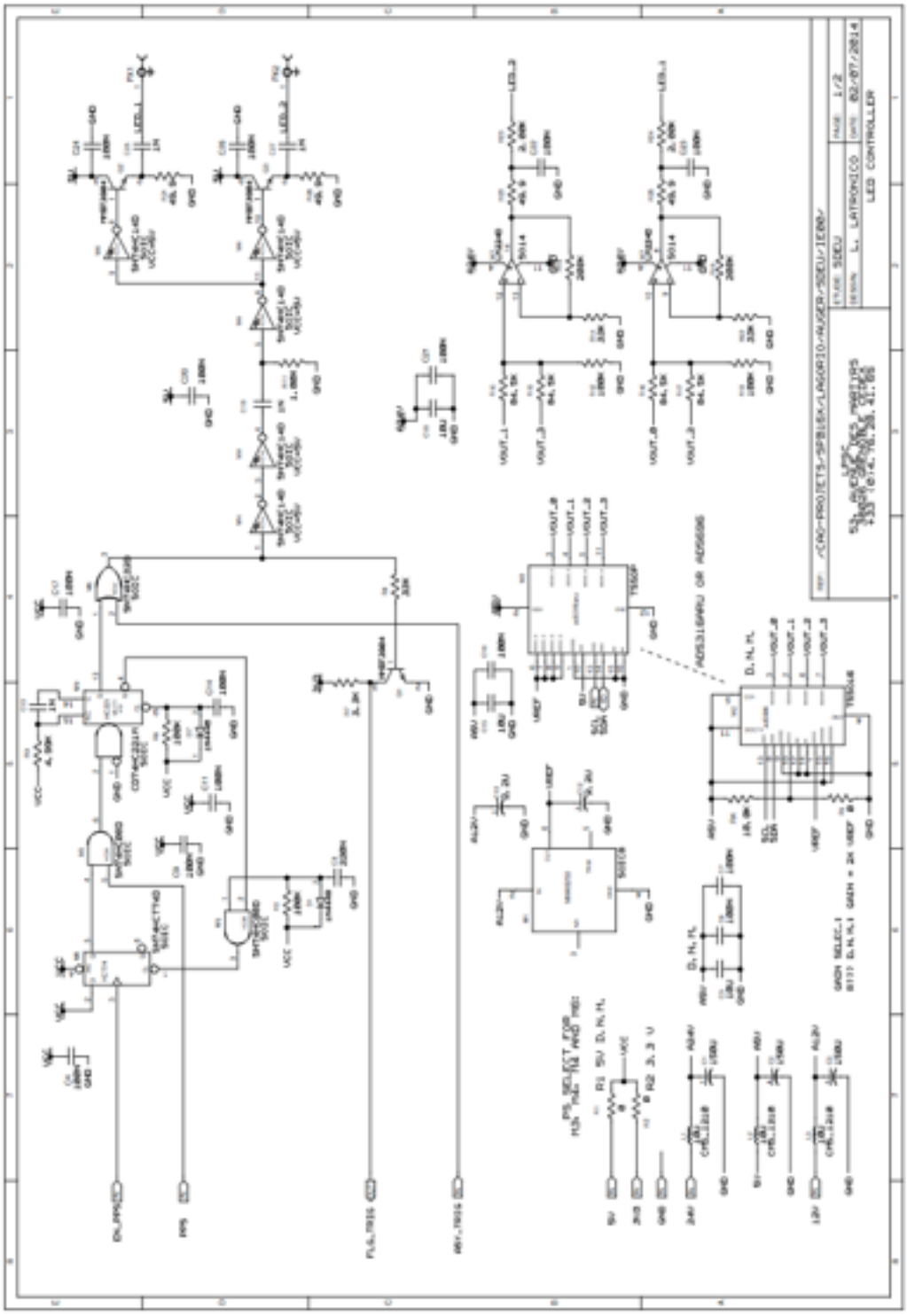


Block diagram and schematics of the existing LED driver



Linearity test of a standard PMT and a Small PMT from test tank DIDI obtained with the existing LED when biased at 20V

Schematics



Schematics of the new LED controller

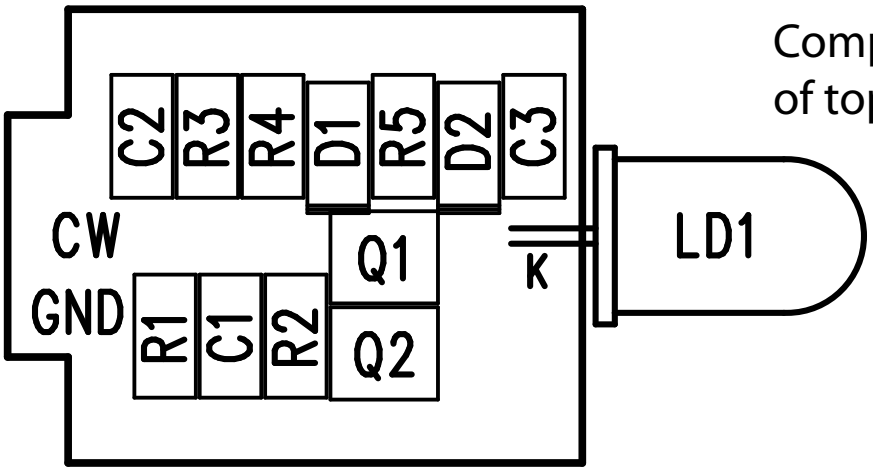
Annexes

1. LED Driver schematics, Bill of Material, mechanics
2. LED Controller schematics

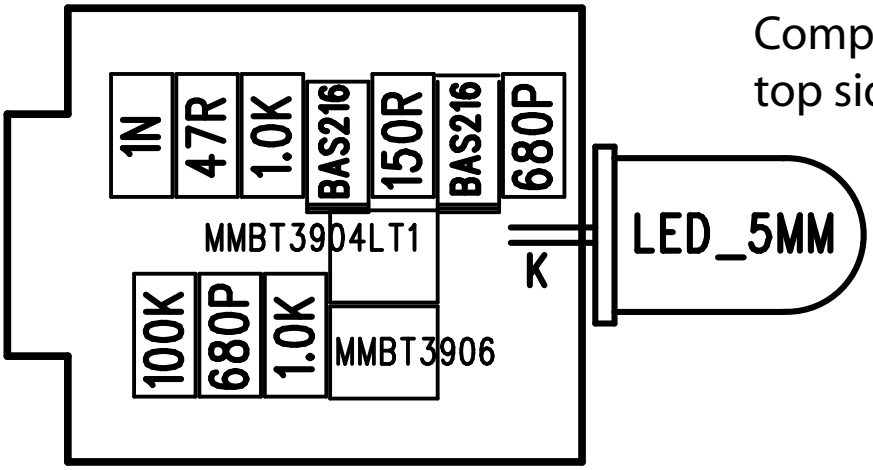
References

1. SDE Upgrade Plan
2. SDE Upgrade Specifications
3. Small PMT Development Plan
4. GAP Note 2003-052
5. GAP Note 2011-025

CAD layout of the Auger LED driver V1.0a

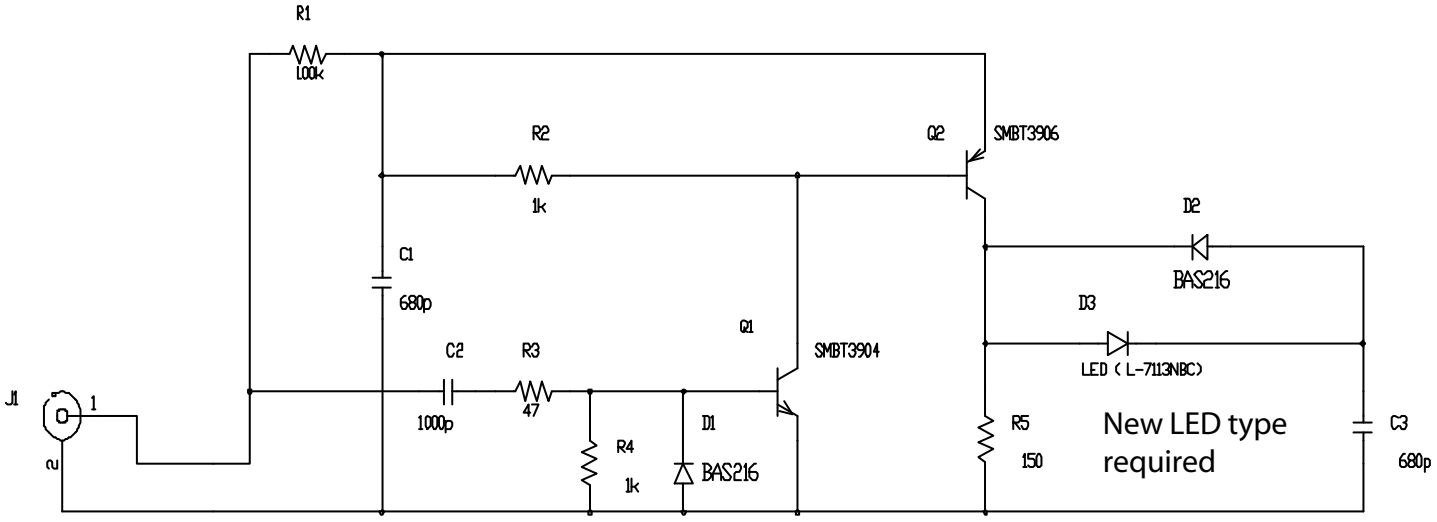


Component designator
of top side

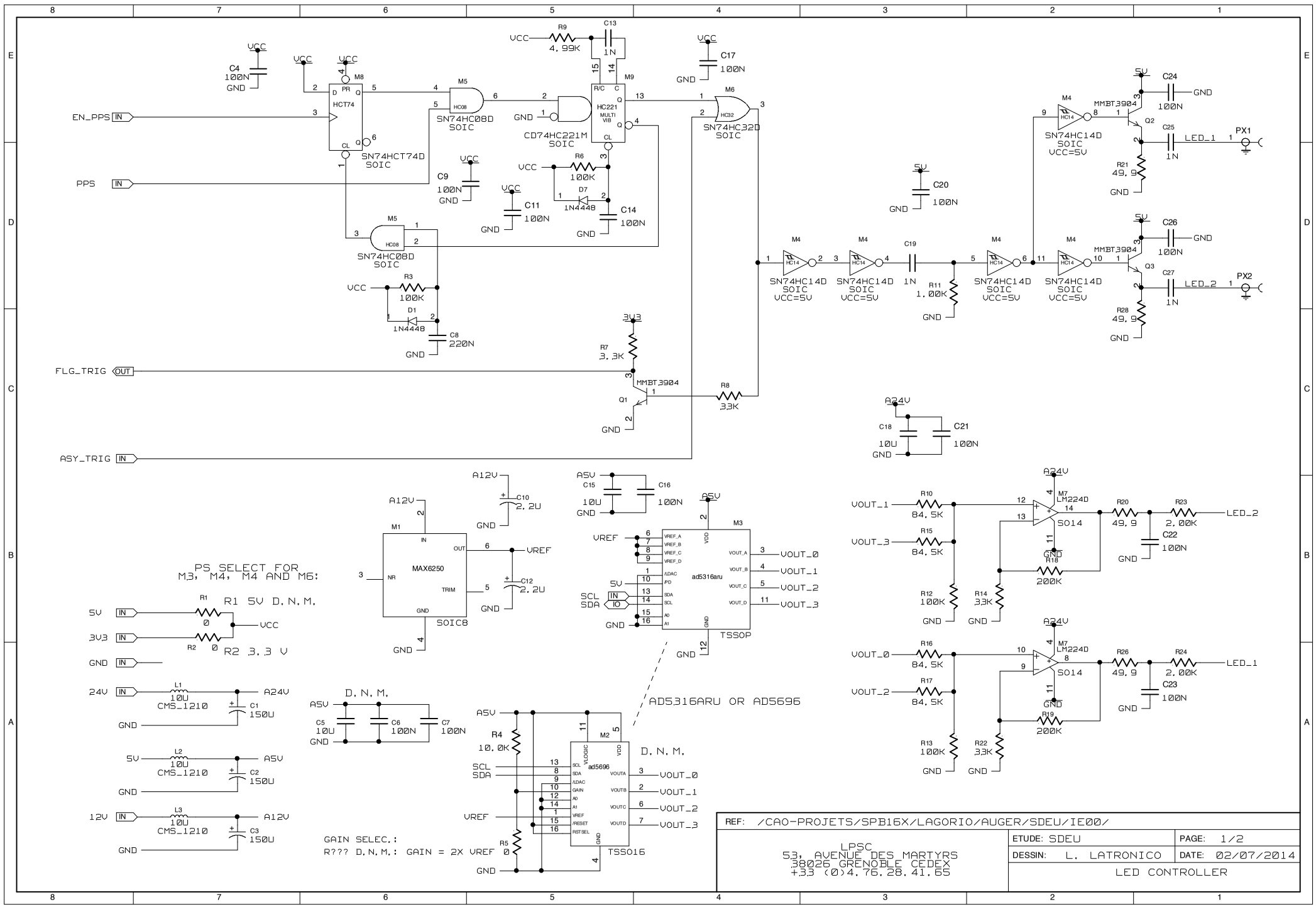


Component values
top side, R's and C's are 0805

Schematic of LED driver from April 11,2002



File: LedDriverDokuV1.pdf M.Kleifges 28-Nov. 2003 Project: IPE-285-8-9-3



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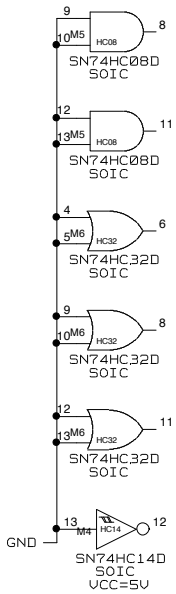
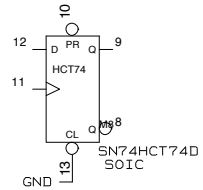
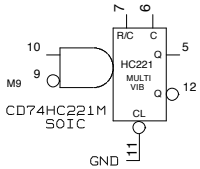
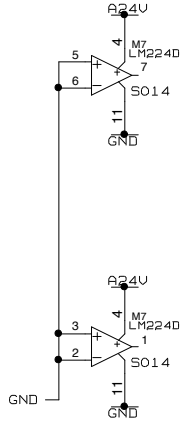
LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65	ETUDE: SDEU PAGE: 1/2 DESSIN: L. LATRONICO DATE: 02/07/2014 LED CONTROLLER









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