Discovering, Analysing and Mitigating Power Integrity, Signal Integrity and EMC/EMI Issues in PCB Layouts

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ANF CNRS 2018 : école électronique de l'IN2P3
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cadence®

Time Plan

Mercredi 26 septembre	08:30 10:00	PSPICE	Stéphan Mouquet (ARTEDAS)
		café	
	10:30 12:00	PSPICE (à confirmer)	Stéphan Mouquet (ARTEDAS)
	12:15	**Déjeuner**	
	16:00 17:30	Integrité du signal : utilisation de CADENCE SIGRITY	Kristoffer Skytte (CADENCE)
		café	
	18:00 19:30	Integrité du signal : utilisation de CADENCE SIGRITY	Kristoffer Skytte (CADENCE)
	20:00	**Diner**	

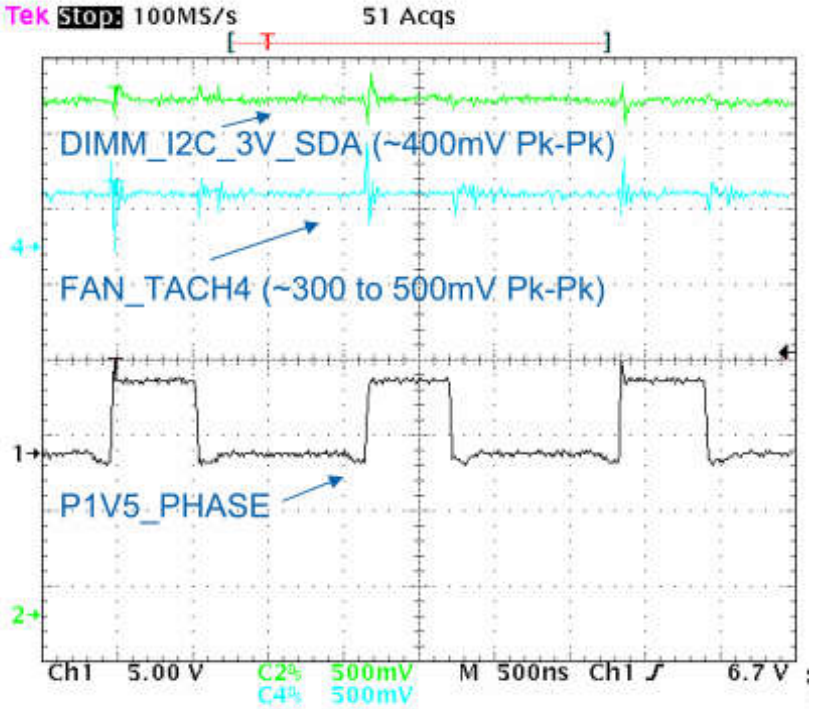
Topics

- Signal Integrity
- Power Integrity
- EMC/EMI
- Thermal
- Links with other Cadence Tools

A System Failure Case Story
Server Blue Screen

Switching Voltage Regulator Noise Coupling on PCB Level

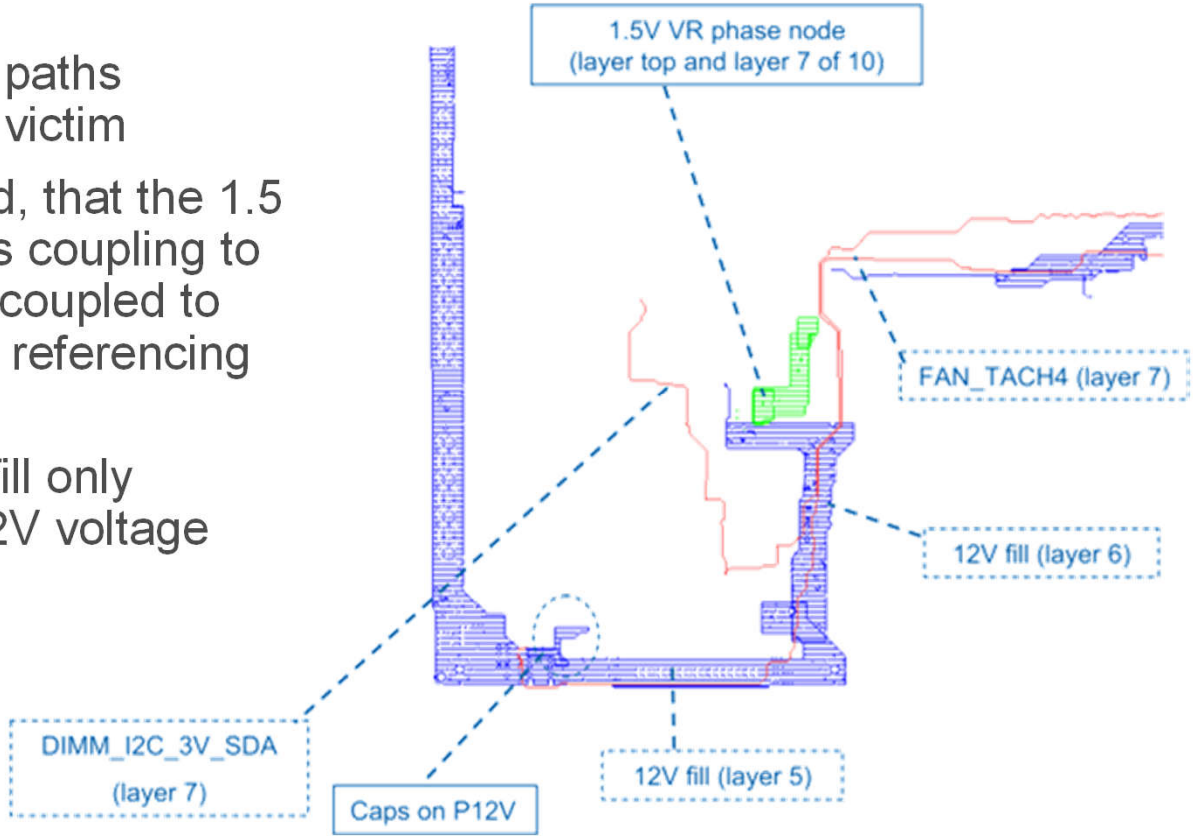
- System was hanging at irregular intervals
- Un-expected noise spikes in the I2C Control lines
- Frequency and Magnitude pointed at DC-DC Noise
- Probing of the I2C and DC-DC switching nodes identified the aggressor



Source: Amy Luoh et al "***Switching Voltage Regulator Noise Coupling Analysis for Printed Circuit Board Systems***" DesignCon 2009

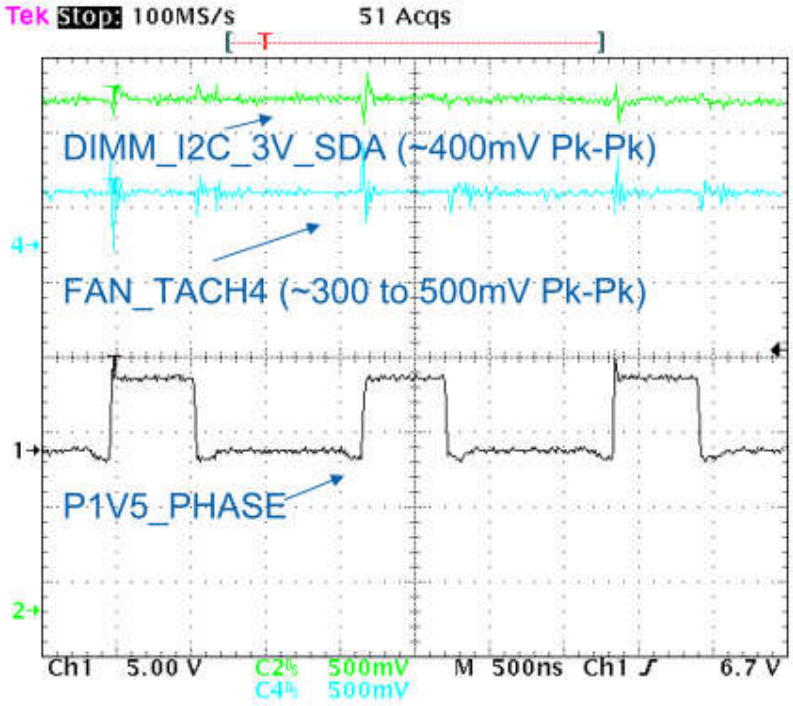
PCB Coupling Path

- No obvious coupling paths between source and victim
- However it was found, that the 1.5 voltage regulator was coupling to 12V fill which in turn coupled to the signals that were referencing the 12V fill
- The decaps on 12V fill only placed around the 12V voltage supply

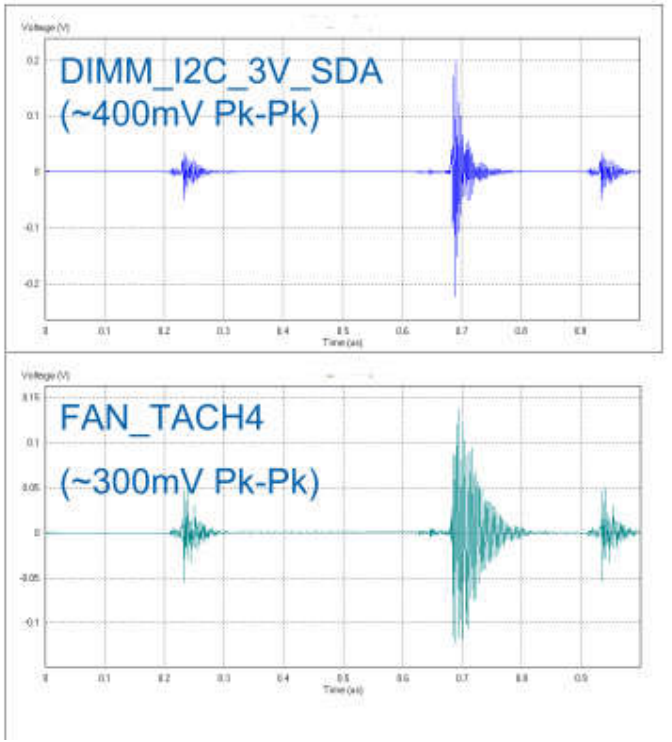


Noise Issue Reproduced in Simulation Environment

Measured results:

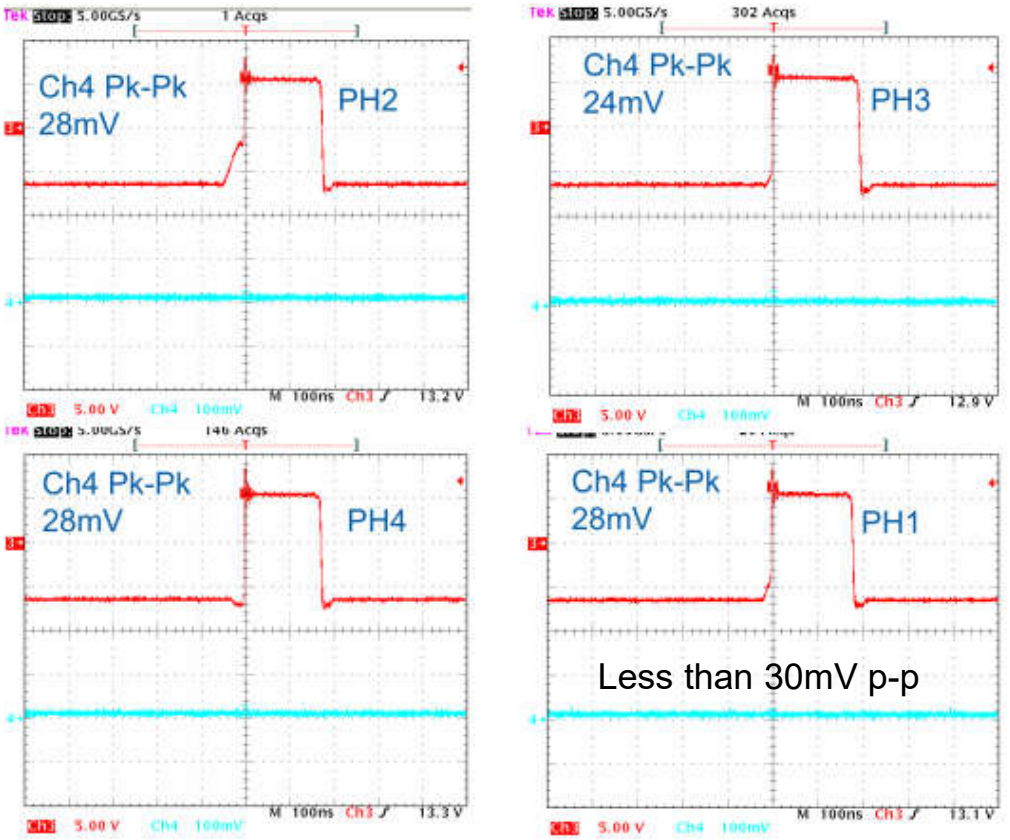


Simulated results:



Repaired Noise Coupling Issue

- Potential solutions
  - Improve decoupling of the 12V plane
  - Move switching nodes
  - Change reference of signals



Observations

- Was this a signal integrity, power integrity or interference issues?
  - From a system stand-point we don't really care – the system is malfunctioning and a fix is needed
- Several factors contributed to the problem but power delivery was central…
- So what should we conclude here?
  a) Letting critical signals reference power fills, is a bad thing and that referencing ground is better?
  b) SMPS switching nodes should have isolation rules?
     - Faraday cage with vias
     - Decoupling across power domains
     - Physical distance from other nets
  c) Decoupling needs to be rigorously applied to avoid resonances in power planes acting as reference for critical signals?
  d) ….

Signal Integrity - The Signal Distribution System

What is Signal Integrity (SI)?

- In broad terms SI is the engineering task of ensuring that an electronic system will work as designed despite the inherent non-idealities in the system
- For systems, this task used to be only related to managing the signals as they propagate through the system
- However a system will malfunction if improper power is delivered to system thus more and more focus has been put on this topic over the years although this field is sometimes referred to as Power Integrity (PI)

Signal Integrity
Aim of the Signal Distribution System (SDS)

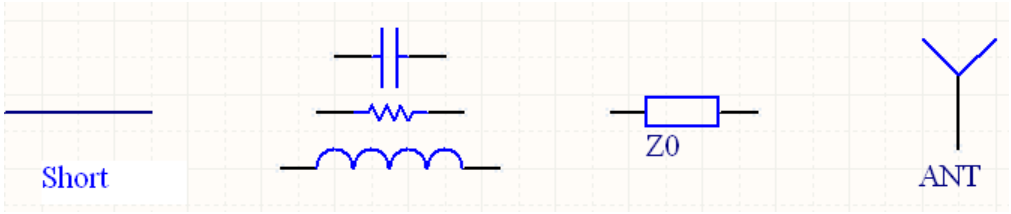
- To allow the components to properly interact in consideration of
  - High speed data lines
  - Distributing clocks / strobes
  - Control signals
  - Provide reference voltages for circuit functionality etc
- Derived requirements
  - The signal distribution system should not severely affect quality of the routed signals
    - Timing
    - Reflections
    - Skew
    - Loss
    - Undershoot etc
  - Nor should the signalling affect proper operation of other devices
    - I.e. through transmission line crosstalk, conducted or emitted noise

Digital System Electrical Specification

- Early digital design
  - Speed of system defined by clock frequency
  - Managing of clock in focus, i.e
    - Timing, setup/hold, skew
    - Propagation delay (as dictated by the logic gate delay)
  - System specified in time domain alone

- Todays and tomorrows digital design
  - Speed of system defined by clock frequency AND rise/fall time
  - Channel influence becomes important
    - Noise, jitter, channel loss
    - Propagation delay dictated by interconnect
  - System specified in both time and frequency domain

Evolution of Device Interconnects



	Ideal connection	Parasitics & Frequency dependency	Transmission lines	Emissions
	No loss Ideal short (a piece of wire)	Frequency dependent parasitics – losses, inductance, capcitance	Reflections Skew Crosstalk Delay	Noise: Disturbances conducted between parts within a design Emissions & Immunity issues
$\frac{t_{delay}}{t_{rise}}$	<< 1	< 0.1 (lumped)	≥ 0.1 (distributed) (ASTTL logic – Tclock=100MHz, trise=2ns)	?

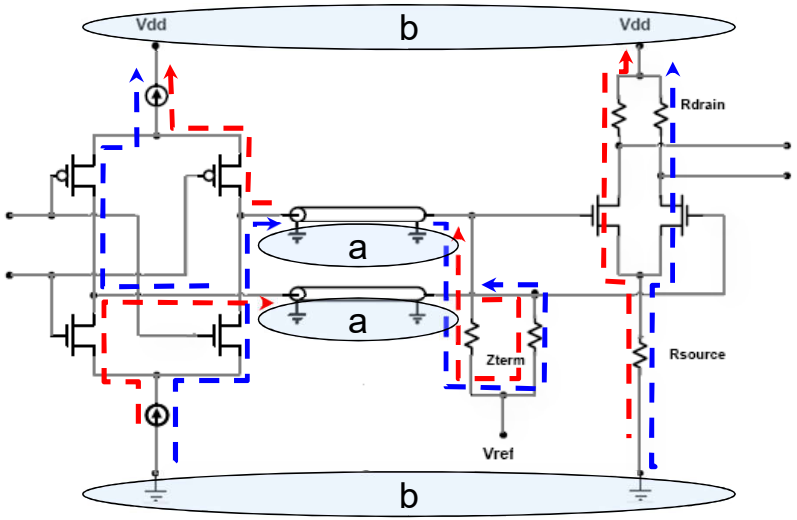
We will come back to this point later

Implicit assumptions in most SI analysis

- In the symbols on the previous slide, no attention was put on the reference for the interconnect – the reference was implicit through GND or “Net node 0”
- From Kirchhoff’s Current Law we know that current flows in loops
- In traditional spice simulations, net node 0 represents
  - a current sink / an ideal current return path
  - a convenient reference to which the voltage potential at any node can be referred – the voltage at this point is always 0V (zero volt)
- Is this an accurate representation of reality?
- Of course not!
  - From an engineering perspective what matters more of course is the question of how our assumption can affect the predicted system performance, thus…

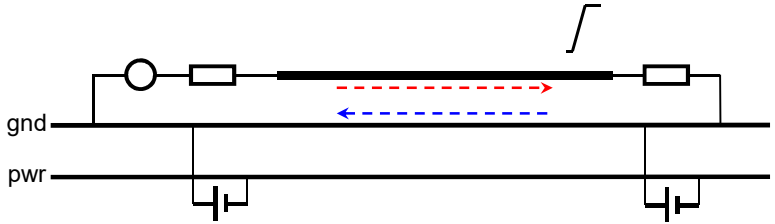
Implicit assumptions in most SI analysis (ii)

- Is implicit ground a practical assumption?
- Let's first make a simple investigation of a driver/receiver circuit

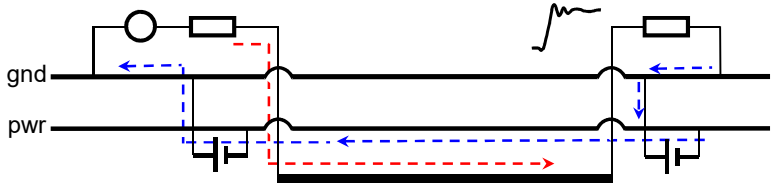


Signal Integrity vs. System Level Analysis

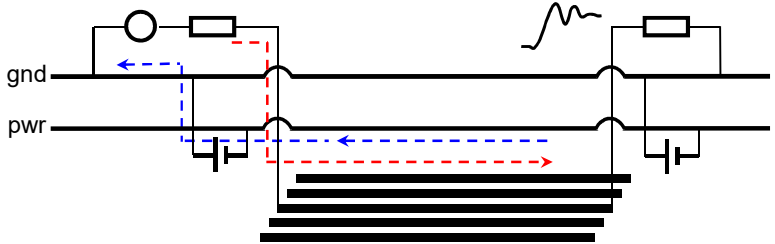
One signal switching without reference plane change (SI)



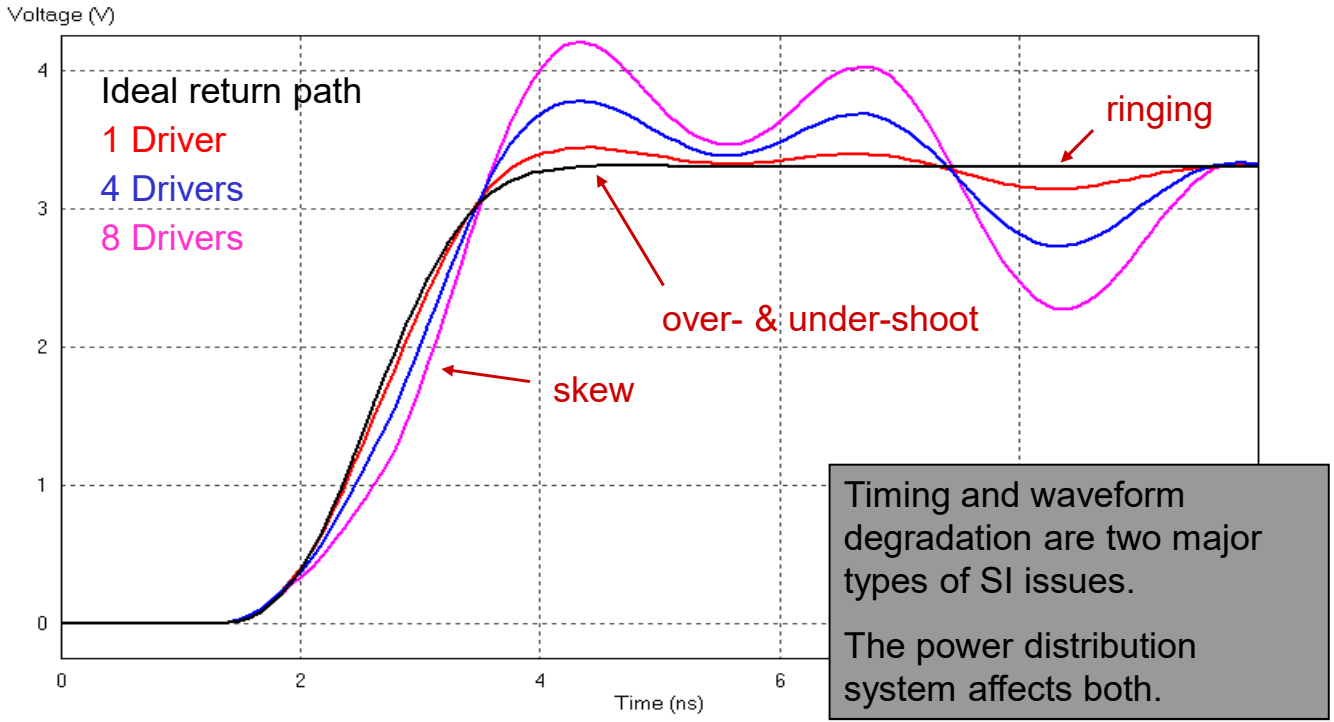
One signal switching with reference plane change (SI & PI)



Multiple signals switching with reference plane change (SSO)



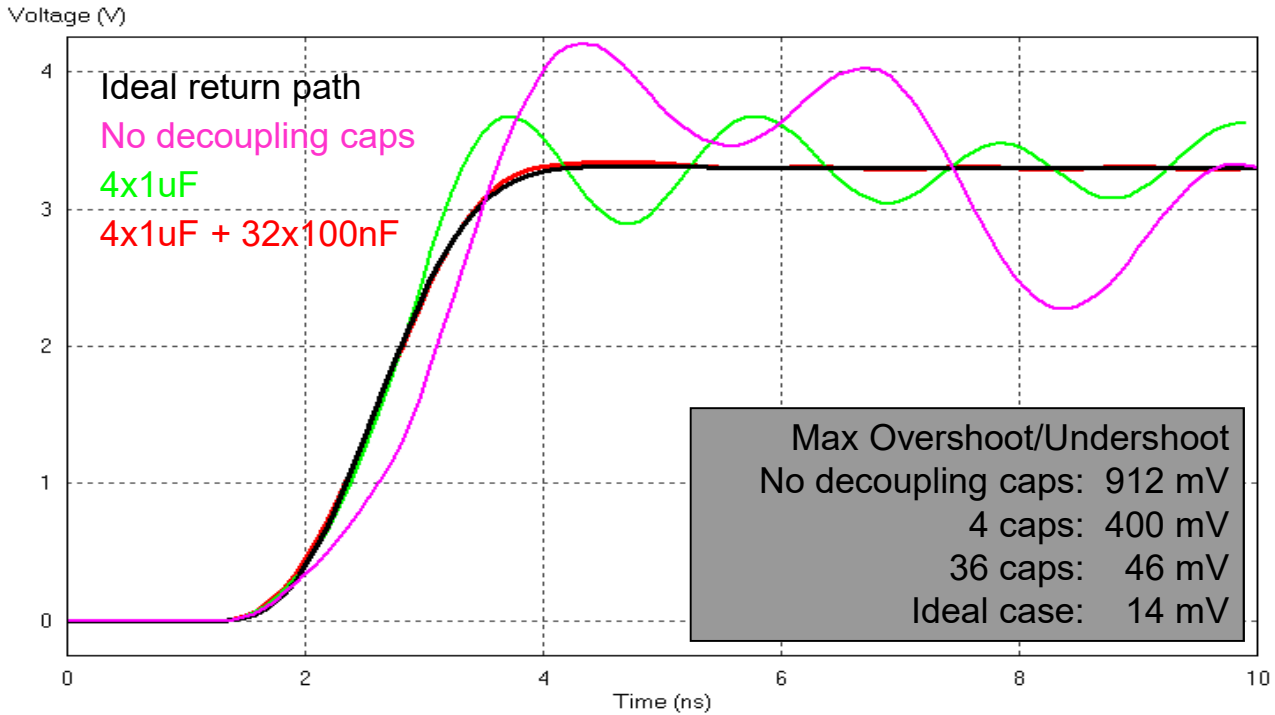
Signal Integrity vs. System Level Analysis
SSO – Simultaneous Switching Output



Timing and waveform degradation are two major types of SI issues.

The power distribution system affects both.

Signal Integrity vs. System Level Analysis
Effect of adding decoupling capacitors



Signal Integrity vs. System Level Analysis Observations

- The power distribution system can have a significant impact on the signal integrity, or in other words

> *Imperfections in the power delivery system can show up as signal integrity issues like skew, ringing, over- and under-shoot.*

- Current does not distinguish ground nets from power nets – the current flows in the signal nets' reference plane(s)
- Current avoids anything that impedes its flow. In electrical terminology: It takes the path of least impedance. This implies the path of least resistance for DC and the path of least inductance for AC
- Current flows in loops – the use of global ground precludes consideration of all effects of the return current
- The PDS and SDS are fully coupled and cannot as such be separated. Good design of both is needed to obtain system level integrity

Power Integrity
The Power Distribution Delivery Network

Aim of the Power Delivery Network

- Deliver a stable voltage to all devices
  - Stable is here defined as nominal voltage ± a certain percentage
  - The voltage variation is both due to IR voltage drop in the PDS, noise due to the switching activity and aging of components

$$\Delta V(\omega) = Z_{input}(\omega) I(\omega) + IR(\omega = 0)$$

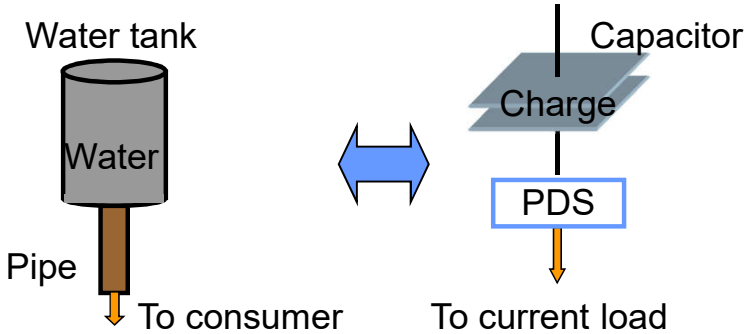
- Deliver required charge / current to all devices
- Provide a low impedance return path for signal currents

- Due to the technolgy trends (shrinking voltage levels, increasing power consumption, lower noise margin, faster IOs) the PDS impedance level decreases to ever smaller values and the requirements on the static losses tightens too.

Topology of the Power Delivery Network Components

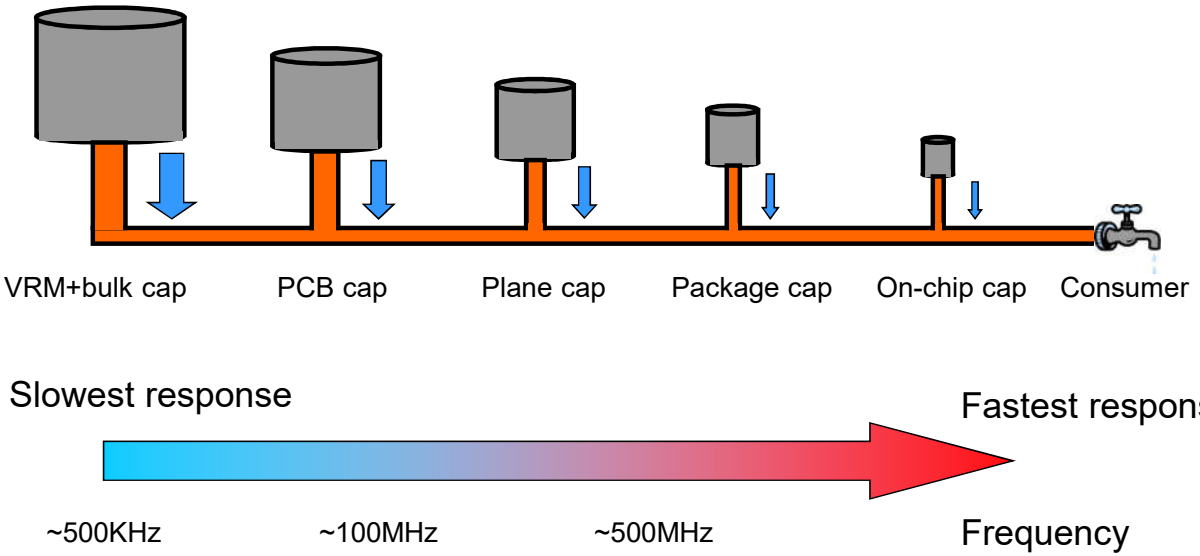
- What is delivering the charge to the ICs?

- Each PDN component acts as a local reservoir of charge.
- We can use a water supply as an analogy



- The different parts of the power delivery network have different response time to the current requirements of the loads

Topology of the Power Delivery Network Response Time

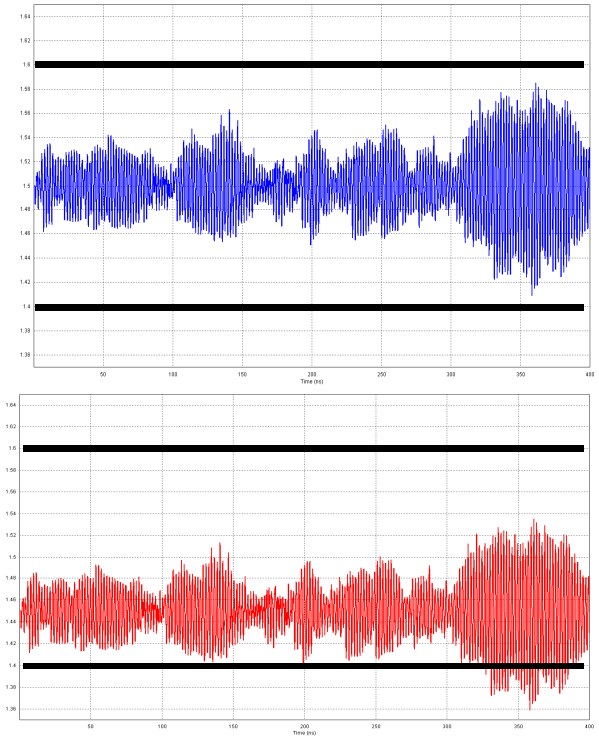


The power delivery network must be able to deliver, sufficiently fast, the required charge to the consumers. This translates into maintaining the input impedance of the PDN sufficiently low to keep down the induced noise due to switching events.

Illustration from [3]

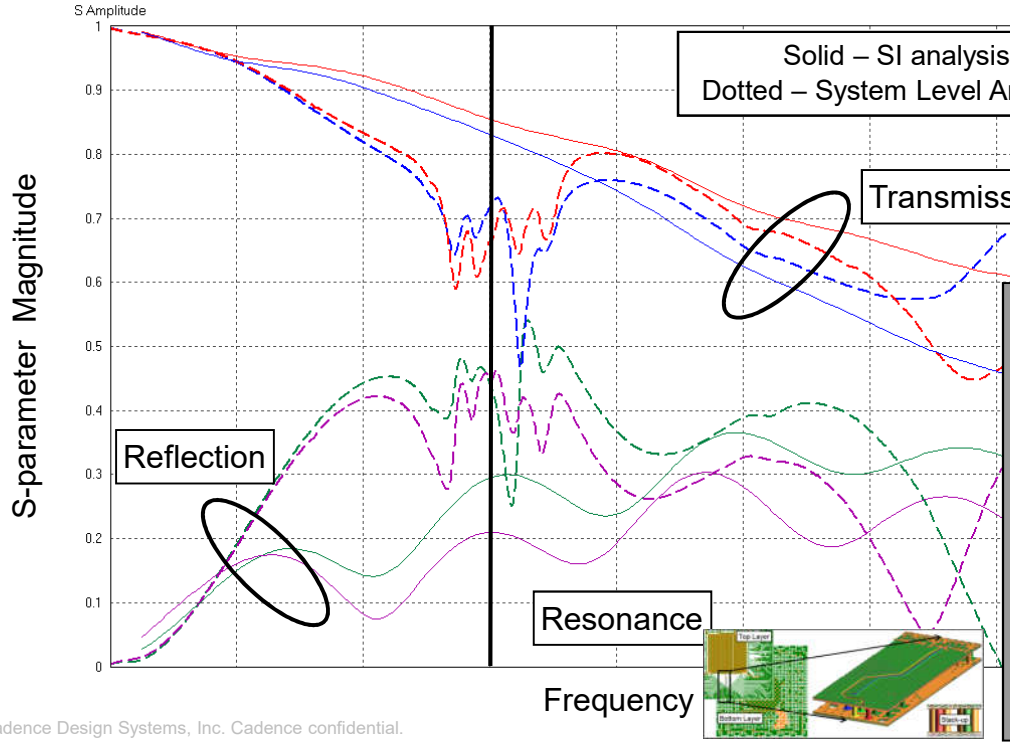
Topology of the Power Delivery Network DC aspects

- The VRM supplies charge at DC and must be able to deliver the total charge required by the loads
- Another requirement at DC is that the power delivery system must be able to handle the charge without introducing too much heating or excessive voltage drop
- These aspects become increasingly difficult to handle with the ever decreasing voltage levels and the associated increasing load currents
- In addition cost and sizing constraints leads to
  - Less layers and higher densities, reducing the available area for power nets
  - Antipads around vias perforate the planes and can overlap increasing plane parasitics
  - Complex geometries make analysis with hand calculations difficult, if not impossible



IR drop can cause system to exceed acceptable noise levels

Power Integrity and Signal Integrity
Two 10Gbps diff pair channels in a package



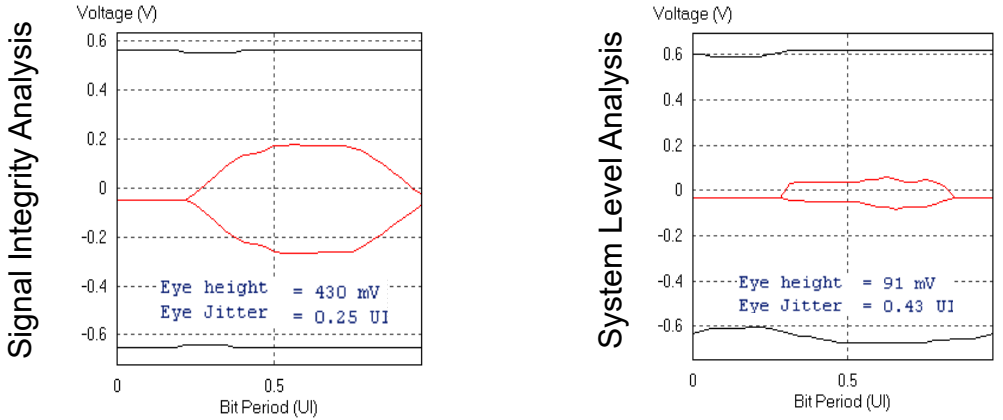
Attention:

A false sense of security is established if only circuit simulation is applied.

If 3D EM simulation is later applied as a "verification", this false sense of security can be reinforced if the full power planes are not included properly in the simulation.

Effect of Power Integrity Issue on SI

- Below shows the eye contours for the LVDS channel on the previous slide operating at 10Gbps



- The resonance of the power planes causes the voltage level difference between 0 & 1 to diminish (hence severly affected BER) and also shows significant jitter increase
- Power plane resonances can also severly affect performance of other devices in the system and can also cause emissions

Summary

- Signal integrity issues can be due to improperly handled power integrity → obtaining system integrity must encompass considerations of both signal integrity and power integrity

- Power integrity issues can occur when you have high current requirements, fast signals, have very dense routing or many voltage domains to handle or improperly selected decoupling

- Ground is a place for carrots and tomatoes

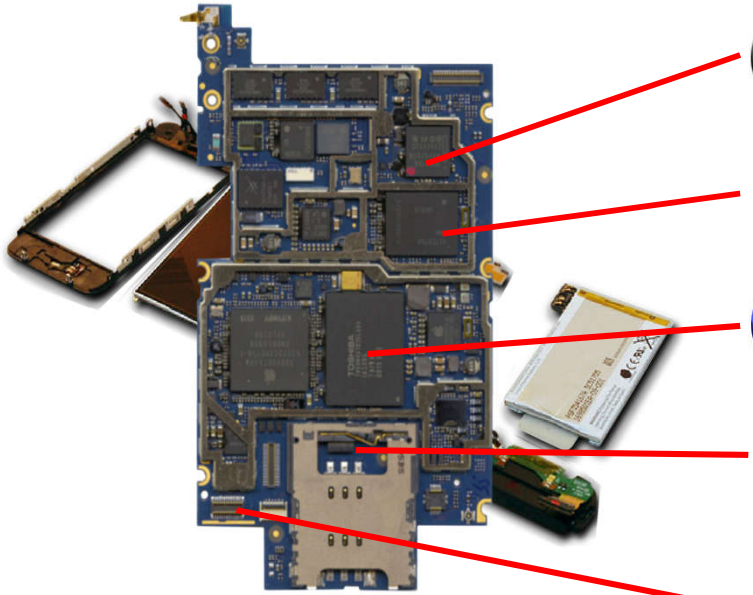
- Simulation tools that consider a fully coupled power and signal distribution system facilitate the most robust boards and package designs

Sigrity Technology Introduction

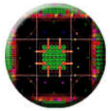
Introduction to Sigrity

- The leading signal and power integrity provider

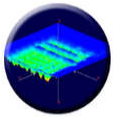
High-speed analysis and verification for PCBs and IC packages



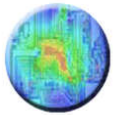
Decap Optimization
Assure power delivery performance constraints are met while targeting a decoupling scheme that is cost effective and conserves space



Silicon-Package-Board Modeling
Create ports for pins to achieve the desired level of abstraction when using models for either chip or system centric simulations



Co-design
Simultaneously simulate the entire chip power grid with the package/board in the time and frequency domain to find power issues that might be missed



EMI / EMC
Gain design stage visibility into potential hot spots with near and far field radiation studies to complement signal and power integrity analysis

High-speed interface analysis
Effectively deal with parallel (DDR) and serial (PCI-E) design challenges by analyzing system-wide behavior

Sigrity Power-Aware SI Products

Highlights

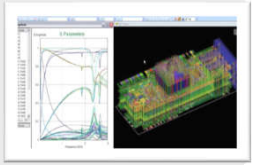
Power Aware IBIS model creation

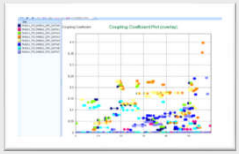
System Level SI Analysis

Detailed Board Level (P/G/S) extraction

PowerSI

- **PowerSI** is a virtual multi-port network analyzer applied to whole boards and packages to characterize all PI and SI effects
- Analyses supported: S-parameter(f), AC (f), Resonances, EMI(f), 3DFEM (f)

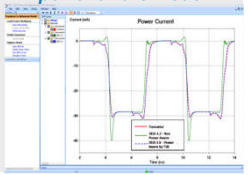




T2B

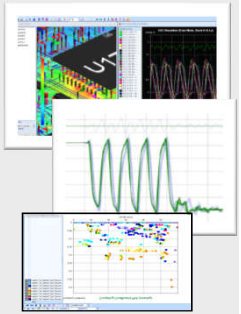
- Industry's most advanced tool for converting transistor models to IBIS
- Provides IBIS v5.0 power-aware model support
- Sigrity's IBIS plus model provides even more accuracy

Built-in simulation check compares transistor to IBIS power-aware model



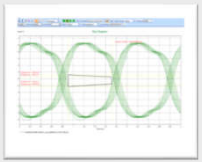
Speed2000

- Unique animation of transient field propagation across PCBs and packages
- Exceptional layout based signal integrity simulation including non-ideal power and ground systems
- Only solution for EMC simulation with non-linear drivers and receivers



SystemSI -PBA

- For the accurate assessment of high-speed chip-to-chip system designs.
- **SystemSI Parallel Bus Analysis**' end to end solution targets source-synchronous parallel interfaces such as designs with DDRx memory.



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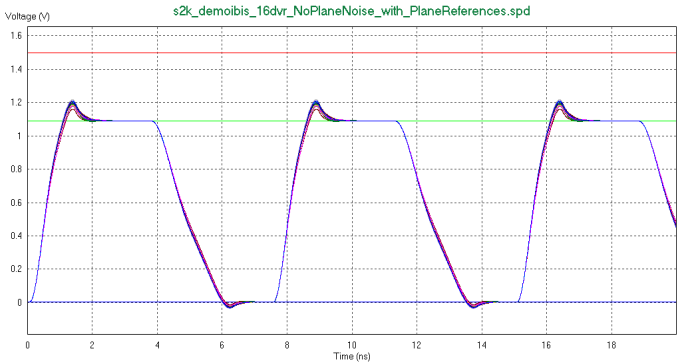
Sigrity Power Aware SI Technology

Sigrity Power-Aware SI Technology

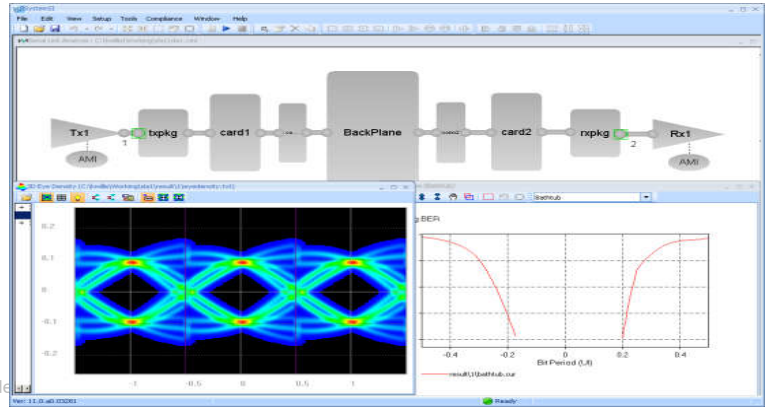
- Signal integrity analysis has traditionally been performed assuming ideal power
- With today's data rates and tight margins, this has become a bad assumption
- Modeling the PDN together with the signals give much more accurate behavior
- This requires very efficient extraction, at which Sigrity excels



Sigrity Serial Link SI Technology

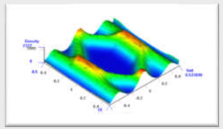
Highlights

- IBIS-AMI Model Creation
- System Level SI Analysis
  - Advanced channel simulation with algorithmic (IBIS-AMI) equalization modeling (ex. FFE, DFE ..)
  - Automated eye diagram and bathtub generation for BER
- Detailed Board Level (P/G/S) extraction
  Hybrid and Full-wave interconnect extraction



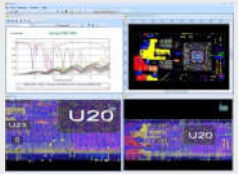
SystemSI – SLA

- **SystemSI Serial Link Analysis** is an award-winning chip-to-chip analysis solution focuses on high-speed SerDes designs such as PCIe, HDMI, SFP+, Xaui, Infiniband, SAS, SATA, USB, and more.

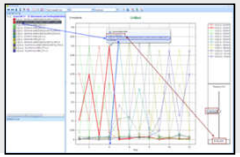


PowerSI

- Market leader and product of choice of companies where power integrity is essential
- Highly accurate modeling of layout structures
- Ability to handle general n-terminal component models

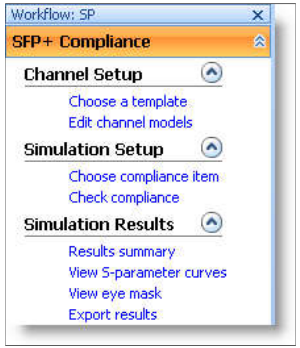


Frequency domain SI, PI and EMC



Compliance Sign-Off Flow

Workflow



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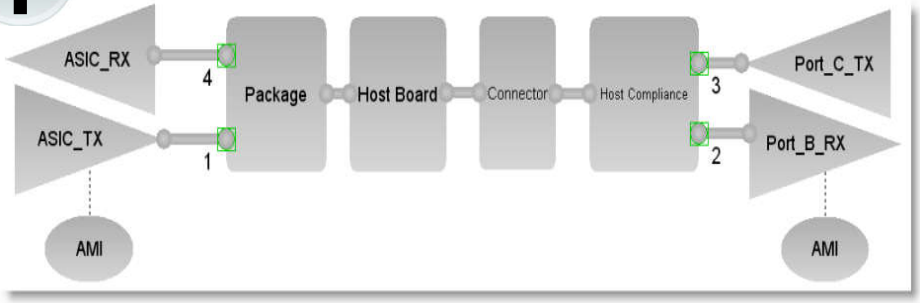


2

Choose compliance item

No.	Parameter	Symbol	
Host Transmitter Output Specification at B (table 11 in SFP+ spec.)			
1	Termination Mismatch at 1MHz	DZ_{tx}	☐
2	Differential Output S-parameter	SDD22	☐
	Common Mode Output S-parameter	SCC22	
Host Transmitter Output Jitter and Eye Mask Specification at B (table 12 in SFP+ spec.)			
3	Signal Rise/Fall Time (20% to 80%)	Tr, Tf	☐
4	Total Jitter	TJ	☐
5	Data Dependent Jitter	DDJ	☐
	Data Dependent Pulse Width Shrinkage	DDPWS	
6	Uncorrelated Jitter	UJ	☐
7	Transmitter Qsq	Qsq	☐
8	Eye Mask	Eye Mask	☐
Host Receiver Input Specification at C (table 13 in SFP+ spec.)			
9	Differential Input S-parameter	SDD11	☐
	Reflected Differential to Common Mode Conversion	SCD11	
SFI Channel Transfer Recommendation (table 25 in SFP+ spec.)			
10	Channel Transfer from chip pad to point B or C	SDD21	☐
Additional SFI Channel Recommendations			
11	SFI Channel Return Loss	SDD11, SDD22	☐
12	SFI Channel Ripple	Ripple	☐
SFP+ Host Output Specification at B for Cu (table 33 in SFP+ spec.)			
13	Voltage Modulation Amplitude(p-p)	VMA	☐
14	Transmitter Qsq	Qsq	☐
15	Host Output TWDPc	TWDPc	☐

3

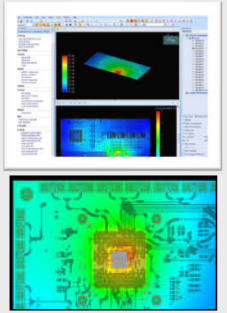
Sigrity Power Integrity Technology

Highlights

- Frequency Domain AC Analysis
- DC Analysis (IR Drop)
- Decoupling Capacitor Optimization
- Layout thermal analysis

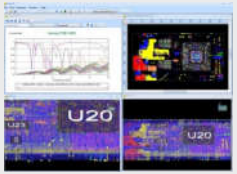
PowerDC

- Industry unique integrated and automated electrical and thermal co-simulation for PCBs and packages
- Patented time saving automation for remote sense line positioning
- Fastest and most accurate IR drop solution

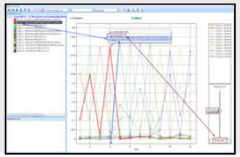


PowerSI

- Market leader and product of choice of companies where power integrity is essential
- Highly accurate modeling of layout structures
- Ability to handle general n-terminal component models

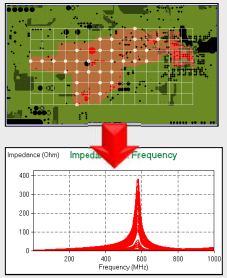


Frequency domain SI, PI and EMC



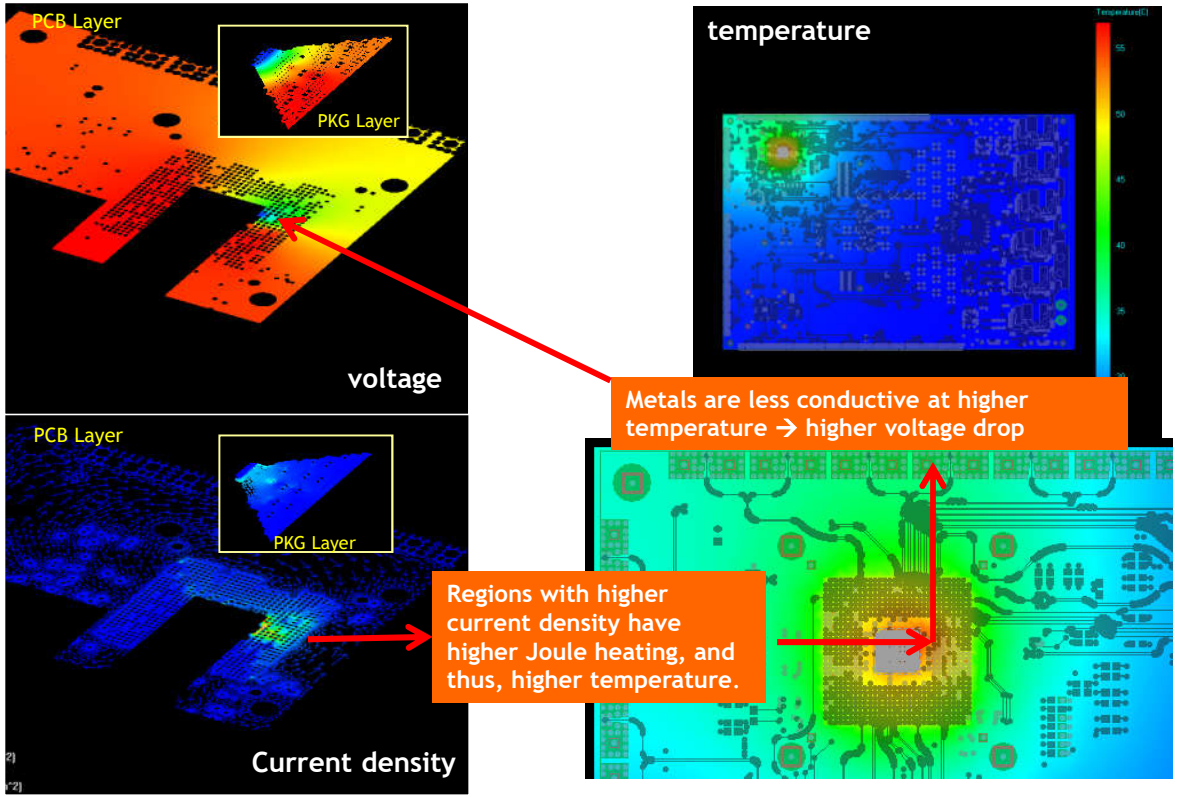
OptimizePI

- Automated decap optimization and verification features
- Clear presentation of economic benefits from decap optimization
- Flexibility in meeting targeted objectives (performance, cost, area …)



Automated positioning of EMI decaps

Voltage, current density and temperature distributions – By PowerDC



Package Assessment and Extraction

Highlights

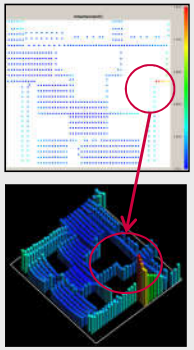
- Easy to use Package Assessment
- Hybrid Solver technology
  - Fast and accurate for gigabit frequencies
- 3D Full Wave Solver
  - Easy to use, accurate and low and high frequency, faster than alternative Full Wave offerings

"We began using XtractIM nearly two years ago and it quickly became our primary RLGC model extraction solution. We are pleased with the accuracy of XtractIM models and very impressed with the dramatic analysis time speed-ups we experienced relative to previous tools."

- Hong Shi Altera

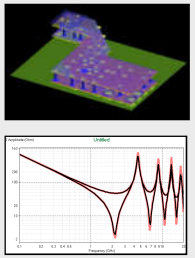
XtractIM

- Built in package assessment rapidly identifies potential package defects
- Unsurpassed extraction speed and ease of use
- Able to address the broadest range of packages (single die & multi-die; flip chip, wirebond & leadframe)



PowerSI – 3D FEM

- Much faster (often 10x vs HFSS) with comparable accuracy
- Highly accurate low frequency solution (ex. lower than few MHz)
- Easy to use with geometry modeling and automated port setup

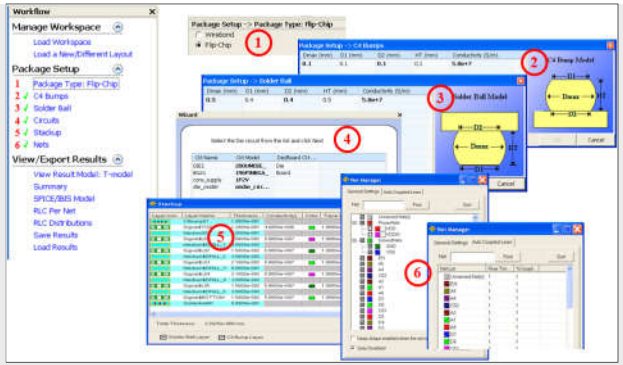


Differential pair in 6 layer package Results showing correlation with HFSS

Package Assessment and Extraction
- XtractIM

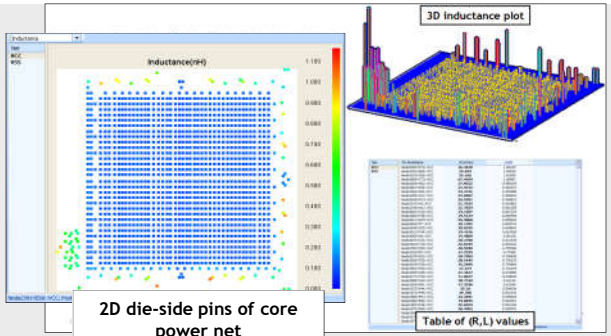
Package Extraction with XtractIM

- 10X – 100X Greater Extraction Speed and Capacity
- Whole-package, All-nets , Accurate AC Analysis Engine
- HTML Sign-off Reports



Package Assessment with XtractIM

- Electrical Performance Assessment
  - "**assessment**" – a judgment about something based on an understanding of the situation
  - "**extraction**" – to obtain something from a source, usually by separating it from other material



2D die-side pins of core power net
1500(+) die pins per net

Sigrity Tool Integration – PCB/Package Domain

- The Sigrity tools are today being integrated more and more within the Cadence design environment, some examples:
  - Embedded impedance, crosstalk and discontinuity checks for signals
  - Static IR drop analysis with constraint violation DRC embedded in the layout
  - Power Integrity constraint set development
  - Decoupling capacitor BOM optimization with back annotation to Allegro
  - Differential via structure optimization
  - Virtual reference design kits for various interfaces

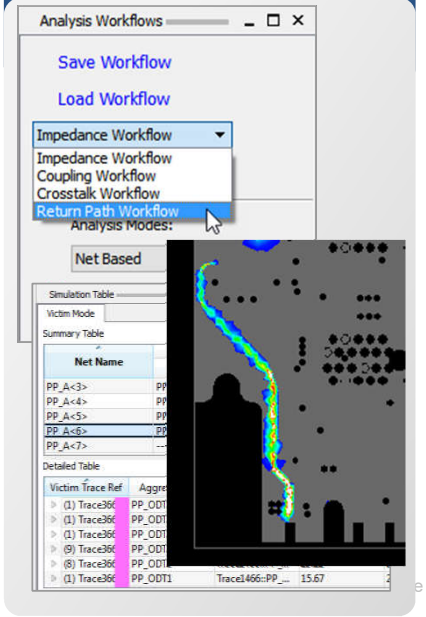
- The Sigrity tools can also be used as stand-alone tools for Cadence and 3rd party based design environments

Allegro Integration Example

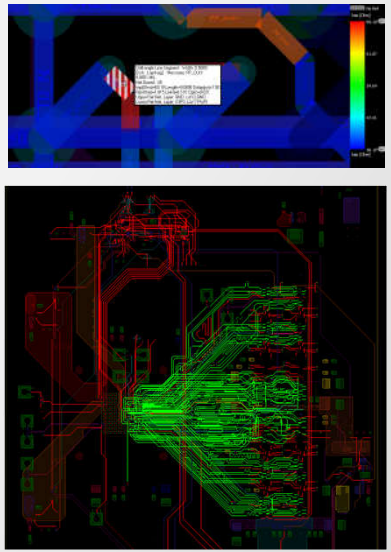
Impedance, Coupling, Return Path Checks and More

- New unique environment blending the best of Allegro and Sigrity technology
  - All within an Allegro framework – layout based analysis / checking for the entire design team
    - Rules for SI / PI / EMI with Constraint Manager as single cockpit for all rule checking

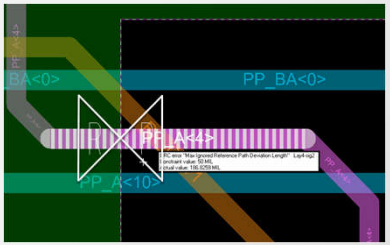
Analysis

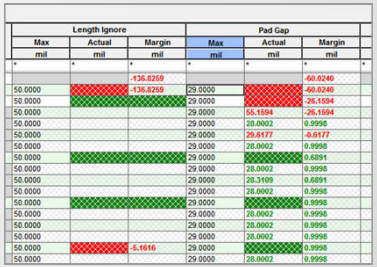


Visions



Advanced ERCs





cadence

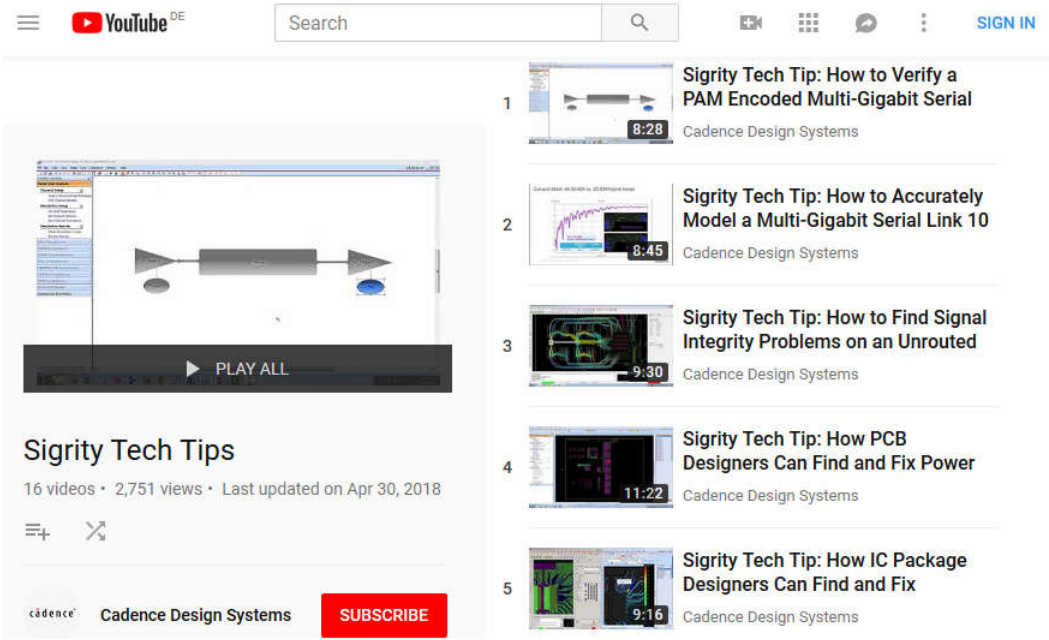
Summary

Summary

- An extensive tool set is now available to IN2P3 for addressing PCB, package and system integration challenges
- The Sigrity toolset helps provide valuable insights into the design behavior with respect to debugging signal integrity, power integrity, noise coupling issues and EMC/EMI
- In addition the Sigrity technology have been integrated into Allegro to make it easier to implement and check high speed design rules

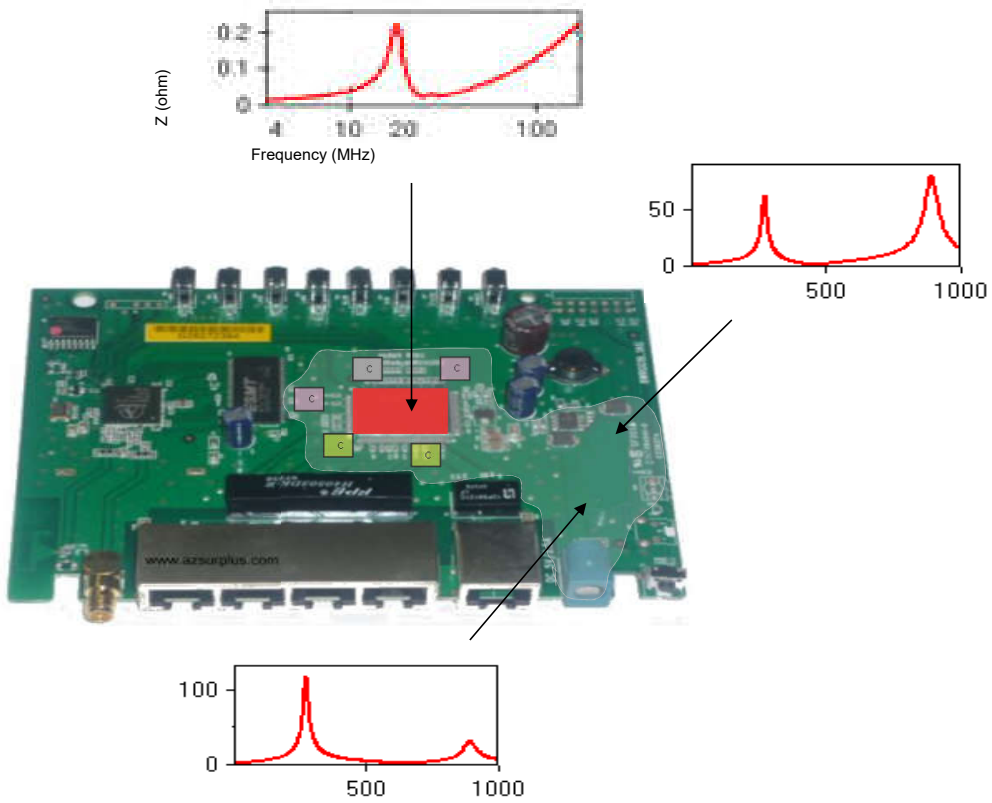
Finding more information

- Several videos on the Sigrity technology available on our YouTube channel
  - https://www.youtube.com/playlist?list=PLYdInKVfi0KbIE3evL5lzy6qkruGfU_N2
- SI and PI Blog
  - https://community.cadence.com/cadence_blogs_8/b/spi/
- Cadence Training
  - On-site training, scheduled classes
  - Internet learning services

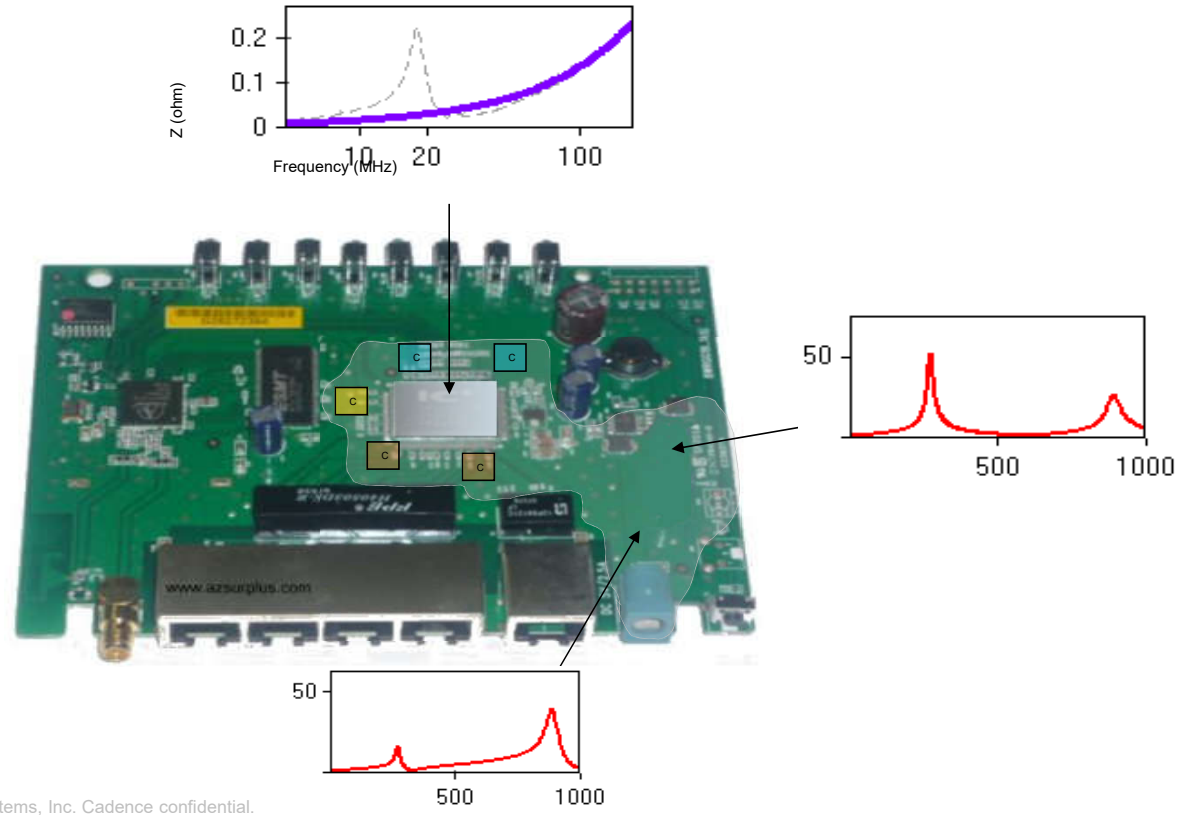


Device and Board Level Resonances

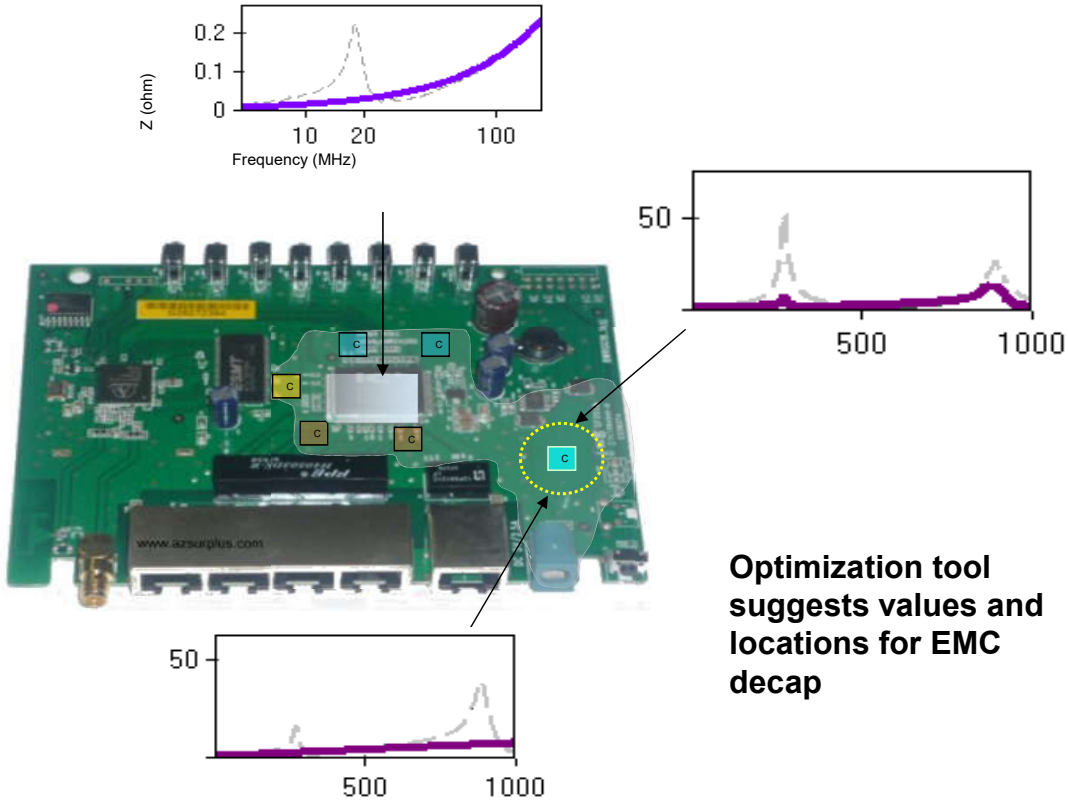
System Input Impedance



Device Focused Optimization



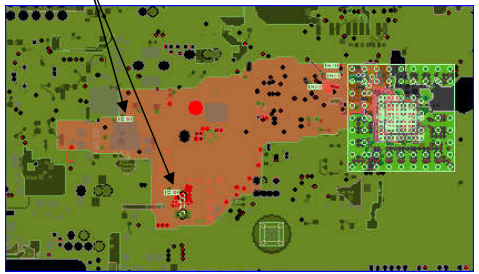
Device and EMI Co-Optimization Results



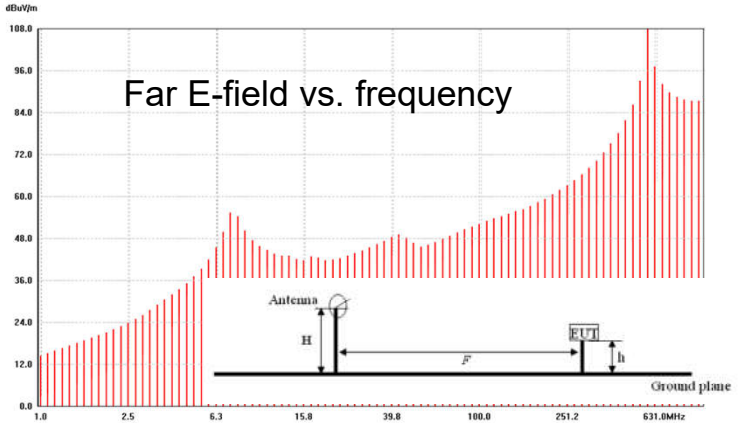
Optimization tool suggests values and locations for EMC decap

Radiation Before Adding 2 EMC Plane Capacitors

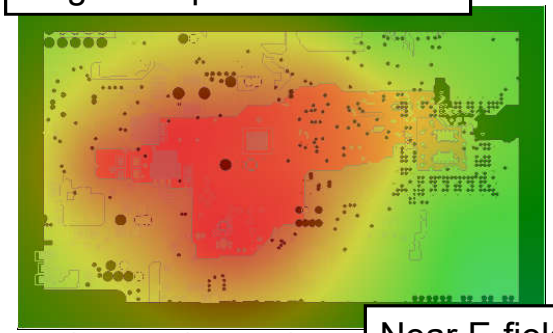
2 capacitor locations identified for lowering EMC – not mounted

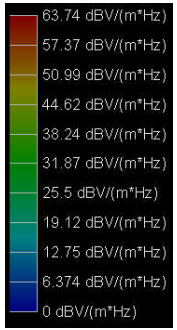


AC=1 source at the device



Original capacitor selection

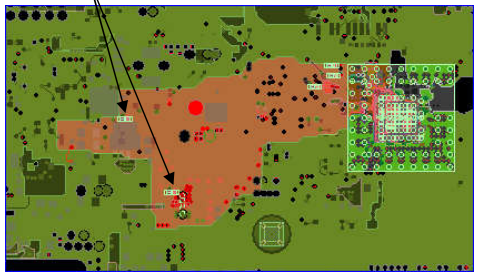




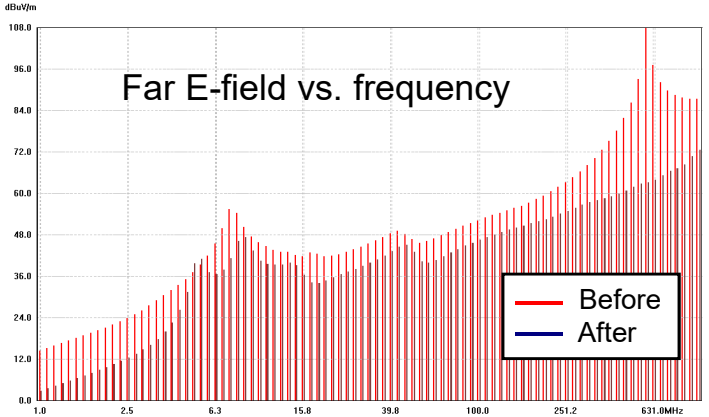
Near E-field at 580MHz
scale on the right

Radiation Before/After Adding 2 EMC Capacitors

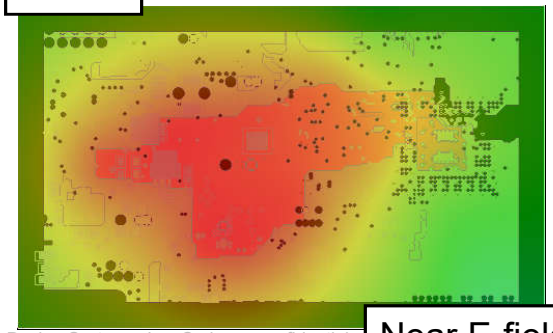
2 added EMC capacitors (100nF)



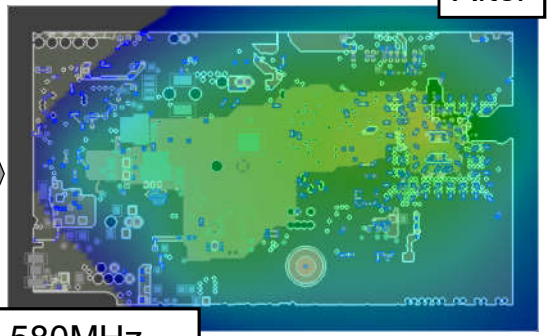
AC=1 source at the device

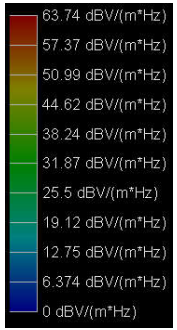


Before



After





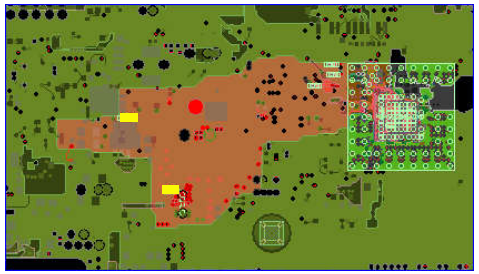
Near E-field at 580MHz

same scale for each plot

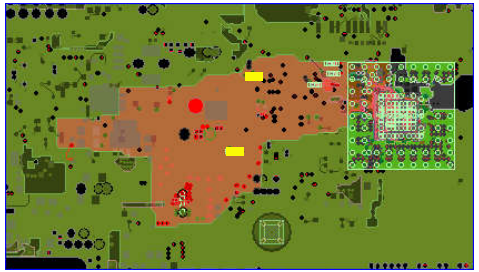
cadence

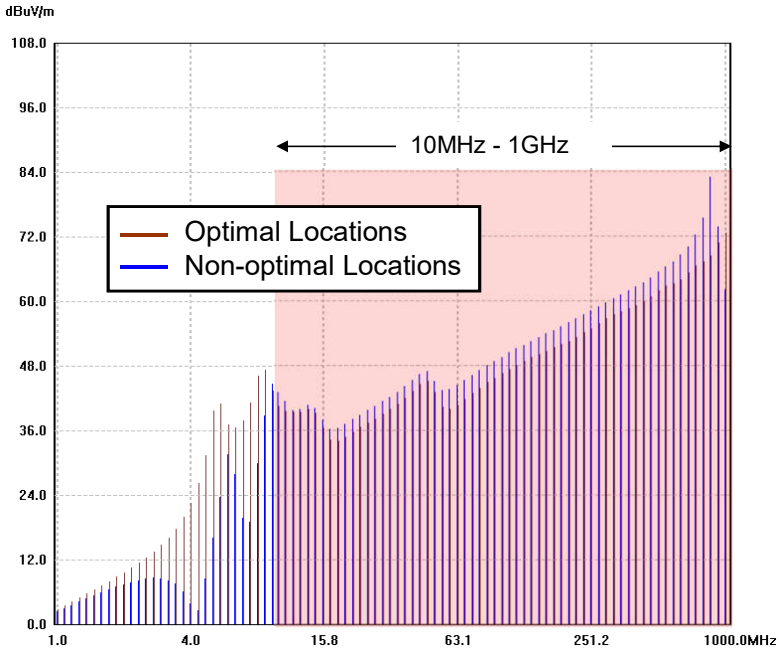
What if: 2 100nF Capacitors Placed at Other Locations

2 Locations suggested by OptimizePI



2 Other Locations

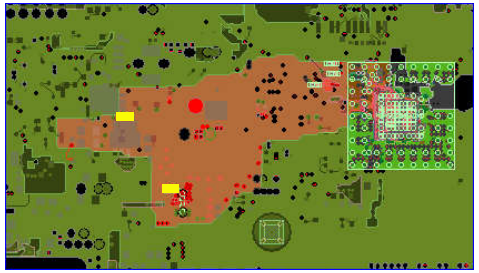




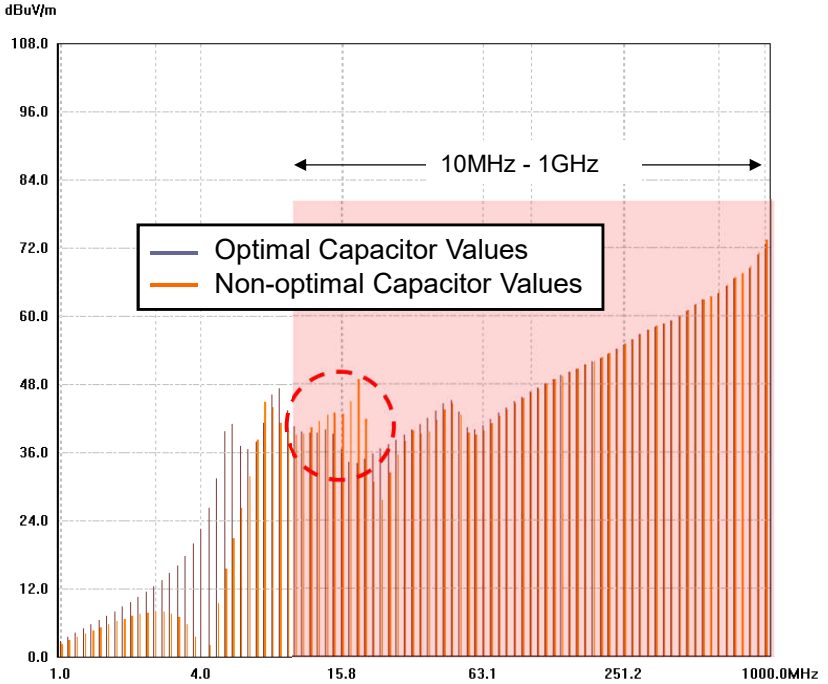
Non-optimal decap locations cause more radiation above 16MHz.

What if: Optimal Locations Populated With Different Capacitors Values

2 @ 100nF emicaps suggested by OptimizePI



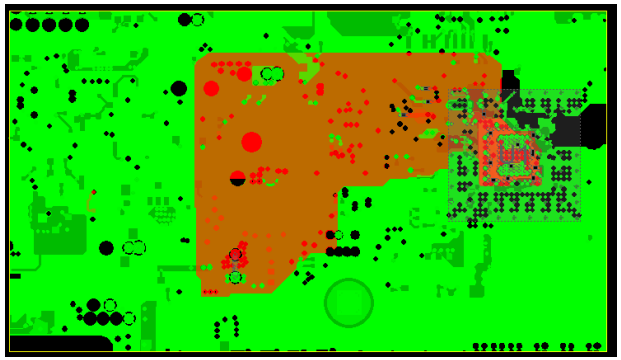
2 @ 10nF emicaps in the same locations

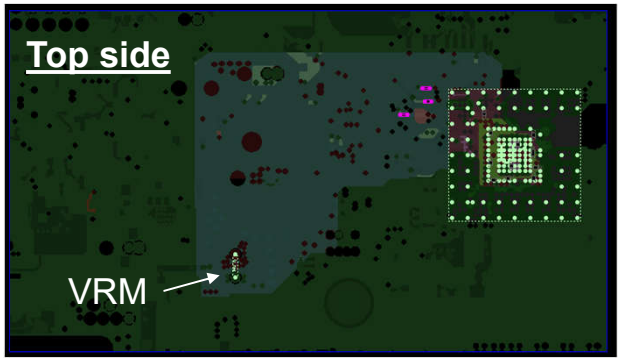


Non-optimal capacitor values cause more radiation between 10MHz - 30MHz.

Input Impedance, Noise Coupling, Near and Far Fields

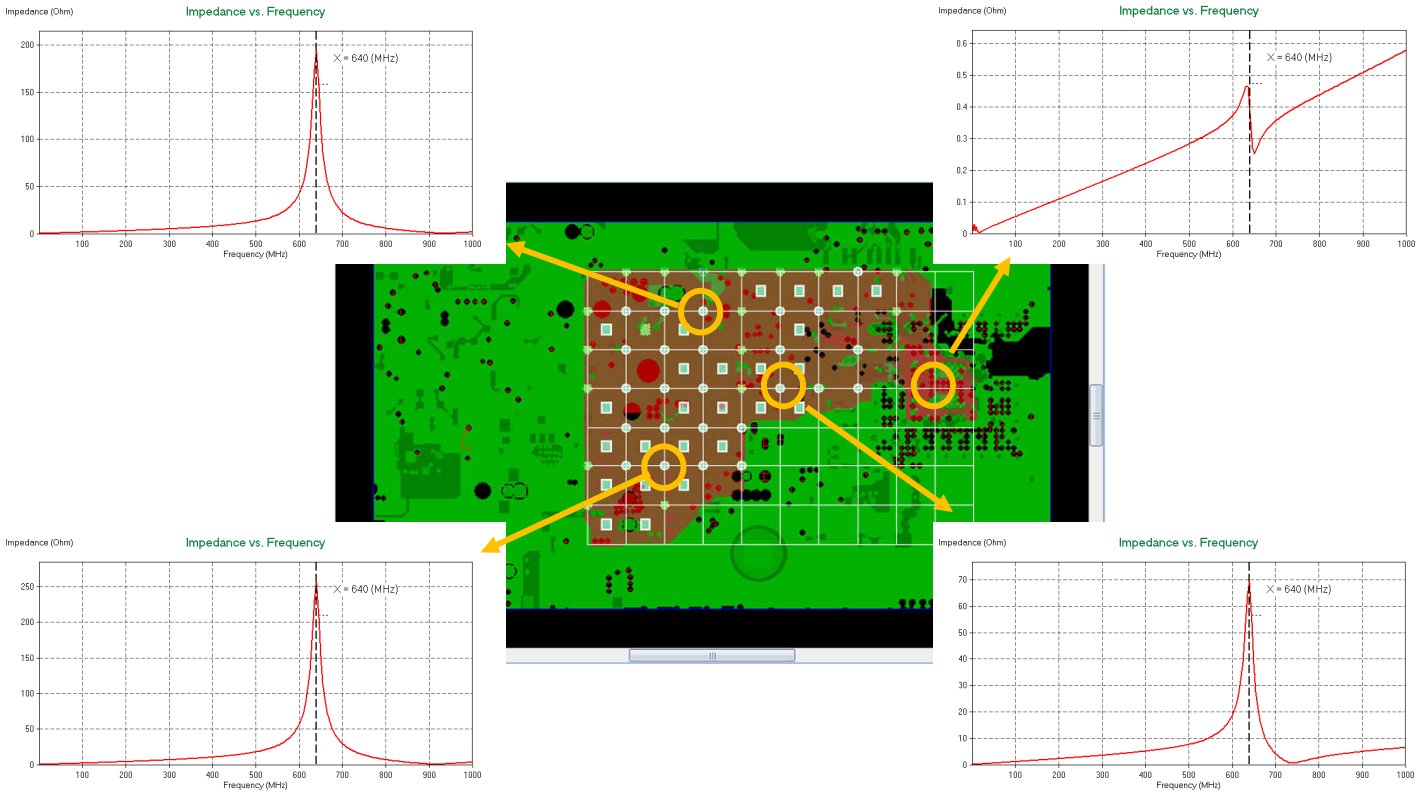
Example Database





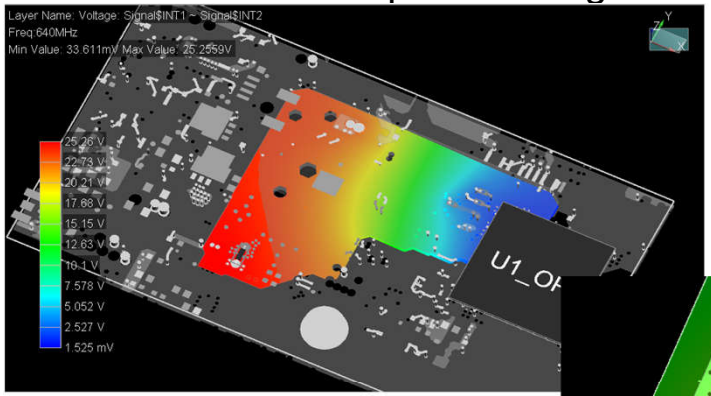
- 14 device decaps
  - 3 same side
  - 11 in core area
- Impedance profile shows peaking at ~640MHz

Impedance Profile For Device Decoupled PCB

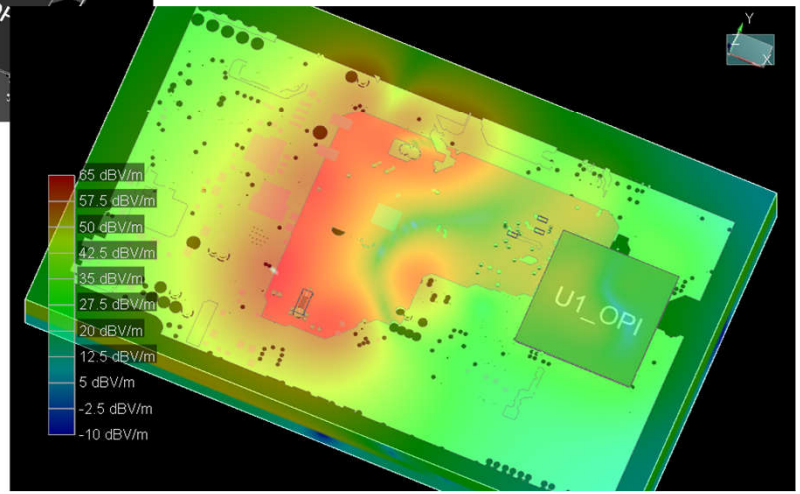


Near-Field and Plane Noise Distribution @ 640MHz

Noise voltage distribution between power and ground

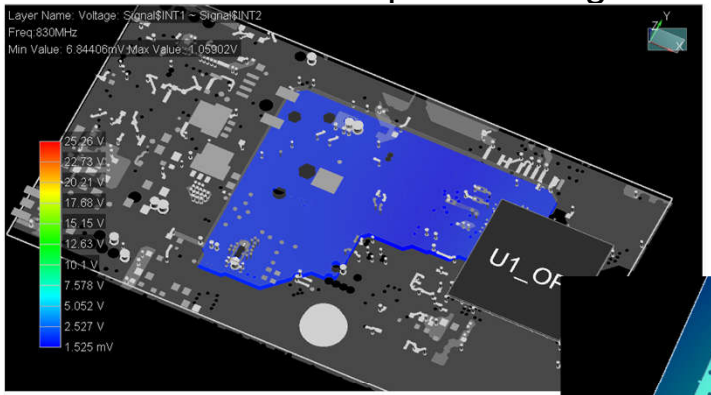


E-Field Distribution

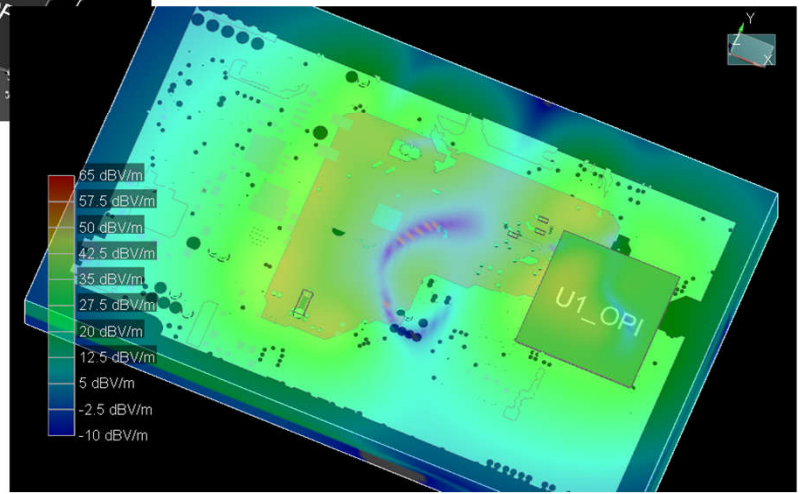


Near-Field and Plane Noise Distribution @ 830MHz

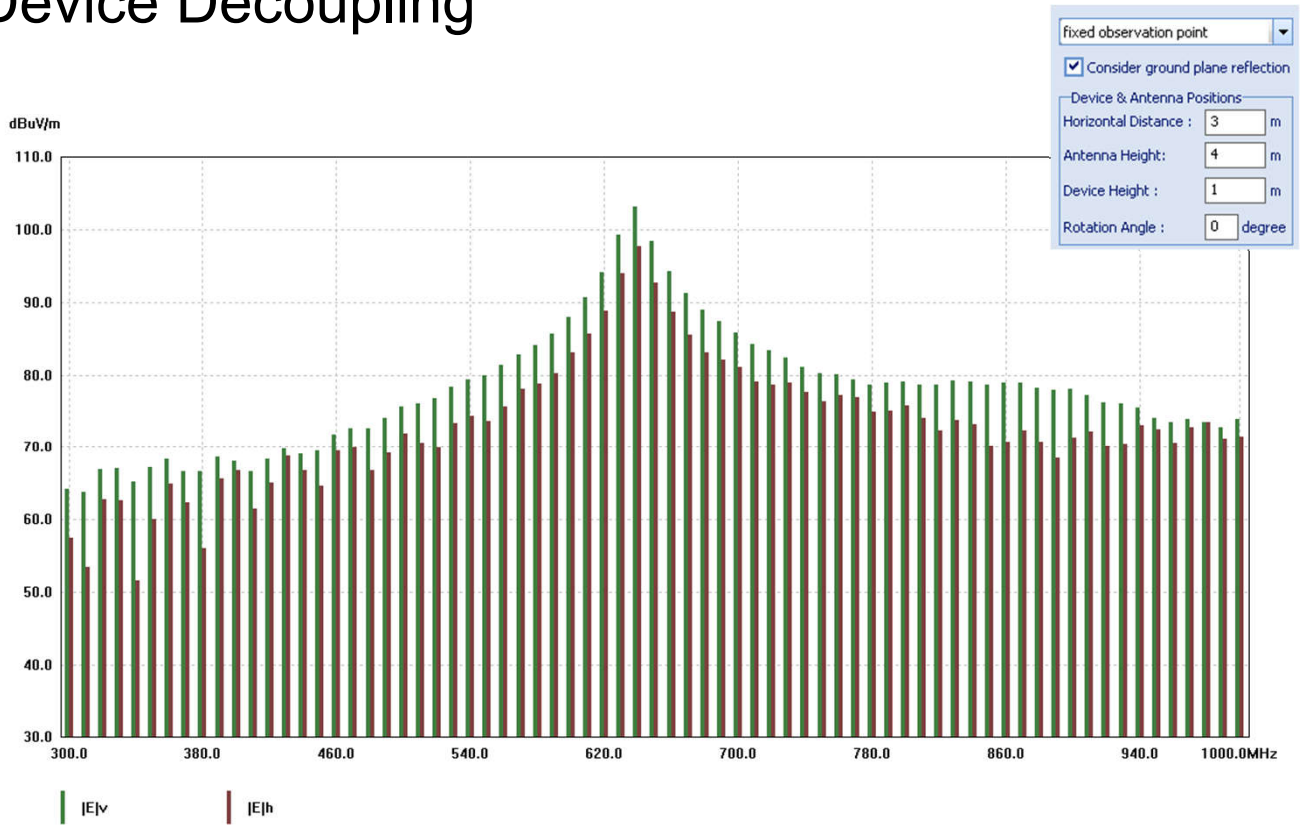
Noise voltage distribution between power and ground



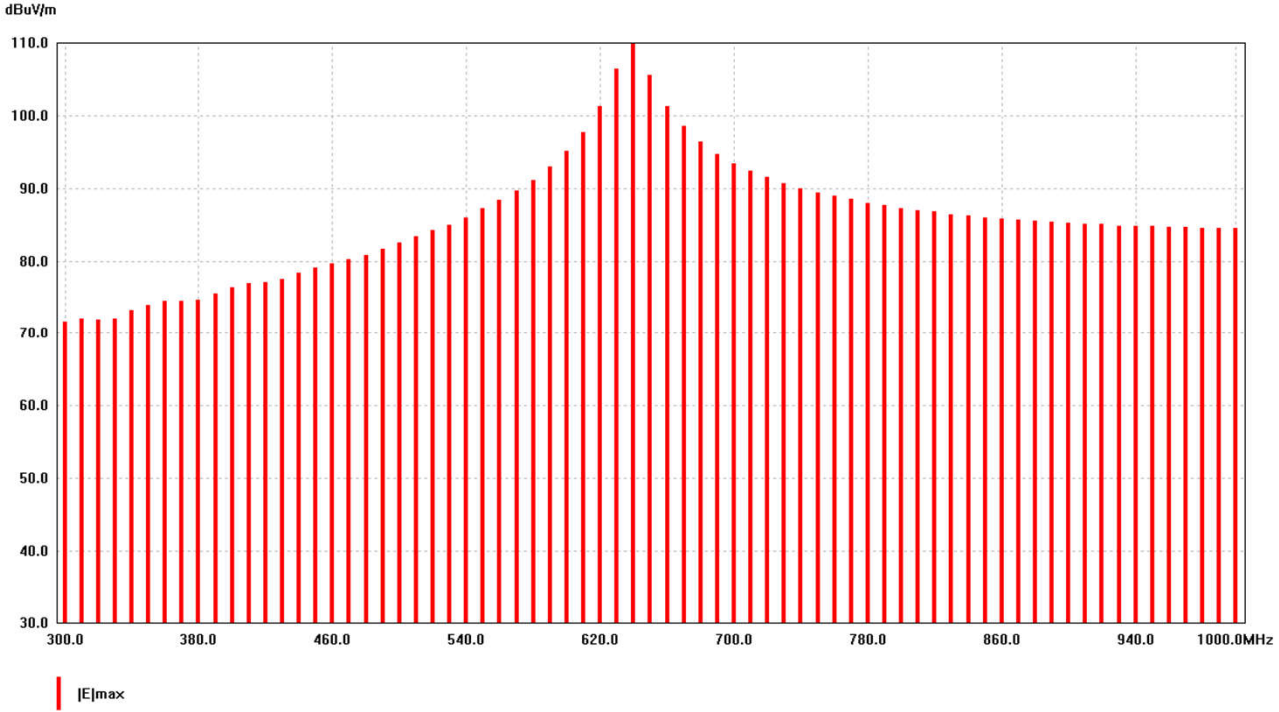
E-Field Distribution



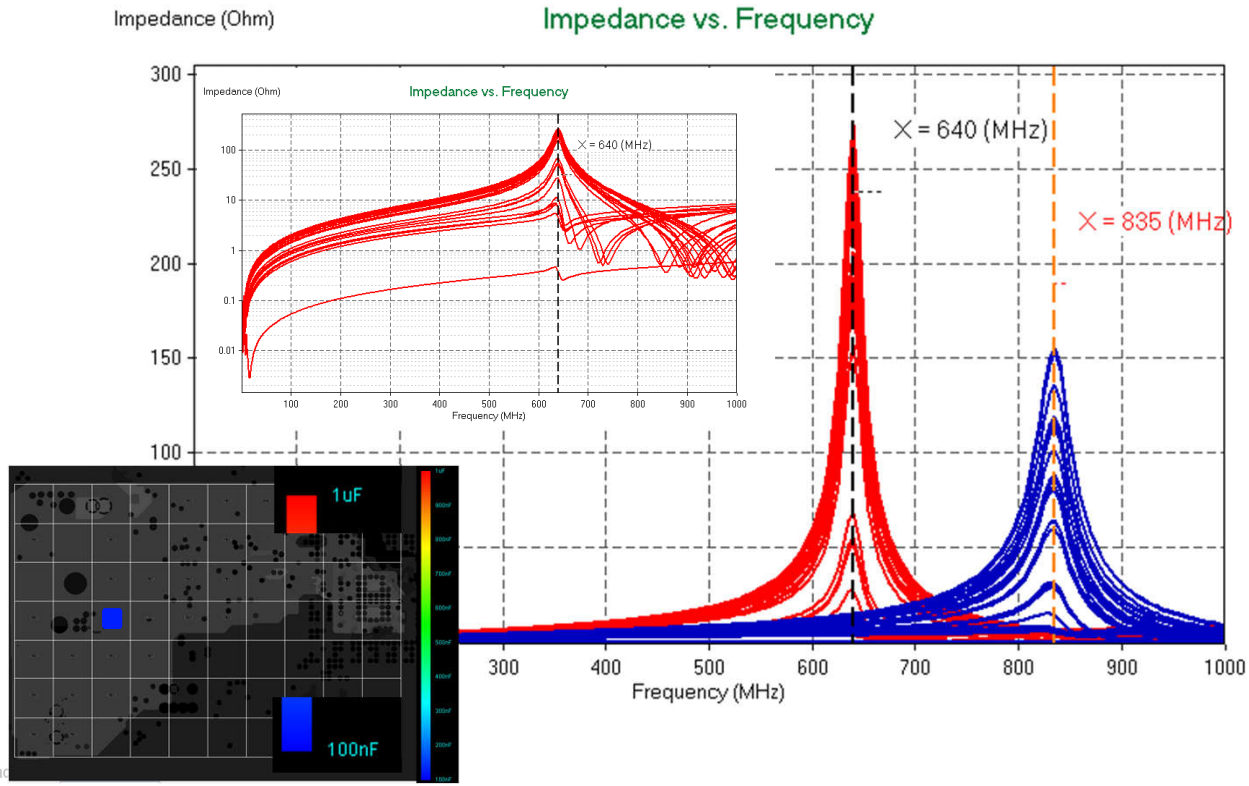
EMC Measurement Setup, Fixed Position
Original Device Decoupling



EMC Measurement Setup, Worst Case
Original Device Decoupling

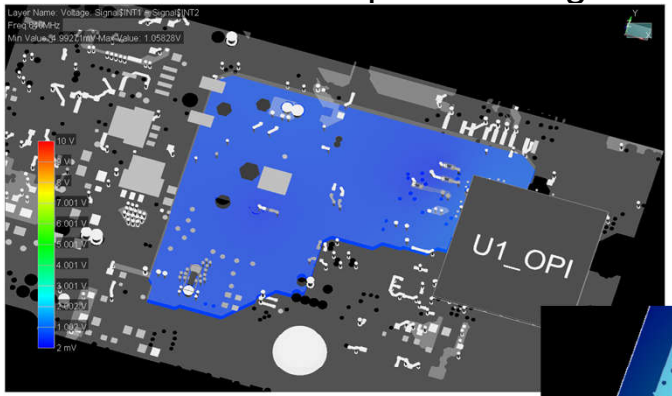


1 Capacitor Placed (1x100nF)

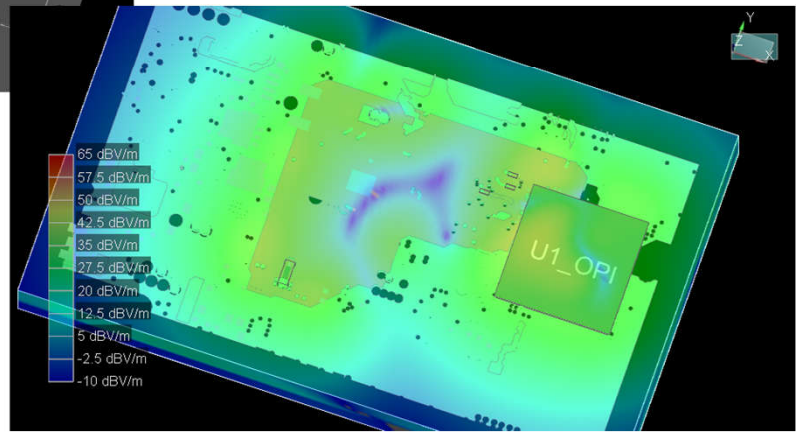


Near-Field and Plane Noise Distribution @ 640MHz

Noise voltage distribution between power and ground

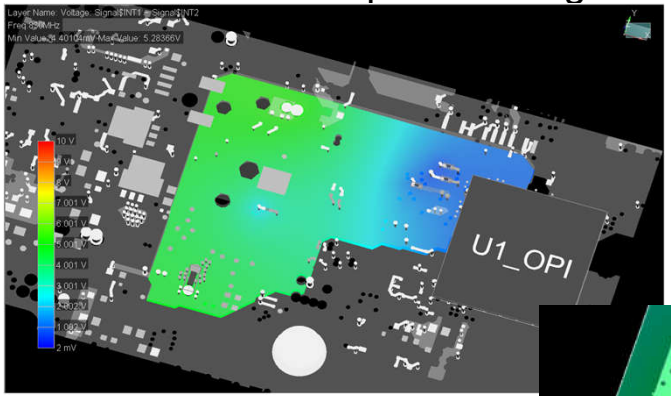


E-Field Distribution

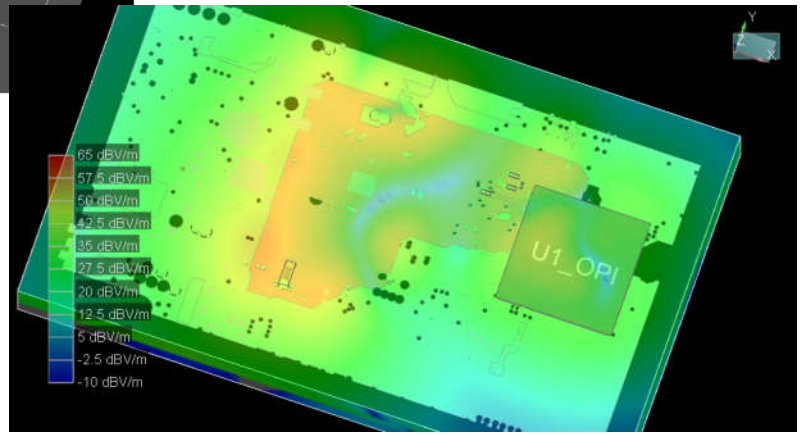


Near-Field and Plane Noise Distribution @ 830MHz

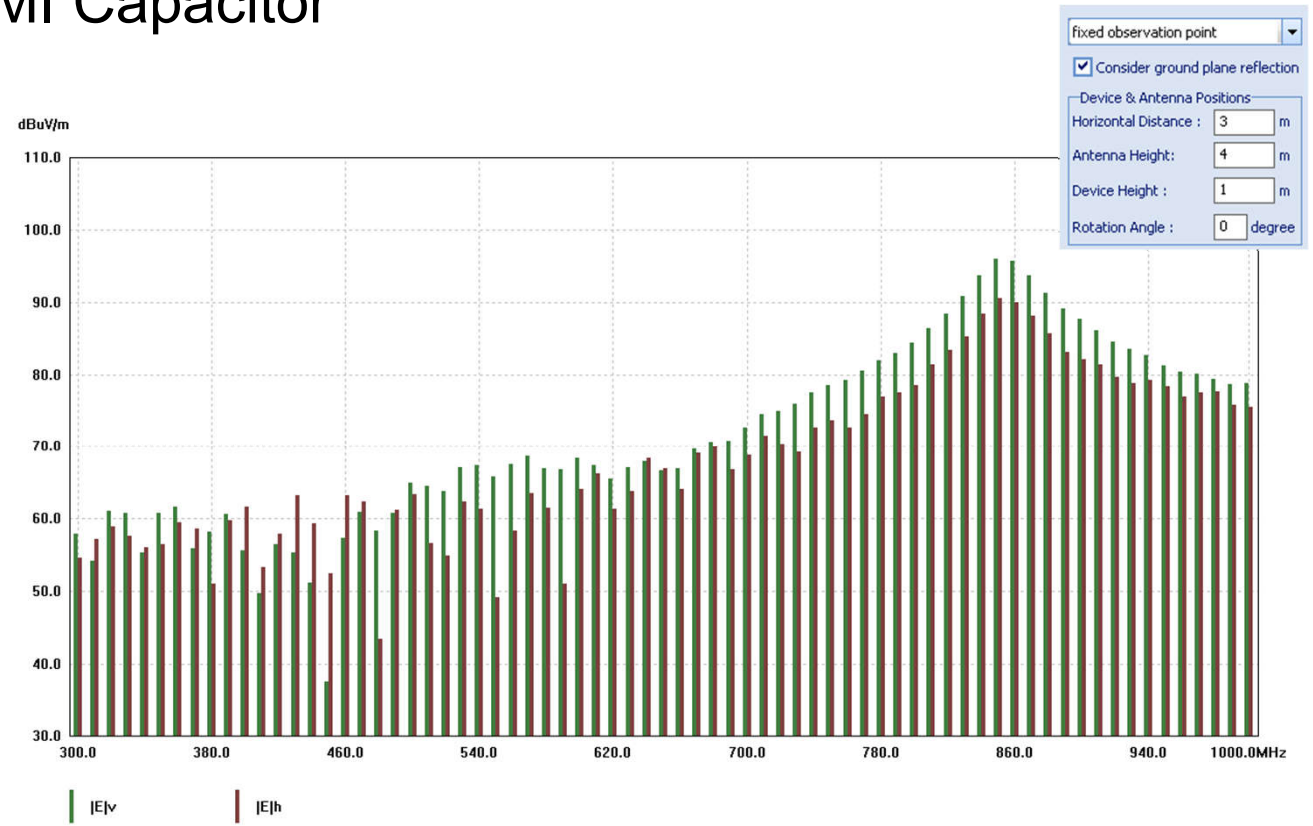
Noise voltage distribution between power and ground



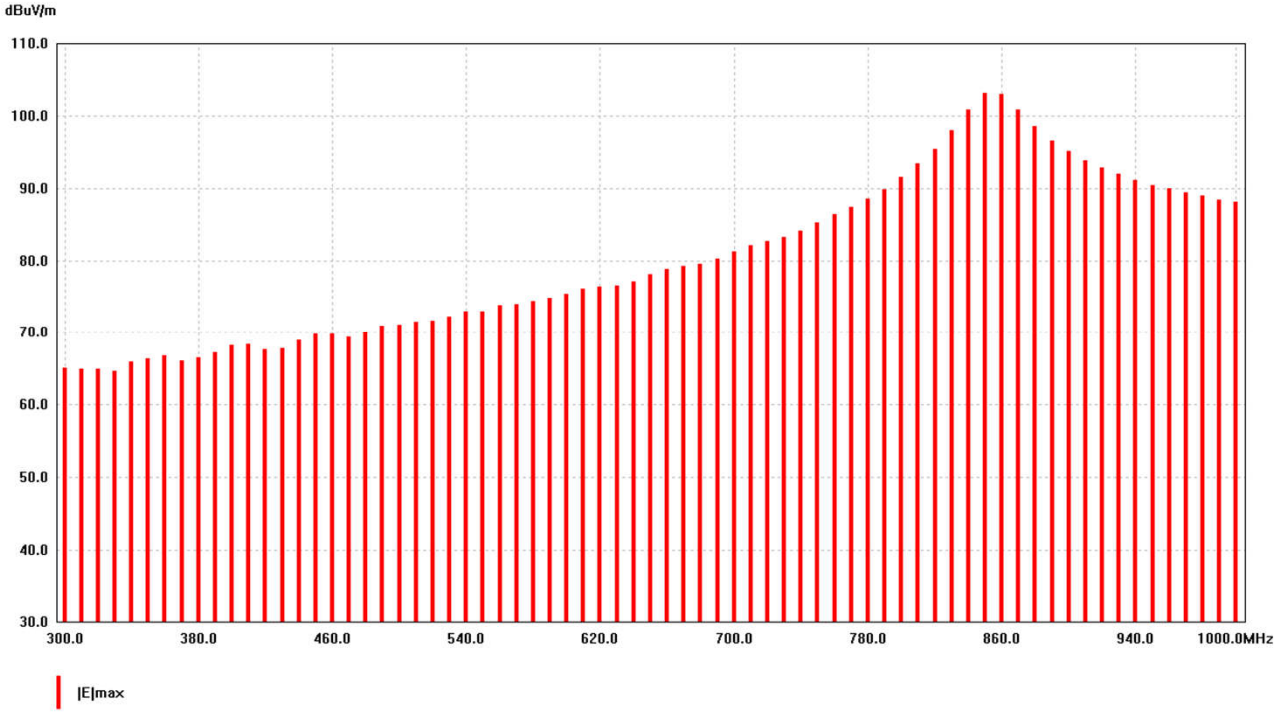
E-Field Distribution



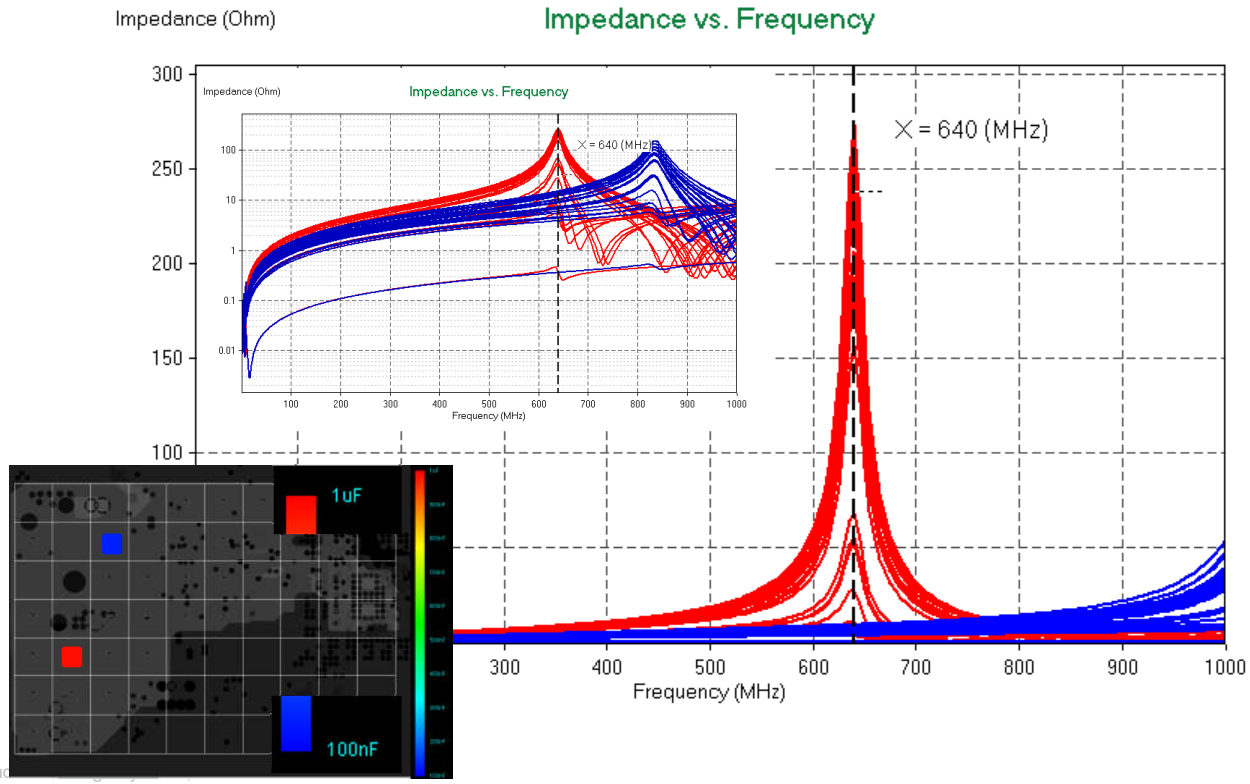
EMC Measurement Setup, Fixed Position With 1 EMI Capacitor



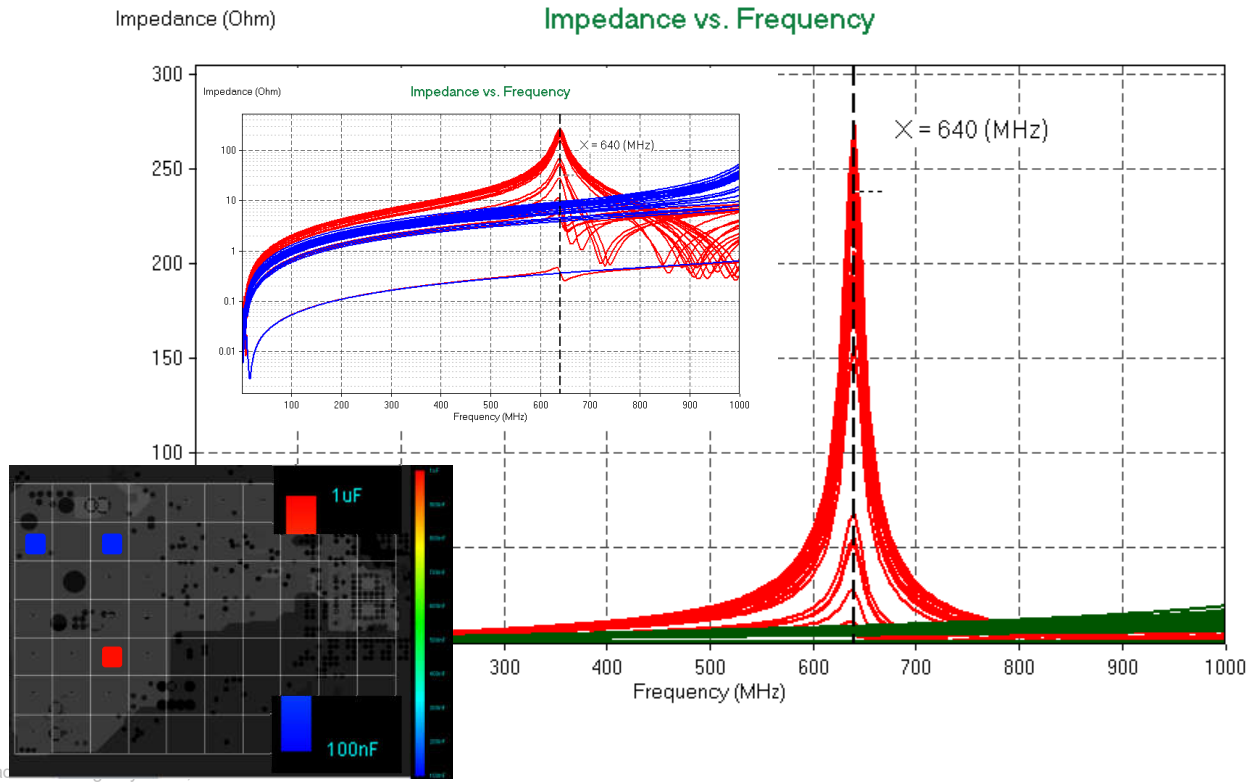
EMC Measurement Setup, Worst Case With 1 EMI Capacitor



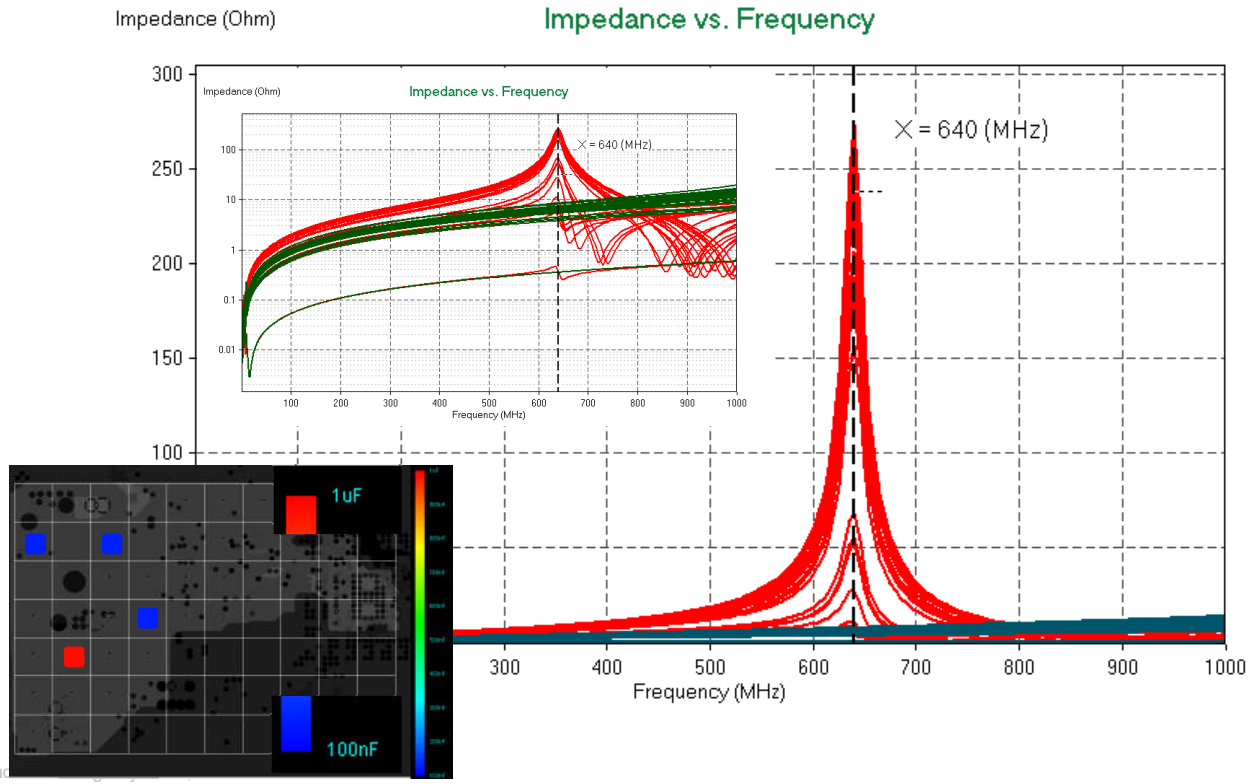
2 Capacitors Placed (1x100nF, 1x1000nF)



3 Capacitors Placed (2x100nF, 1x1000nF)



4 Capacitors Placed (3x100nF, 1x1000nF)

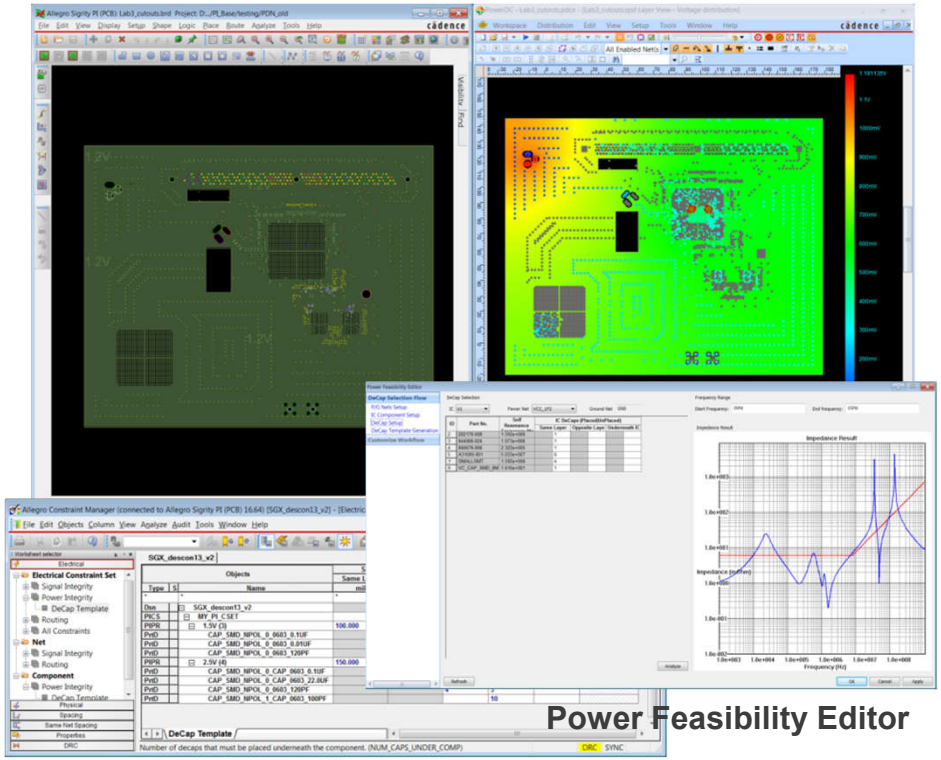


Sigrity Product Summaries

Allegro Sigrity PI Base

Floorplanner

DC Analysis



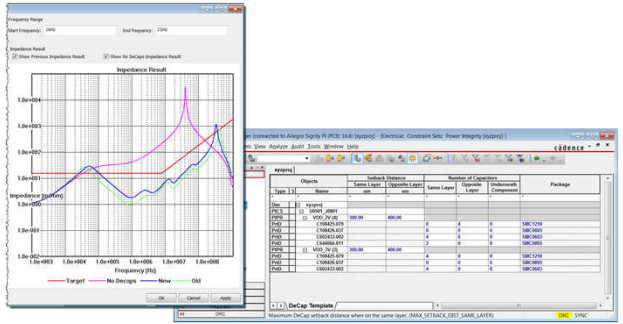
Power Feasibility Editor

Constraint Manager

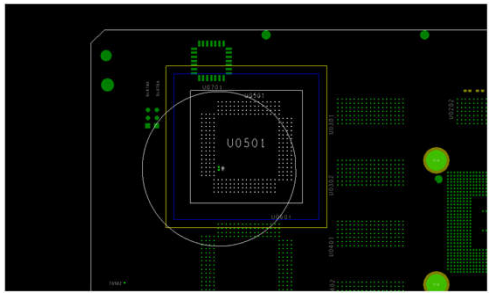
Allegro Sigrity PI Base integrates Allegro and Sigrity technology for PI analysis of PCB, IC Package and SiP designs. Enables constraint driven design with an integrated layout and analysis solution.

Allegro Sigrity PI Base Primary Advantages

- ✓Proven Sigrity analysis engines
- ✓Industry's first constraint-driven PI design process to drive DeCap selection and placement
- ✓Automated crossprobing configuration after DC Analysis to easily identify and resolve IR drop issues in physical layout
- ✓Targeted for layout designers and PI engineers
- ✓Add-on options for detailed analysis, compliance and assessment

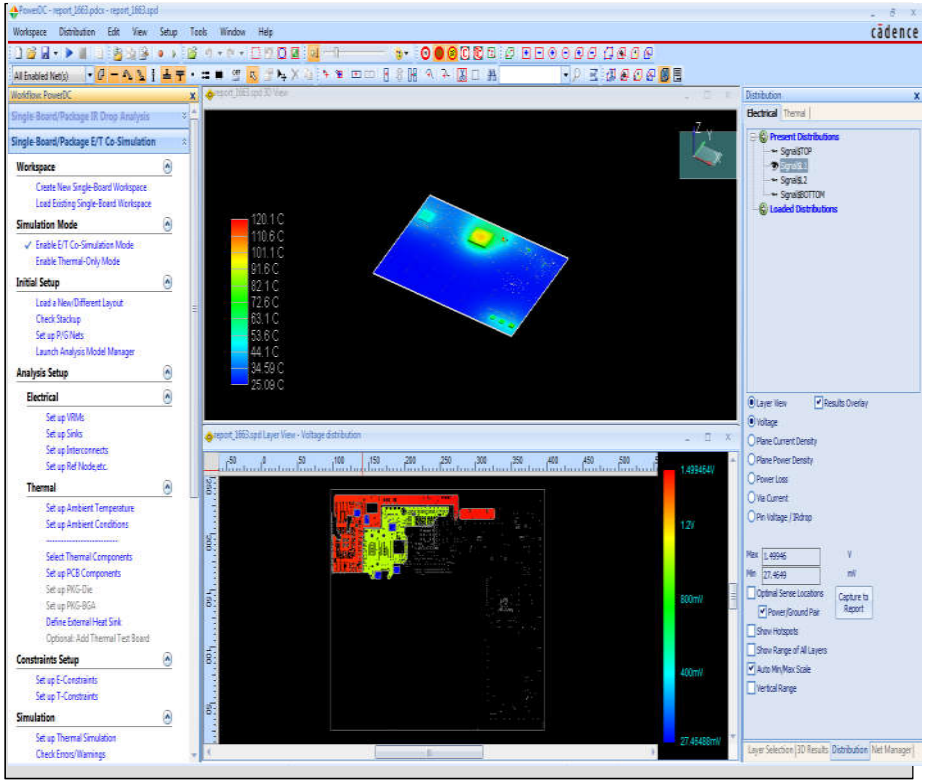


DeCap configurations can be analyzed and saved as PI CSets



Effective radius and setback drive DeCap placement

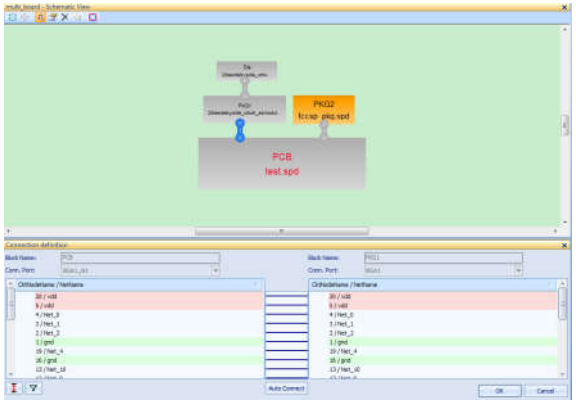
PowerDC



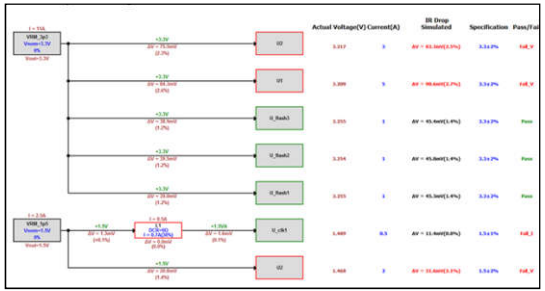
PowerDC is an efficient DC sign-off solution for IC package and PCB designs with electrical / thermal co-simulation to maximize accuracy. IR drop and current hot-spots are quickly pinpointed. Best remote sense locations are automatically found.

PowerDC Primary Advantages

- ✓ The first and only integrated and automated electrical and thermal co-simulation for PCBs and packages
- ✓ Patented time saving automation for remote sense line positioning
- ✓ Fastest and most accurate IR drop solution
- ✓ Broad range of visualization options for rapid design improvement
- ✓ Unique block diagram results visualization supporting what-if updating
- ✓ Blockwise multi-board E/T co-simulation
- ✓ Unified management for setting parameters
- ✓ Integration with Allegro Sigrity PI solution

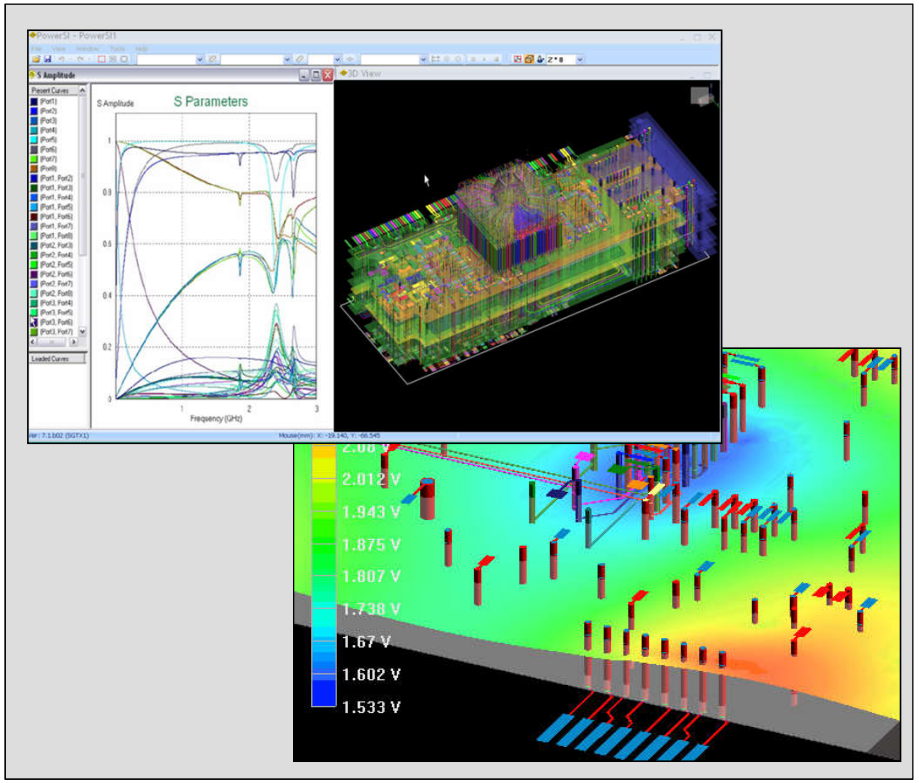


Multi-board E/T Co-simulation



Power DC block diagram view

PowerSI

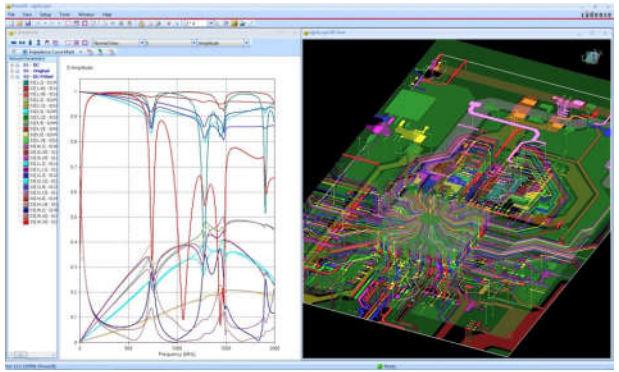


PowerSI is a virtual multi-port Vector Network Analyzer for advanced signal integrity, power integrity and design-stage EMI analysis.

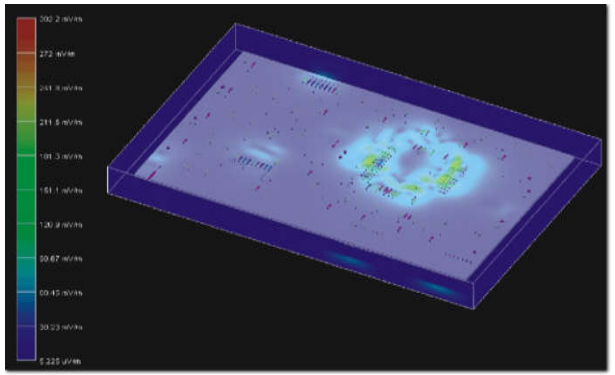
Supports S-parameter model extraction, trace impedance and coupling checking, and provides multiple frequency domain analysis modes for entire IC package and PCB designs.

PowerSI Primary Advantages

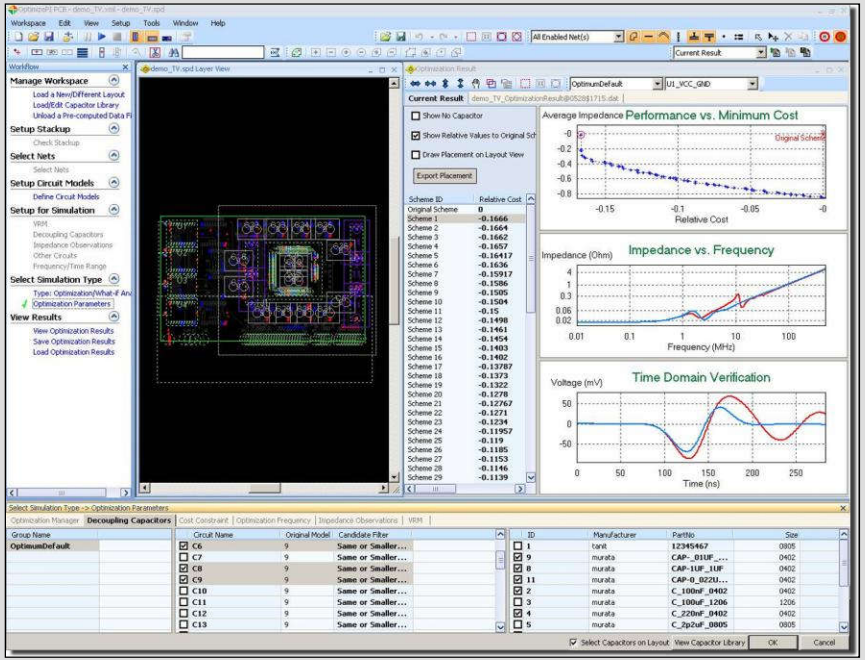
- ✓ Market leader and product of choice where power and signal integrity analysis is essential
- ✓ Highly accurate modeling of IC package and PCB structures
- ✓ Single-ended and mixed-mode results and post-processing
- ✓ Adaptive frequency sampling and intelligent result storage
- ✓ Supports component / circuit models with unlimited terminals
- ✓ Unique capability for ensuring accuracy down to DC with integrated PowerDC analysis
- ✓ Targeted workflows to streamline setup operations
- ✓ Integration with full wave and quasi-static 3DEM solver



Frequency domain SI, PI and EMC



OptimizePI



OptimizePI is a highly automated AC analysis solution for IC Packages and PCBs. Optimizes decoupling capacitor selection and placement during pre- and post-layout for target device and EMI. Identifies impedance and PDN resonance issues.
DeCap implementations are optimized for performance, cost, area and number.

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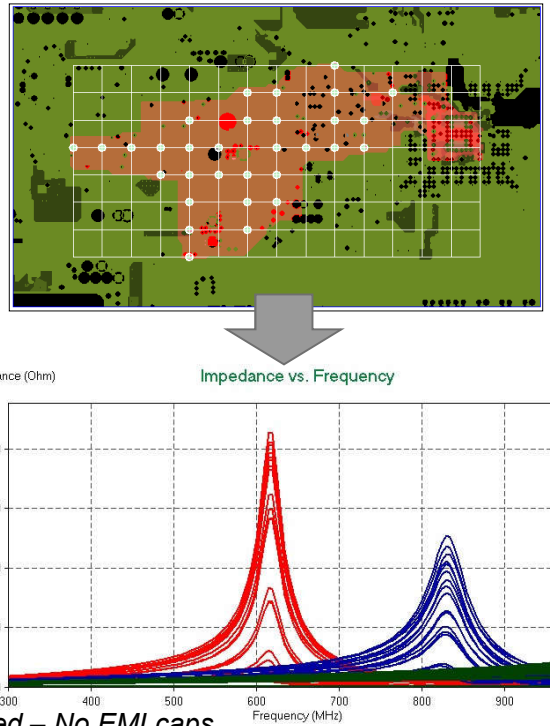
OptimizePI Primary Advantages

- ✓ Automated DeCap optimization of placement and value selection
- ✓ Back-annotation of optimized DeCap scheme to Allegro
- ✓ Clear presentation of economic benefits from DeCap optimization
- ✓ Flexibility in meeting multiple objectives (performance, cost, area, number); what-if; statistical
- ✓ Easy-to-use AC analysis environment with workflow setup
- ✓ Unique device impedance and EMI resonance checking
- ✓ Support for early-stage studies and post-layout verification
- ✓ DeCap loop inductance analysis to identify poorly mounted caps
- ✓ Device Per-Pin inductance checking and display

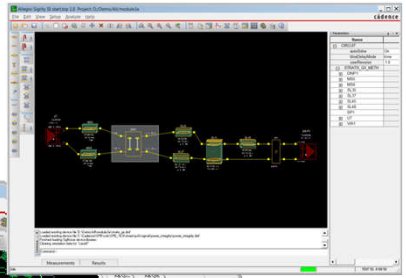
Automated positioning and selection of EMI decoupling capacitors



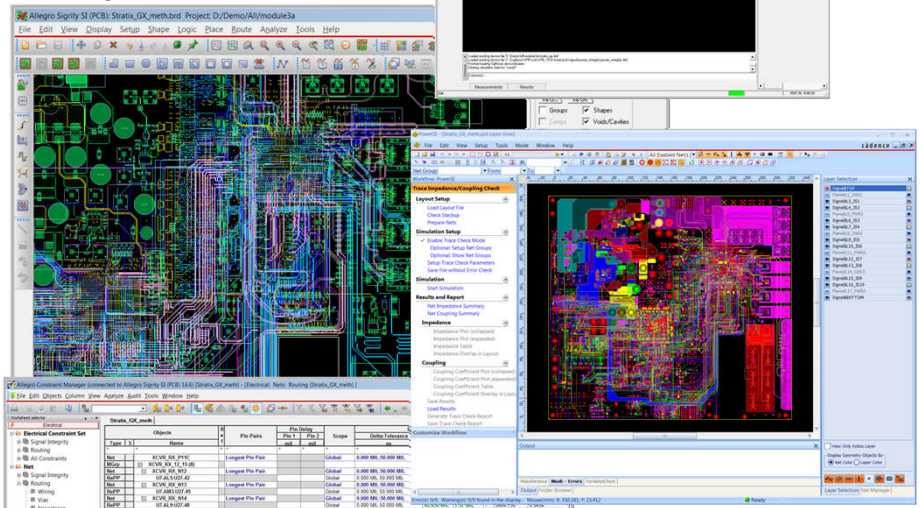
Red – No EMI caps
Blue – 1 cap; Green – 3 caps

Allegro Sigrity SI Base

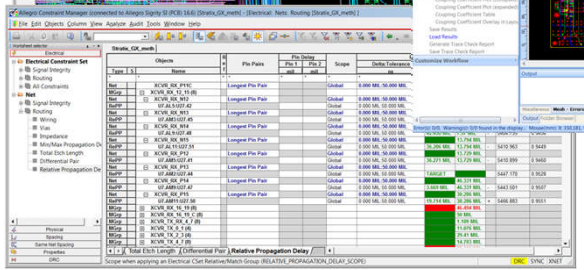
Topology Editor



Floorplanner



SI ERC checking

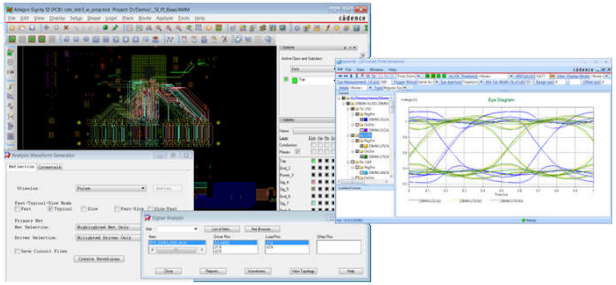


Constraint Manager

Allegro Sigrity SI Base integrates Allegro and Sigrity technology for SI analysis of PCB, IC Package and SiP designs. Enables constraint driven design with a unique combination of TD SI simulation, layout editing, topology exploration, and SI related ERCs

Allegro Sigrity SI Base Primary Advantages

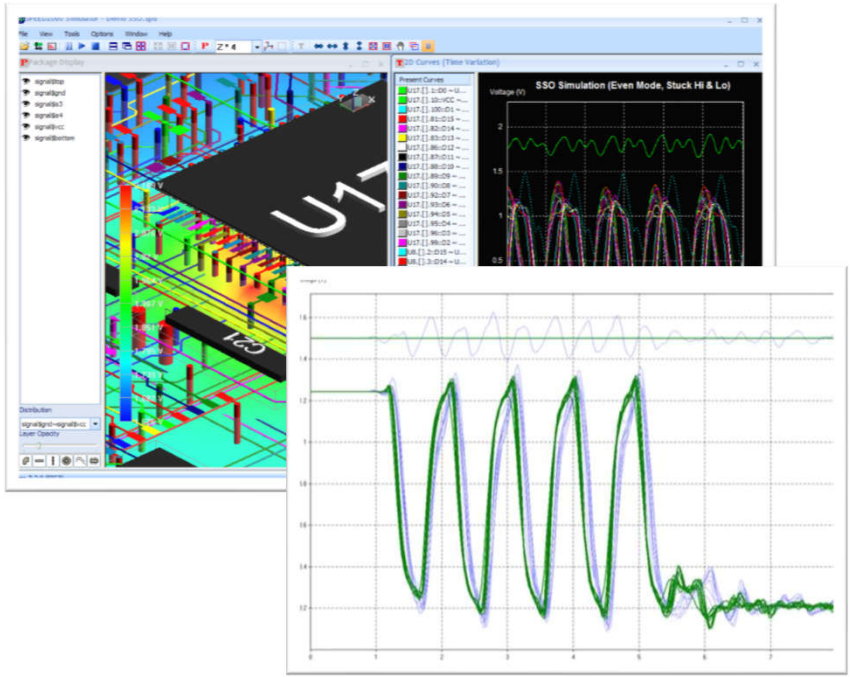
- ✓ Virtual prototyping and floorplanning of physical layouts leveraging Allegro libraries
- ✓ Seamless integration enables direct simulation of design changes on the fly
- ✓ Electrically aware physical design for simulation and constraint validation at any design stage with Allegro Constraint Manager
- ✓ Sweeping of topology parameters to determine solution space can be captured as constraints to drive physical PCB and package layout
- ✓ Easy to use SI ERCs for quick screening of impedance or coupling
- ✓ Add-on options for detailed analysis, compliance and assessment



Layout editing / routing and first order TD SI simulation

What-if simulation and constraint capture

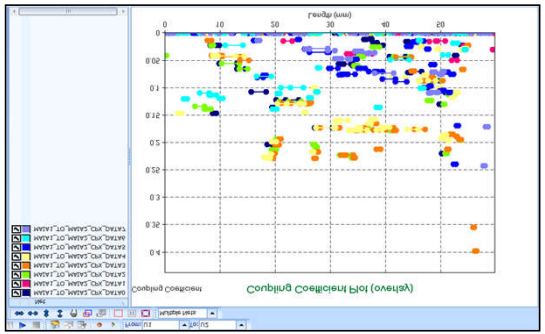
SPEED2000



SPEED2000 is a comprehensive PCB/package layout based time domain EM simulation tool for signal integrity, power integrity and design-stage EMI analysis. It supports advanced physical and electrical layout checking for design sign-off and debug.

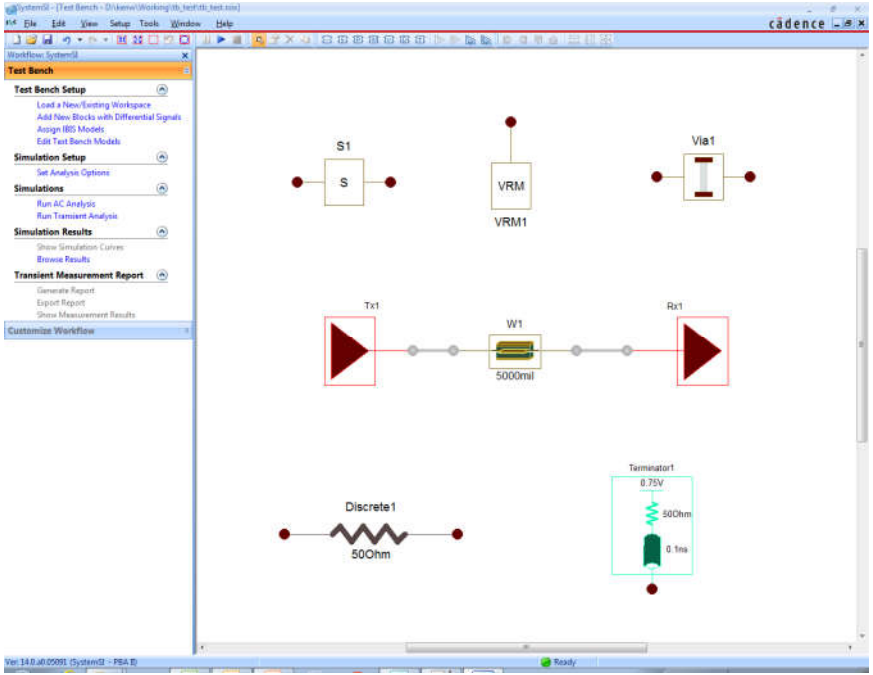
SPEED2000 Primary Advantages

- ✓ Unique layout-based SI simulation, incorporating non-ideal power distribution network (PDN)
- ✓ Unmatched ability to simulate very large groups of signals together with non-ideal PDN
- ✓ Targeted workflows for Trace Checking, SI Metrics, General SI Simulation, SSO Simulation, and SI/PI/EMI Co-Simulation
- ✓ Unique animation of transient field propagation across PCBs and packages
- ✓ Only solution for EMC simulation with non-linear drivers and receivers
- ✓ Provides Level 1 and Level 2 Extraction where models can be used in System level analysis



Trace coupling check
(initial and expanded views)

System Explorer



System Explorer is a general purpose signal and power integrity environment that enables custom topologies to be quickly constructed for AC, DC, and transient circuit simulation.

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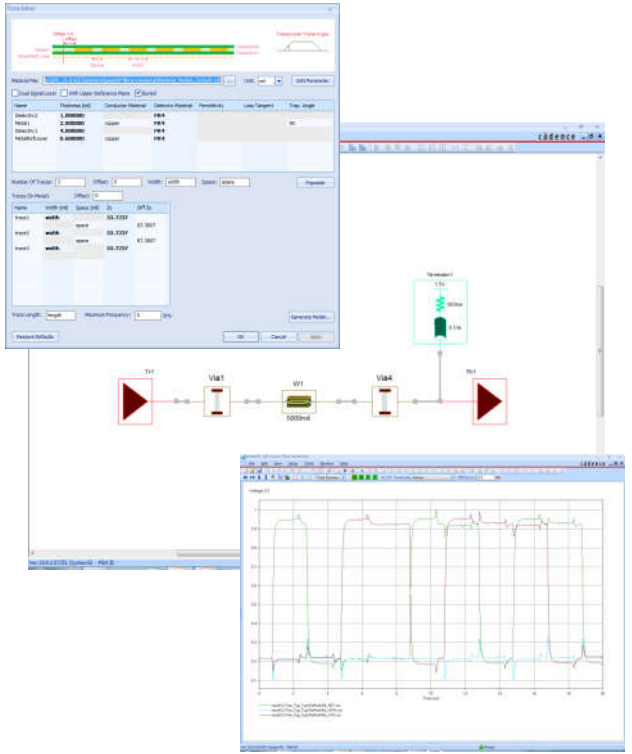
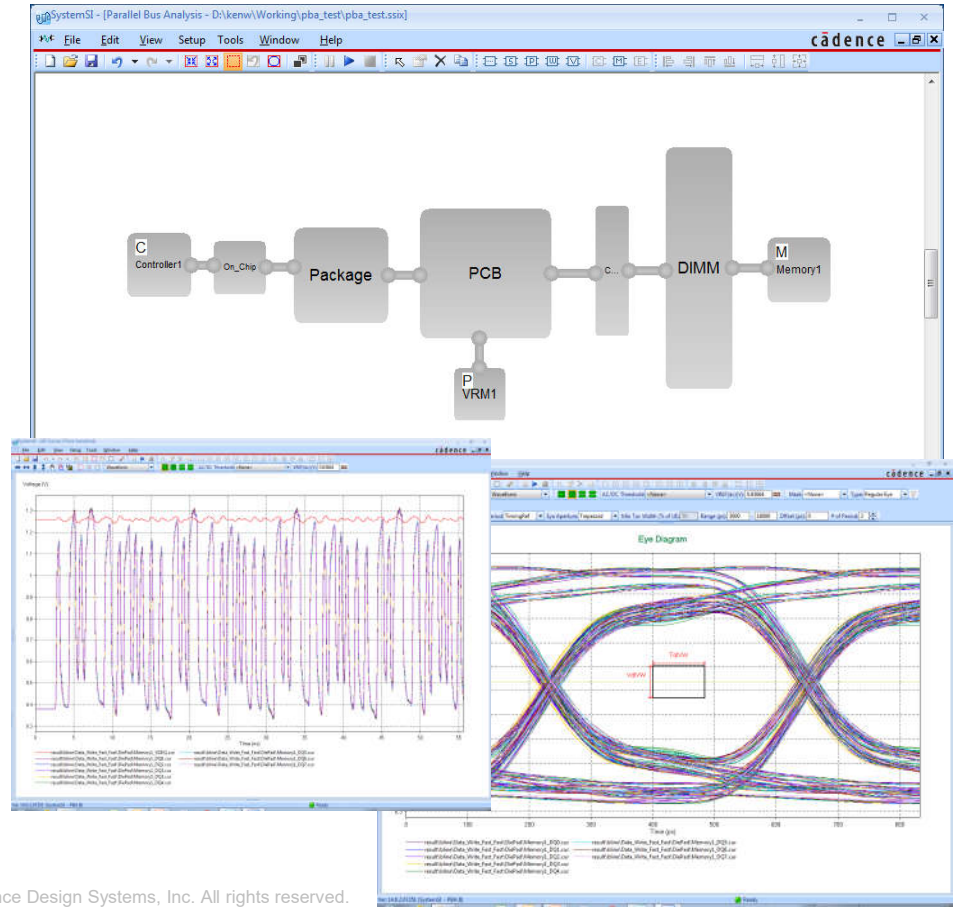
System Explorer –Primary Advantages

- ✓ Easy-to-use wire-based graphical connectivity definition
- ✓ IBIS, SPICE, and S-parameter power-aware system-level modeling
- ✓ Concurrent, comprehensive simulation of both SI and PI effects
- ✓ Convenient pre-defined blocks for common circuit elements (RLCs, W-elements, TLines, drivers, receivers, etc.)
- ✓ AC, DC, and transient circuit simulation
- ✓ Automated measurement and report generation for waveform quality, eye quality, and delays



SystemSI – Parallel Bus Analysis



SystemSI – Parallel Bus Analysis is a comprehensive and automated signal integrity and timing environment for the assessment of source synchronous interface performance.

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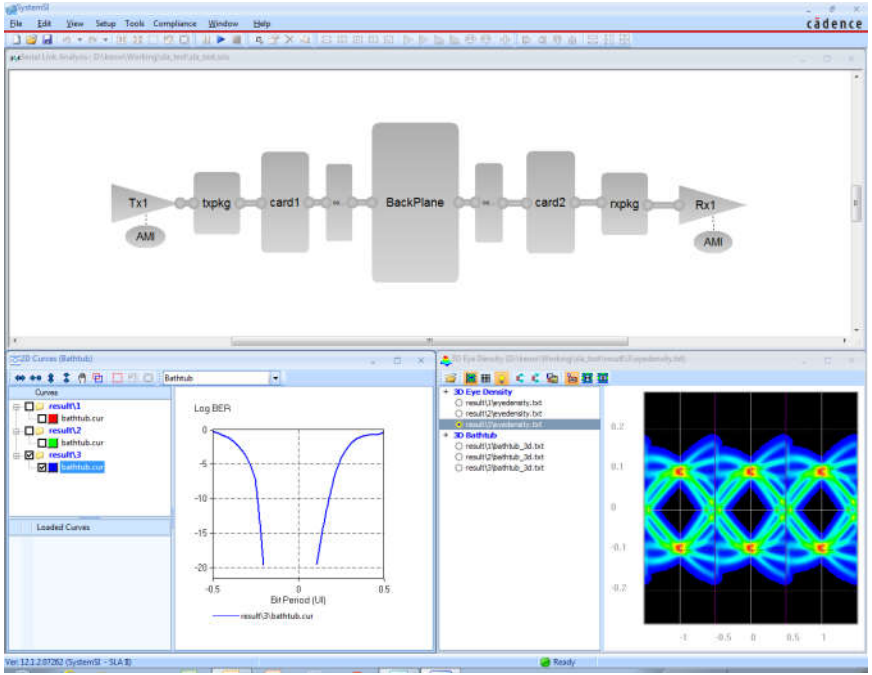
SystemSI – Parallel Bus Analysis Primary Advantages

- ✓ Simplified model connections with Model Connection Protocol (MCP) and block-level editor
- ✓ IBIS, SPICE, and S-parameter power-aware system-level modeling
- ✓ Concurrent, comprehensive simulation of both SI and PI effects
- ✓ Detailed worst case/best case timing analysis for source synchronous interfaces
- ✓ Highly automated JEDEC-based measurement, reporting, and crossprobing capabilities for DDR compliance
- ✓ Use and/or build AMI models that model I/O equalization (created models will run only in SystemSI)

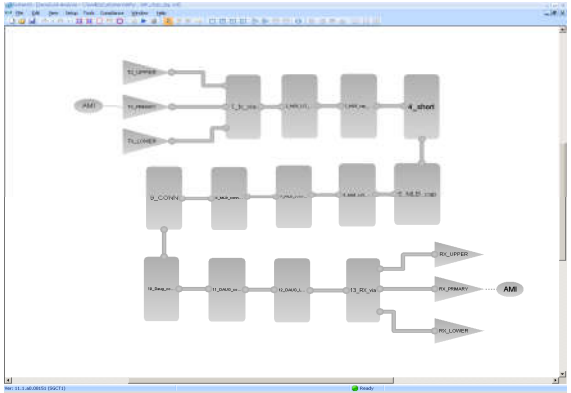
SystemSI – Serial Link Analysis

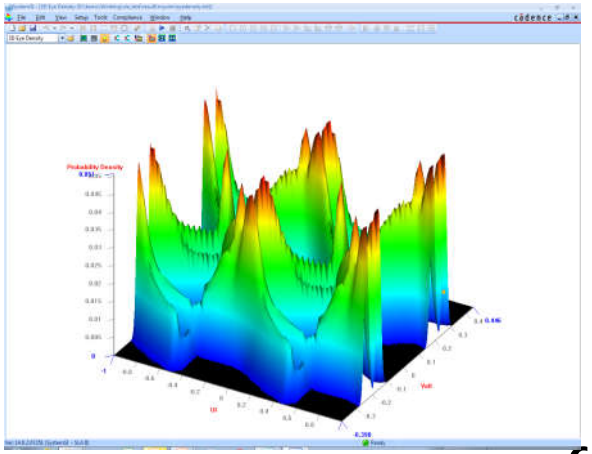


SystemSI – Serial Link Analysis is a comprehensive and automated signal integrity environment for the assessment of BER performance in multi-gigabit serial link interfaces.

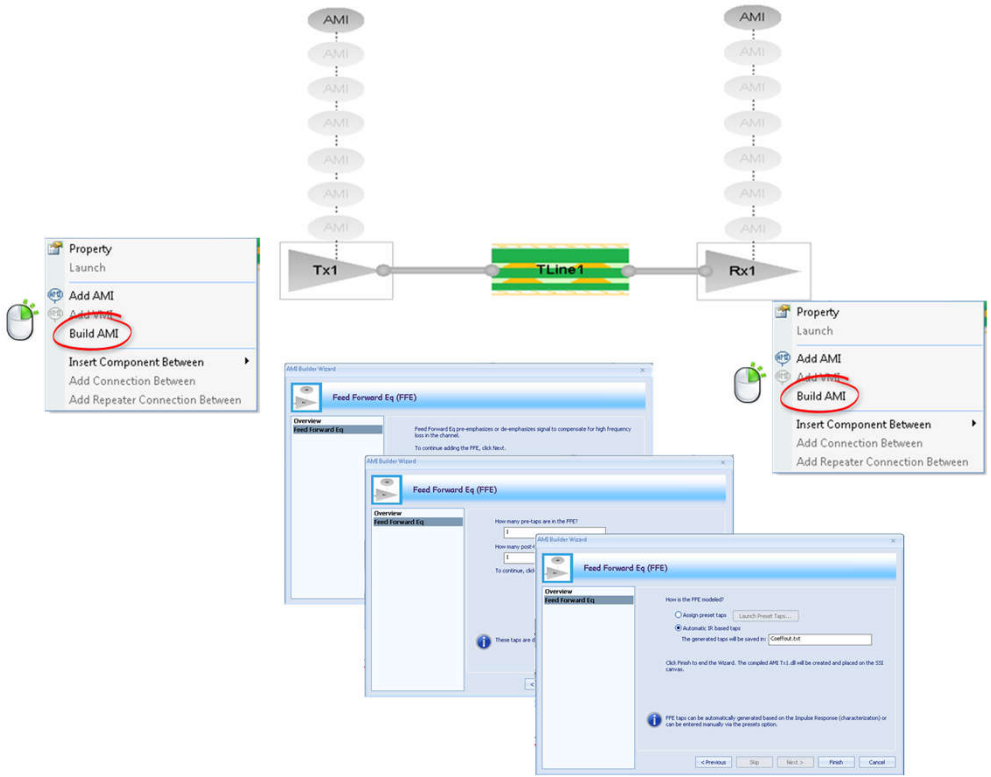
SystemSI - Serial Link Analysis Primary Advantages

- ✓ IBIS, SPICE, and S-parameter power-aware system-level modeling
- ✓ Concurrent, comprehensive simulation of both SI and PI effects
- ✓ Advanced channel simulation engine for high-capacity serial link simulation and BER analysis
- ✓ Comprehensive, parameterized AMI model library for modeling of advanced SerDes equalization
- ✓ Automated compliance kits for popular serial link standards
- ✓ Use and/or build AMI models that model I/O equalization (created models will run only in SystemSI)





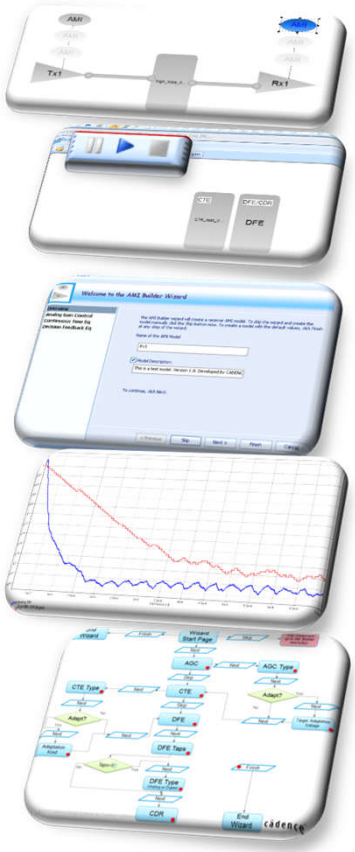
SystemSI - Advanced AMI Builder



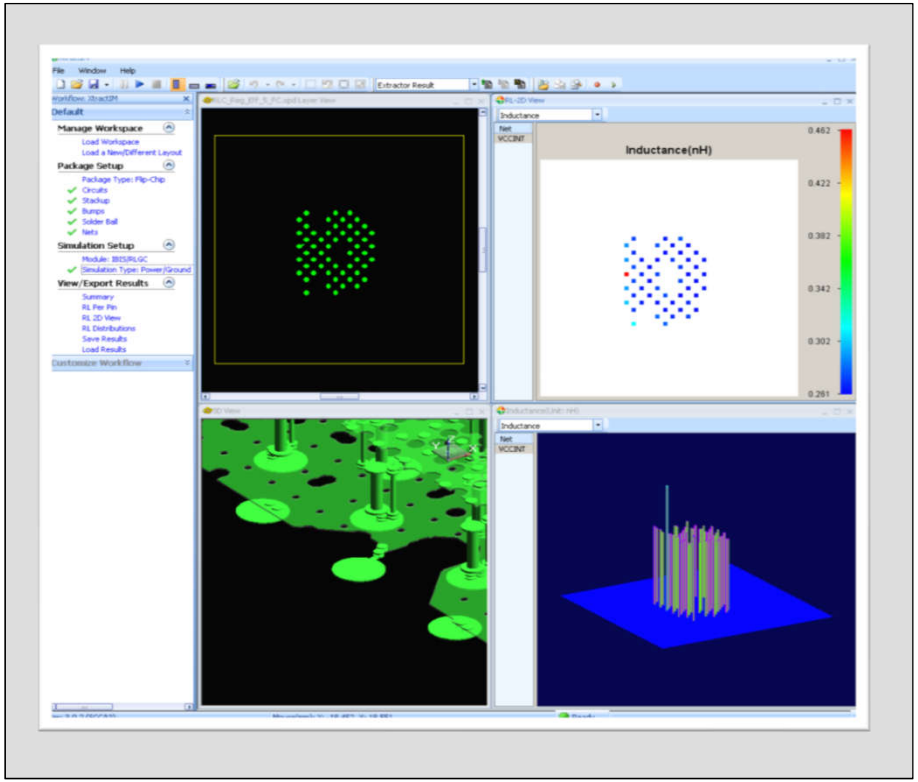
Advanced AMI Builder contains all the features of SystemSI SLA and PBA plus the ability to create IBIS-AMI models that can run in any vendor's simulator that supports IBIS-AMI

SystemSI Advanced AMI Builder – Primary Advantages

- ✓Includes all the features of SystemSI SLA and PBA
- ✓AMI models have no restrictions – can run in any vendor's channel simulator
- ✓Fast turnaround – model gets created at the click of a button



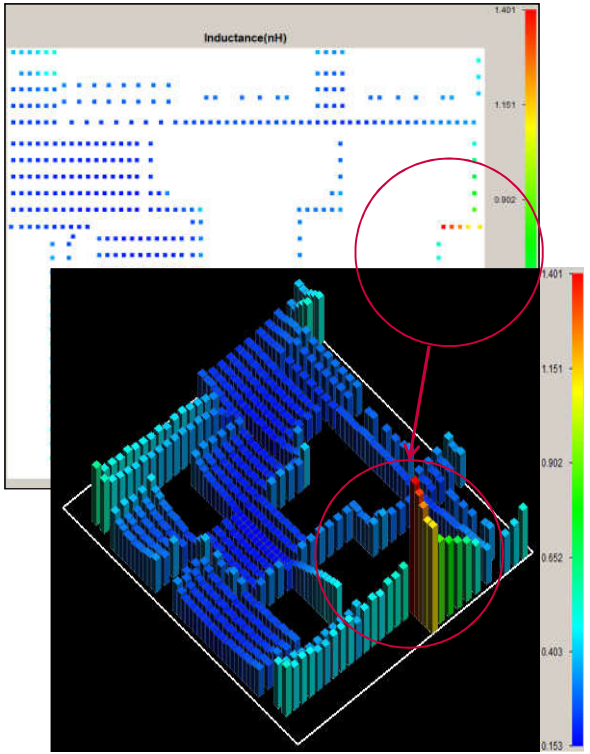
XtractIM



XtractIM is a fast IC package RLC extraction and assessment solution with an option to generate highly accurate broadband models. Supports a broad range of package types including BGA, SiP and leadframe designs.

XtractIM Primary Advantages

- ✓ Built in package assessment rapidly identifies potential package defects
- ✓ Unsurpassed extraction speed and ease of use
- ✓ Able to address the broadest range of packages (single die & multi-die; flip chip, wirebond & leadframe)
- ✓ Users control model extraction precision (RLCG to broadband accurate)
- ✓ Extraction with Sigrity hybrid solver, quasi-static and full wave 3D-EM engines
- ✓ Easy to learn for occasional users and layout designers
- ✓ HTML reports that can be readily shared with partners



Red curve shows impact of Per-pin self loop inductance

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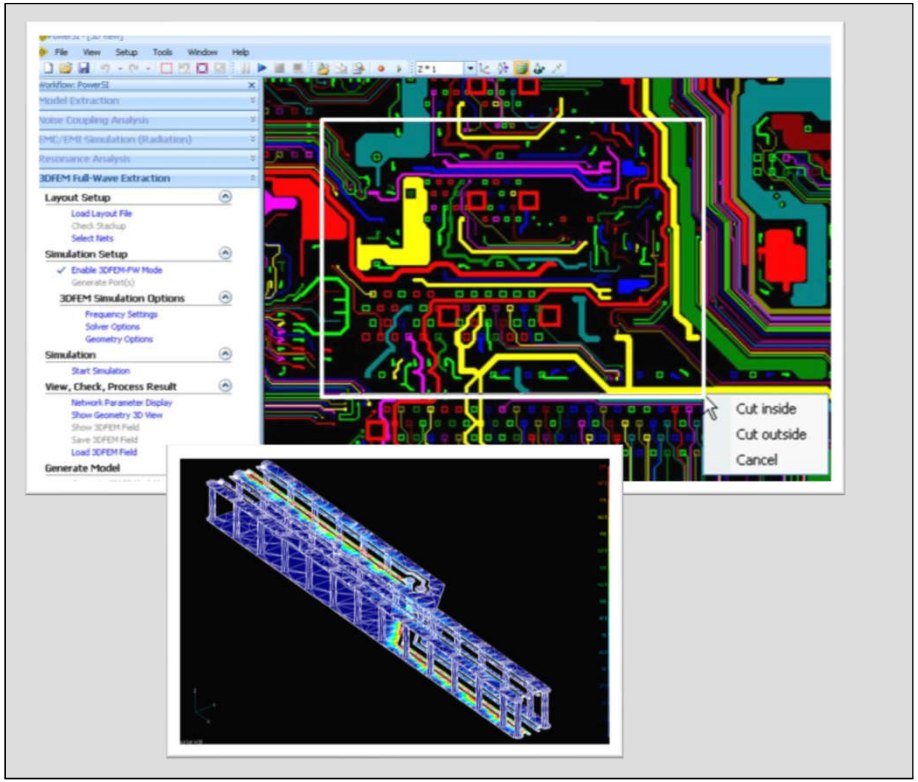
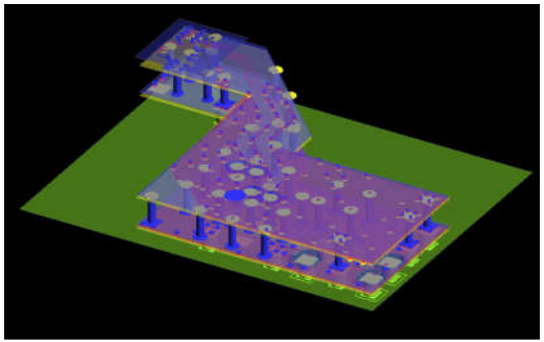
PowerSI 3D-EM

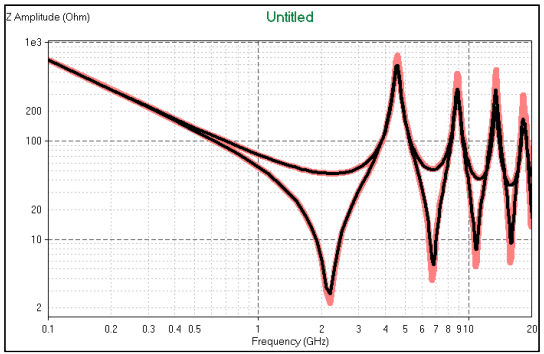


PowerSI 3D-EM provides full-wave and quasi-static solver capability inside PowerSI for accurate analysis of complex 3D structures. The software is tailored to IC package and PCB structures. Adaptive meshing assures accuracy combined with fast simulation time.

PowerSI 3D-EM Primary Advantages

- ✓Much faster (often 10x vs. HFSS) with comparable accuracy
- ✓Highly accurate low frequency solution and explicit DC solution
- ✓Easy to use with geometry modeling and automated port setup
- ✓Reliable frequency sweeping solution with no time-consuming point-by-point simulation.





- ***Differential pair in 6 layer package***
- ***Results showing correlation with HFSS***

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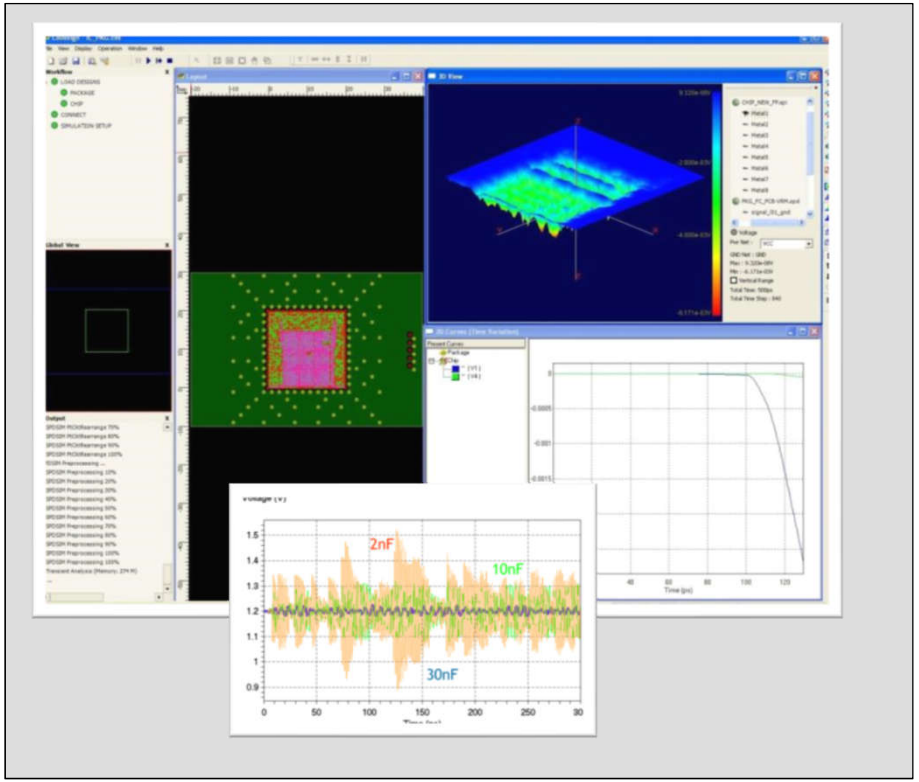
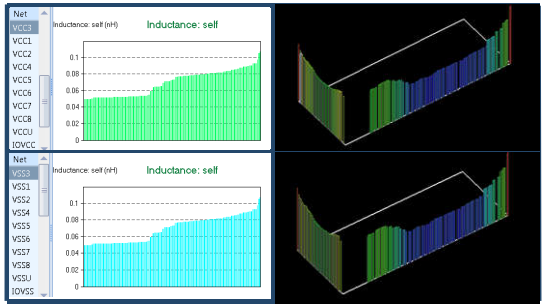
XcitePI



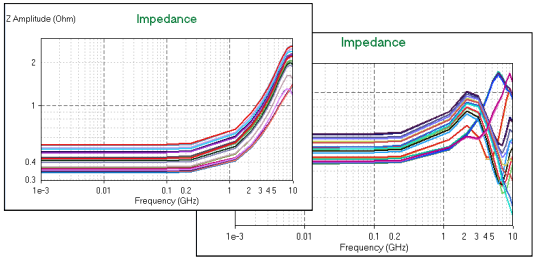
XcitePI is a full-chip power integrity solution targeting on chip / system co-design applications. It supports early chip power planning, IO and core model extraction, and simulation in both the time and frequency domains.

XcitePI Primary Advantages

- ✓ Performs both transient and frequency domain analysis of on-die PDN including packaging effects
- ✓ Easy what-if analysis of decoupling capacitor placement, and power grid and bump design changes
- ✓ Generates full-chip PDN models with high pin resolution and compact circuit size
- ✓ Quickly checks IO power/ground and signal electrical performance to identify potential design defects
- ✓ Generates IO power/ground and signal interconnect models for system-level analysis of high-speed channels and buses
- ✓ Supports early stage studies and post-layout verification



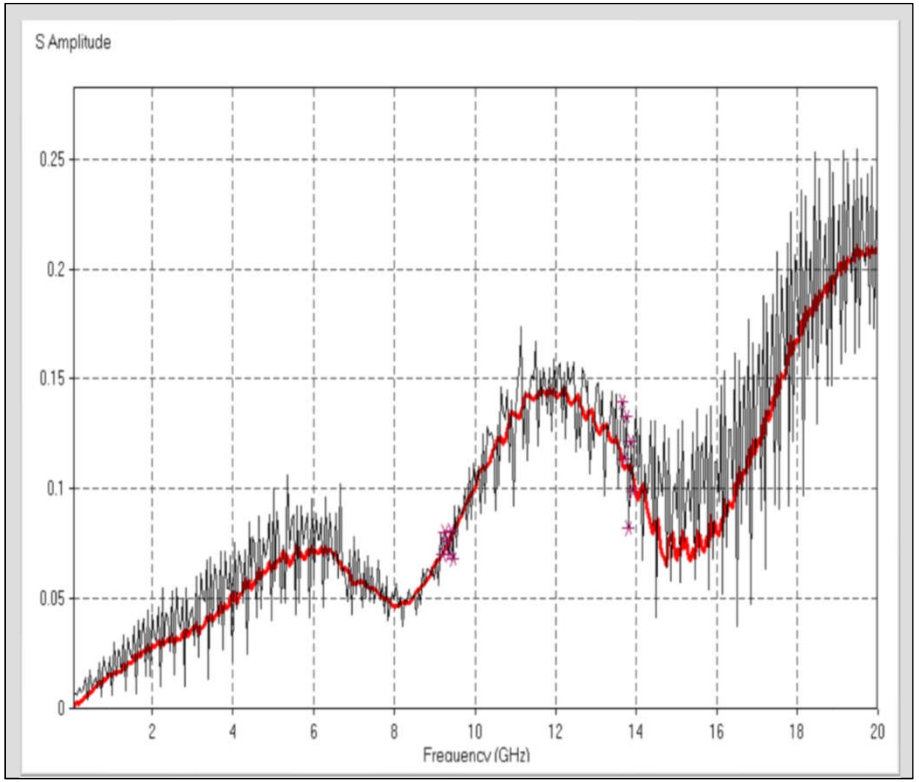
Power net self loop inductance at each IO cell



Power net impedance

(L = power net only / R = power net plus on-die circuit

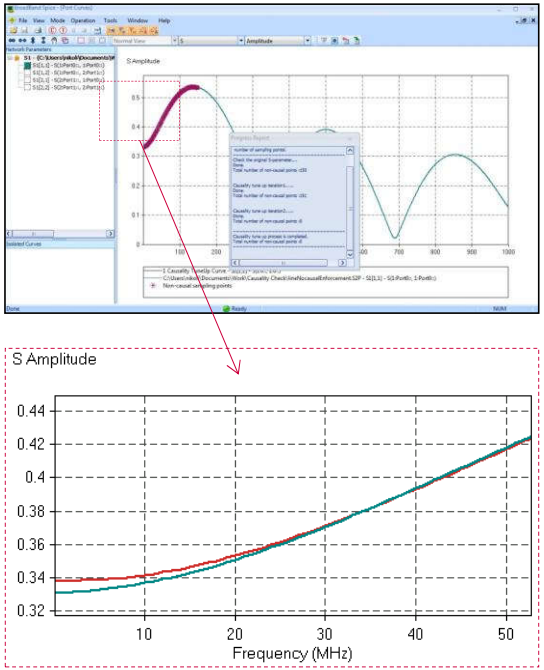
Broadband SPICE



Broadband SPICE offers a combination of S-parameter checking, tuning and extraction capability to convert N-port network parameters to efficient SPICE compatible circuits that can be used in time domain circuit simulators.

Broadband SPICE Primary Advantages

- ✓ Market leader for SPICE macro-model extraction
- ✓ Extensive checking functions for S-parameter model tuning and improvement
- ✓ Automated adaptive port reference impedance technique to enhance model accuracy (patent pending)
- ✓ Enables faster S-parameter simulations
- ✓ Integration with PowerSI and SystemSI for streamlined design flows



Red curve shows impact off S-parameter tuning

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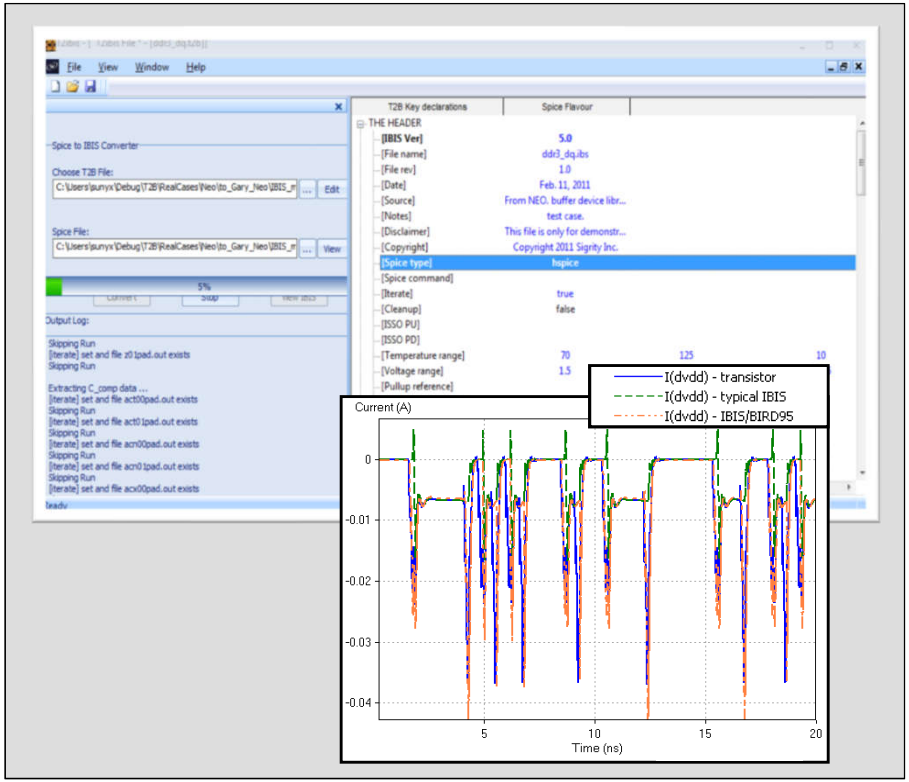
T2B

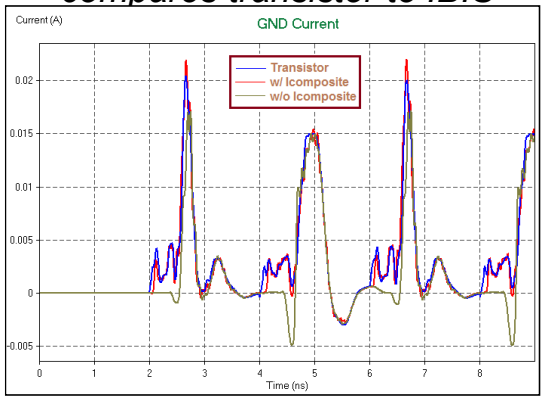


Transistor to Behavioral Model Conversion (T2B) provides an efficient way to create accurate power-aware IBIS IO models for simulations with SSO effects. These models run orders of magnitude faster than the original transistor models.

T2B Primary Advantages

- ✓Industry's most advanced tool for converting transistor models to power-aware IBIS
- ✓Convenient GUI verifies conversion accuracy
- ✓Simulation speed-up makes full bus simulations practical that would otherwise take weeks
- ✓Optional IBIS plus model provides additional level of accuracy

Built-in simulation check compares transistor to IBIS



Impact of pre-driver current

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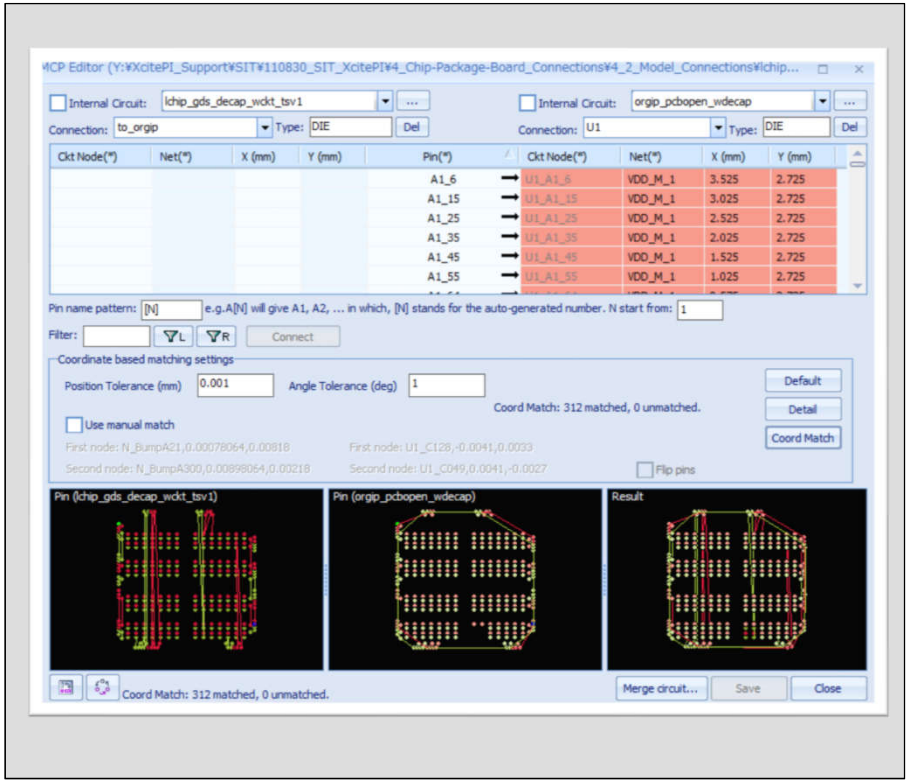
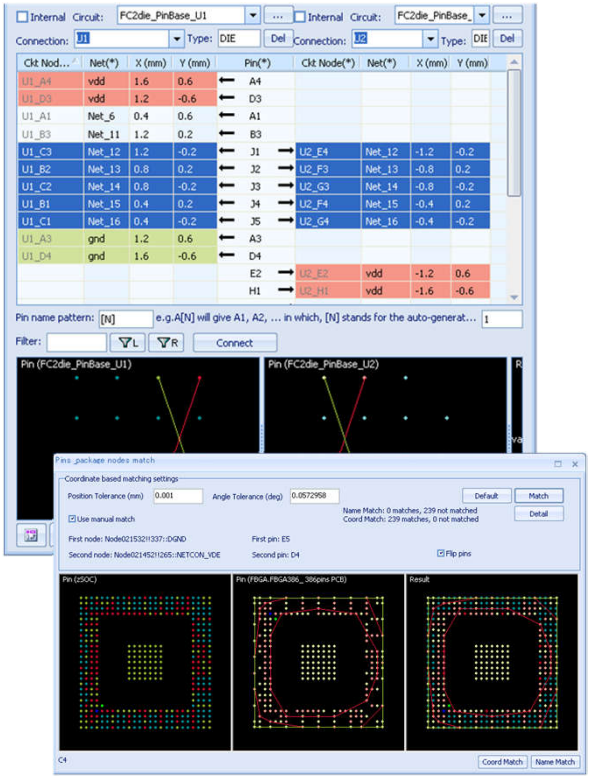
MCP



Model Connection Protocol (MCP) simplifies time consuming model connections to support multi-structure simulations. Tedious and error prone operations are streamlined to make complex simulations practical.

MCP Primary Advantages

- ✓Open format, available from Cadence without charge
- ✓Reduces error-prone connection and wiring tasks
- ✓Simplifies connectivity to enable multi-structure simulations
- ✓Large scale chip-to-package, package-to-PCB connectivity easily achieved
- ✓Makes it practical to predict localized behavior by enabling per-pin connections



Simplified model connections