AGATA AMB Phone conference 28 of June 2024

Sujet : AGATA AMB June 2024

Apologies:

LNL Status (J.J. Valiente-Dobon)
No Report

ASC Report / ASC Matters
Magda Gorska is the new chair of the ASC.
Magda Zielinska is the new vice-chair of the ASC

ACC Report / ACC Matters
Acc deadline for contribution is set on the 26th of August. Call for abstract to be sent ASAP with focus on 2022+2023 data.
There will be presentations by GANIL and LNL for the host laboratory process on Thursday.

GSI Status (K. Wimmer)
No report

REPORTS FROM THE WORKING GROUPS

Detector Module (H. Hess)

Activities on Detector Capsules

A021: new detector, owner Liverpool, FAT by IPHC Strasbourg
Delivered to Cologne on 29th January

A022: new detector, owner Spain, FAT by Saclay
Delivered to Cologne on 24th April

A006: delivered to Mirion on 20th March for annealing
Delivered to Cologne on 25th June

A008: delivered to Mirion on 20th March for annealing
Under repair due to leakage current after annealing

B008: FAT after repair due to leakage current by IPHC Strasbourg & Saclay
Delivered to Cologne on 29th January

B005: delivered to Mirion on 20th March for annealing
Delivered to Cologne on 27th May

B009: delivered to Mirion on 20th March for annealing
Delivered to Cologne on 07th May

C001: delivered to Mirion on 20th March for annealing
Delivered to Cologne on 25th June

C014: delivered to Mirion on 20th March for annealing
Delivered to Cologne on 07th May

Allocation of the detectors:

66 detectors available within the AGATA community

INFN Legnaro:
At the moment 45 detectors are mounted in 15 ATCs

Saclay:
0 detectors

Liverpool:
0 detectors

IPHC Strasbourg:
1 detector

- A005 mounted in the Salamanca TC, scanning ongoing

Salamanca:
1 detector

- B003 mounted in the IPHC TC, scanning ongoing

IKP Cologne:
18 (+3 + 3) detectors

- A001, A006, A015, A022
- B002, B005, B009, B013
- C001, C002, C008, C017
- S001, S002, S003
- A021, B022, C014, mounted in ATC22
- A012, B008, C022, mounted in ATC23
- A501, B501, C501 mounted in DEGAS TC

MIRION:
1 detector

- A008 repair due to leakage current after annealing

The AGATA community is at the moment proprietor of 66 detectors. Out of this 66 detectors 36 are in use at Legnaro for the physics campaign and 6 are prepared to be transported to Mirion for annealing. In Cologne are at the moment allocated 18 detectors with 11 spare ones and C017 which suffers from leakage current over segment B1. This detector will be delivered end of July for repair. Remarkable is also that for the first time one detector suffers from leakage current after annealing (A008).

Open Orders:
7 detectors

- A023: Owner (UK)
- A024: Owner (GSI)
- A025: Owner (Italy)
- B023: Owner (GSI)
- B024: Owner (CEA)
- C023: Owner (GSI)
- C024: Owner (Italy)

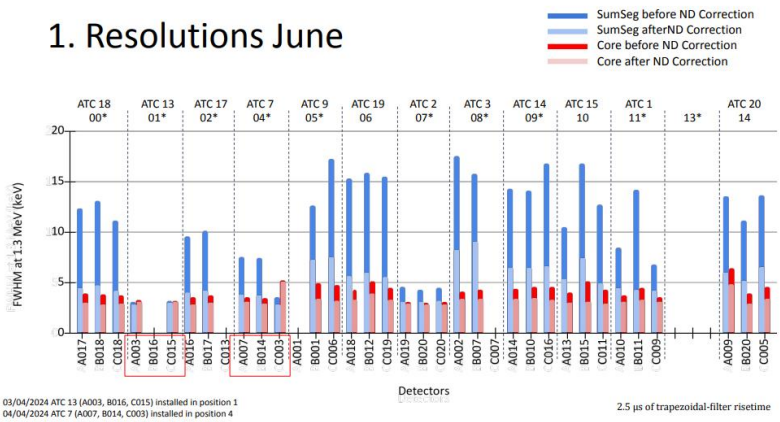
At the open orders the periodization is first at the UK order then the three GSI detectors.

Cluster Assembly and Maintenance

Legnaro:

Status Array & repairs:

12 ATCs mounted in the frame



5 ATCs in the lab:

ATC21: one segment missing used for new digitizer tests

ATC06: cryostat annealed waiting for detectors

ATC12: cryostat annealed waiting for detectors

ATC10: (A011, B006, C012) detectors waiting for transport to Mirion for annealing

ATC11: (A004, B004, C010) detectors waiting for transport to Mirion for annealing

Cologne:

DEGAS TC: assembled with A501, B501 & C501
Cold core preamplifier exchanged on detector B due to slightly degraded core
resolution.
Now the segment and core resolutions of all three detectors are within specification.
Waiting for delivery to FAIR, intention to use it for DESPEC experiments.

ATC22 (serial number 10092, owner INFN): assembled with A021, B022 & C014
Detector C017 was replaced with detector C014 due to leakage current, will be transported to Legnaro in week 29

ATC22 (serial number 10093, owner INFN): assembled with A012, B008 & C022
will be transported to Legnaro in week 29

ATC16 (conversion of ADC to Triple): tests with electronic test device finished, waiting for
detectors

Other Business:
It is proposed to use the INTRANS funds from EURO-LABS for the Herbert visit in LNL.

Infrastructure (B. Million)

No specific news.
See mail for the Host Lab document → Please read it !!

Front End Electronics (A. Gadea)

Coordination: last Electronics W.G. VC June 17th 2024, next Electronics W.G. VC meeting on Tuesday July 23rd 2024 at 10:00 CET, 9:00 U.K.

Pending actions:
-Meeting with O. Stezowski and N.Dosme: RUDP discussion meeting. Possibly during the AGATA week
-Meeting with J.Collado, GANIL, LNL and Padova Colleagues: brainstorming on GTS alignment protocol.

Status at LNL (A.Goasduff et al.):

-Procurement started for an Isolated heat exchanger to cool digitiser.

-Last experiment is AGATA high energy performance test at the end of July

-Regarding the EMC testing, the Inspection line output from DIGIOPT12, discussed at last meeting, exists but there is not enough space to access the inspection line without disconnecting the MDR, so presently it can't be used.

-E.Clement reported good news regarding the progress on the Trigger Processor. A. Boujrad is working on the Xilinx development platform to correct the FIFO behaviour in the current firmware.
He is working on a new firmware version where emptying FIFO is done at the end of the coincidence window (not using the acceptance window or timeouts). In simulation this version reduces close to zero the problems previously observed. He is implementing this new version in the hardware now to check that hardware behaves like the simulations and shows the same improvement.
An alternative, in a parallel task, he is migrating 2018 Michel Tripon firmware (Used during the NEDA campaign) to the latest hardware platform. This week he will complete the tests on updated new firmware and then compare with the code port of M.Tripon's firmware using same test script for both tests. The aim is to compare the error rates with the 2 versions.

-A.Goasduff proposed the updated firmware to be tested at LNL in July.

DIGIOPT12 (A.Pullia, S.Capra):

A new delivery of 3.7.0 cards is coming soon. Two of the batch will be of a new version of the card, v3.7.1, which have been updated to overcome the problem of one channel which is noisier than the others. The digital output used as a trigger for ancillaries in the core cards can now be implemented with galvanic isolation which requires 3V PSU in the connector- a jumper has been added to allow connection of a power supply to one of the pins. This can be used to power a small external card to buffer the lines whilst retaining the ground isolation.

Analogue conditioning op-amps are becoming obsolete with July 2024 being the last buy. The op-amp is in a very compact package; v3.7.1 has a redesigned footprint with the standard sized footprint to broaden the options for replacements. A.Pullia is discussing with Benedicte Million to see if a large batch of the current op-amps can be bought with the next batch of INFN digitisers.

EOS has completed completed the production and qualification of the 9 AGATA boards ordered by GANIL. The board are:

-5 units AGATA DigiOpt12 v3.7.0 - Segment Boards
-3 units AGATA DigiOpt12 v3.6.1 - Segment Board - v3.6.0 layout adapted to v3.6.1
-1 units AGATA DigiOpt12 v3.6.1 - Core Board - v3.6.0 layout adapted to v3.6.1

These are spare boards to be used at LNL in the phase 1 electronics.

PACE Status (J.Collado, reported by A.Gadea)
PACE PCB PACE-CAP-v100-t58 design with a small modification. Quotations being provided and PCB production is being started (delivery in 2 months). Delivery expected by mid September. Buying 90 PCBs with the cost split between Valencia (2x 20 units) and GANIL (2x 25 units). Quotations due in few days and then procurement will start.

Working on updating the BOM to clear up some old components that are still there from previous versions. Quotes for board assembly after September will be obtained.

Regarding the issues in the Firmware- we still have
1) Data Packager to be validated
2) GTS Alignment to be tested.

Working philosophy is still to use the little time available from Javier to concentrate on one problem at a time.

The run 1800 data analysis report was received from Lyon. There are still some formatting issues. ADF header is just a copy of static data from a memory, but somehow is being intermittently corrupted in the data output.
The controlling state machine locks-up from time to time when combining all the blocks (GTS, readout, buffers…). A workaround in use now is to reset the state machine every time it locks-up which causes incomplete buffers in the output.
Javier's current theory is that the Xilinx inspection lines that Javier is using in the firmware might produce problems in normal running of the firmware.
J.Collado prepared a version without Xilinx inspection lines (the code uses Xilinx's own inspection blocks but apparently they can perturb the signals) but no improvements were found. This week he is concentrated in adding more control/inspection points to understand why the state machine signal is corrupted.

Goal for the PACE firmware work is first to complete packaging and data formatting code. Then move on to GTS code. At this point, a meeting will be called with Padova, GANIL, Valencia and J.Collado to discuss GTS testing. GTS does not align the PACE because it doesn't recognise PACE as a leaf. But PACE gets GTS clock and can synchronise to it. It seems that something else needs to be done, but is not clearly documented, and the people who have worked on this code previously in other parts of AGATA don't remember or don't know how the GTS recognises a leaf.
GTS testing is not yet started so we are discussing the option of testing this in collaboration with GANIL.

V.Gonzalez reported about changes to allow the option for the logical trigger input- mechanically this is possible- rear panel is already modified to add an extra hole for a new connector. There is an SMC connector on PACE that can be connected to an adapter on the back panel Also PACE cooling is being updated. There is no firmware available to work with this option yet.

No news yet on whether J.Collado can be paid by Valencia to continue to work on AGATA as part-time.

PSU and Mechanics: (V.Gonzalez, J.Collado)
Updated totals on the mechanics production:
12 PACE cooling blocks
66 STARE cooling blocks
204 Digiopt12 cooling blocks
45 heat exchangers (5 extra in the last month)

Front Panel- Al panels prepared for production
Rear panel Steel and Al prototypes produced (Al is for prototype only)
Trigger connector hole is implemented.
Front Panel lettering to be defined and added.

PACE board Valencia prototype with issues in the I2C configuration is a problem (can't make a full initialisation or read the sensors) now the SC FPGA is being modified to test the chain integrity.

PSU Backplane production is ongoing (On 7th July PCB due to be delivered and go to assemblers)
PSU discussion continues with providers to reduce lead time. PSU Noise as reported last time- no progress

Regarding the connector to the differential trigger signal, the rear panel is connected to PACE ground so connector will be connected to PACE ground (unless isolated). Connector is currently a 2 pin ECL connector in AGATA for GGPs but something more robust with grounding is needed, maybe 2 pin LEMO with ground to panel (or maybe a 3M SCI connector if a panel mount option is available) Decision on connector type will be discussed between A.Goasduff and V.Gonzalez.

STARE Status (N.Karkour, X.Lafay)
Production is ongoing, due in July- if delayed slightly then delay may be extended by Olympic Games

Still waiting for new 10Gbits switch for the readout test bench.

Software/Slow Control (Ch.Bonnin)
Oscilloscope GUI now exists to show monitoring data. Slow control is ready too.
ADF format created artefacts in the oscilloscope display. Previous to the meeting data from STARE without ADF headers were not available.
Confirmed that the Scope functionality in the specification documents is fully available.

J.Collado confirmed that there is an example of written monitoring data in run 1107 (onlineancillaries/testV2/) with adc data in 4 ch version: ch0, ch12, ch24, ch36. Monitoring is not ADF format, just raw data. Data can be extracted with https://sqm-mon-cat.py script in https://github.com/jacorui/sqm-a, is a very simple script.

The monitoring configuration is explained in the documentation and in the software help command of PACE_QuadLink_start. Presently the monitoring firmware allows to obtain data from STARE Eth link from: adc data, trapezoid, cfd... online for up to 4 selected channels. There is a limitation because the 4 selected channels have to be on the same type of data, i.e. yu can't show ADC stream data together with the trapezoid or DCFD. Work to extend the possibilities of the monitoring is to be scheduled.

Testing so far has validated slow control in one card, but not yet for 'scope mode data or multiple cards. Once the PACE firmware monitoring functionality is included, we can test the full chain of electronics and software for slow control and monitoring. A test bench is available in Orsay which has already been used to verify that the slow control software works correctly. X.Lafay is able to connect about 5 or 6 STAREs (although only 1 attached to a PACE) for further testing of the slow control with multiple hardware channels simultaneously. This already works in simulation, but the simulation can be verified with multiple hardware channels.

Testing and Production of phase 2 electronics:
DIGIOPT12 cards are being produced (upgrade to v3.7.1 is under test)

STARE production is under way (due end July)

PACE production. We selected the 38 day PCB option which is currently being purchased with mid September delivery
Assembly time- normally 2 months including the time to schedule the work (4 weeks to do the work and 4 weeks delay to schedule the work). October is likely date for the first production PACE cards.
PACE Mounting: The quantity of components at the company is enough for 70 units. Aim for 2024/25 production is 90 units so some extra sets of components are needed and for expensive parts AG is considering ordering for total 135 cards to get quantity discounts.
VG reported about changes to allow the option for the logical trigger input

Mechanics: VG needs to finish PACE cooling block change for cable run, then front/rear panel for production so likely to have everything for 50 units by end of September. Power backplane is produced, signal backplane is being designed, PSU production is not planned- assembly company offered 8-10 days to assemble 50 units (components exist).
PACE firmware is possibly going to become the limiting critical path item for the scheduling of the final installation now that hardware production of both PACE and STARE are under way.
System debug and installation: In LNL there is already a prototype system which can test the new hardware, firmware and software alongside GGP, GTS, GANIL Trigger

Processor which are all in the 2nd hall and ready to be used with an AGATA detector as soon as GTS progress can be made.

Personnel issues
Valencia is trying to get an internship and is also pushing for the contract to be readvertised.

E.Clement suggests trying to find a flexible contractor if we can't fill the post. We know that the documentation is not complete and sometimes missing entirely so we can't easily engage a contractor who delivers a fixed package of work for a fixed price. However, we could perhaps find a person who joins our team on site in LNL and we could buy their time as the deliverable rather than paying for specific tasks or pieces of code.

AGATA week draft programme
The following draft programme has been distributed to the Working Group:

- Introduction and Schedule 10'
(I.Lazarus/A.Gadea)

- Digitizers (DIGOPT12) Status and advancements on V.3.7 20'+5'
(A. Pullia)

- PACE Hardware and Firmware Status 25' + 5'
(J. Collado but if not available it will be given by A.Gadea)

- STARE Hardware and production Firmware Status 25'+5'
(X. Lafay / N.Karkour)

- Mechanics and Power supply Status 20'+5'
(V. Gonzalez)

Coffee Break 16h00 – 16h30

- Status of the Triggers and Trigger Processor test / Status of the Phase 1 electronic at LNL 25'+5'
(A. Goasduff)

- Status of the SMART development 20'+5'
(G. Wittwer)

- Status of the R&D on Energy Processing 20'+ 5'
(M. Kogimtzis)

- Discussion on how to proceed with the FEBEE developments/production in AGATA (Chairpersons I.Lazarus/A.Gadea)

The Slow Control contribution by Christian Bonnin will be included in the DAQ session on the morning of Wednesday 11th of September.

We need an EDAQ parallel session where among other questions we will discuss the RUDP firmware, Monitoring Firmware, SMART installation in AGATA, etc.
My idea is to have it the same day Tuesday September 10th from 09:00 to 12:30.

ACTIONS A.Gadea- Firmware brainstorming meeting with all those who have worked on GTS recently e.g. at GANIL Matthieu and Frederic plus anyone from INFN who remembers the GTS to review GTS code in PACE. Need to understand what is not working and how the undocumented parts of the GTS system work.

Data Processing (O. Stézowski)

Coordination:

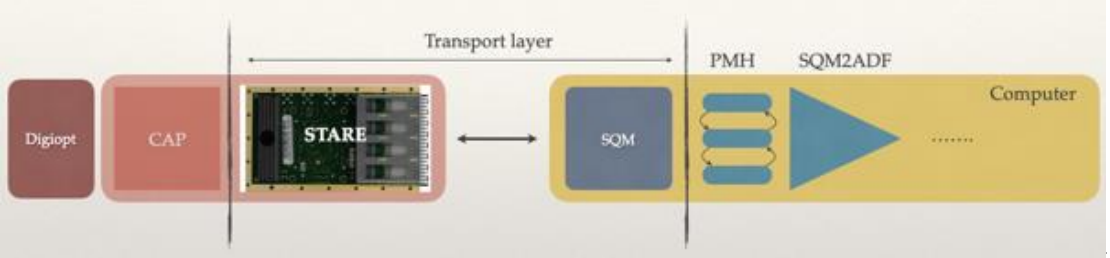
Last regular meeting 17/06/2024
CEPH dedicated meeting to discuss CEPH upgrade this year
Page dedicated to current actions here

Phase 1 and commands:

- RAM memory to upgrade all current machines
  - Ordering done 16/05/2024
  - Waiting for delivery
- CEPH upgrade
  - 3 new (core) disk arrays to be bought. 2 for CEPH + 1 to be used as anodeds6
    - About 36 000 euros … waiting for final quote from HP
    - should bring CEPH close to 400 [+100] To of safe disk [replica3]
    - hopefully at LNL beginning of September
    - NOTE: 2 other backup systems available on site
      - ancillary disk of LNL,
      - one old globicephala refurbished
- Others hardware check
  - Warning on anodeds6 seems ok after re boot
- Many issues on analysis1
  - ok to start a procedure on OC money ? [1U machine to be bought]
- Host lab document
  - Better to wait for tests with the dev daq box
- To help getting data from the grid
  - Docker provided to be used as Grid User Interface
  - https://agata.pages.in2p3.fr/handbook/data/grid/

Phase 2 developments:

- V2 electronic data pipeline



- Slow control developed by Christian being installed at LNL
  - Tests with the card foreseen
  - First version of the oscilloscope mode to be tested with Javier's data
  - And then directly on site by IPBus

- Data produced at LNL
  - 3 'recent' runs produced (29/04)
    - 1800: many TS issues … not checked more than that
    - 1801: 190 000 UDP packets supposed to be single ADF?
      - 188 300 single UDP
      - 1700 dispatched on 2 packets
    - 1802: 190 000 UDP packets supposed to be single ADF?
      - 188 366 single UDP
      - 1636 dispatched on 2 packets

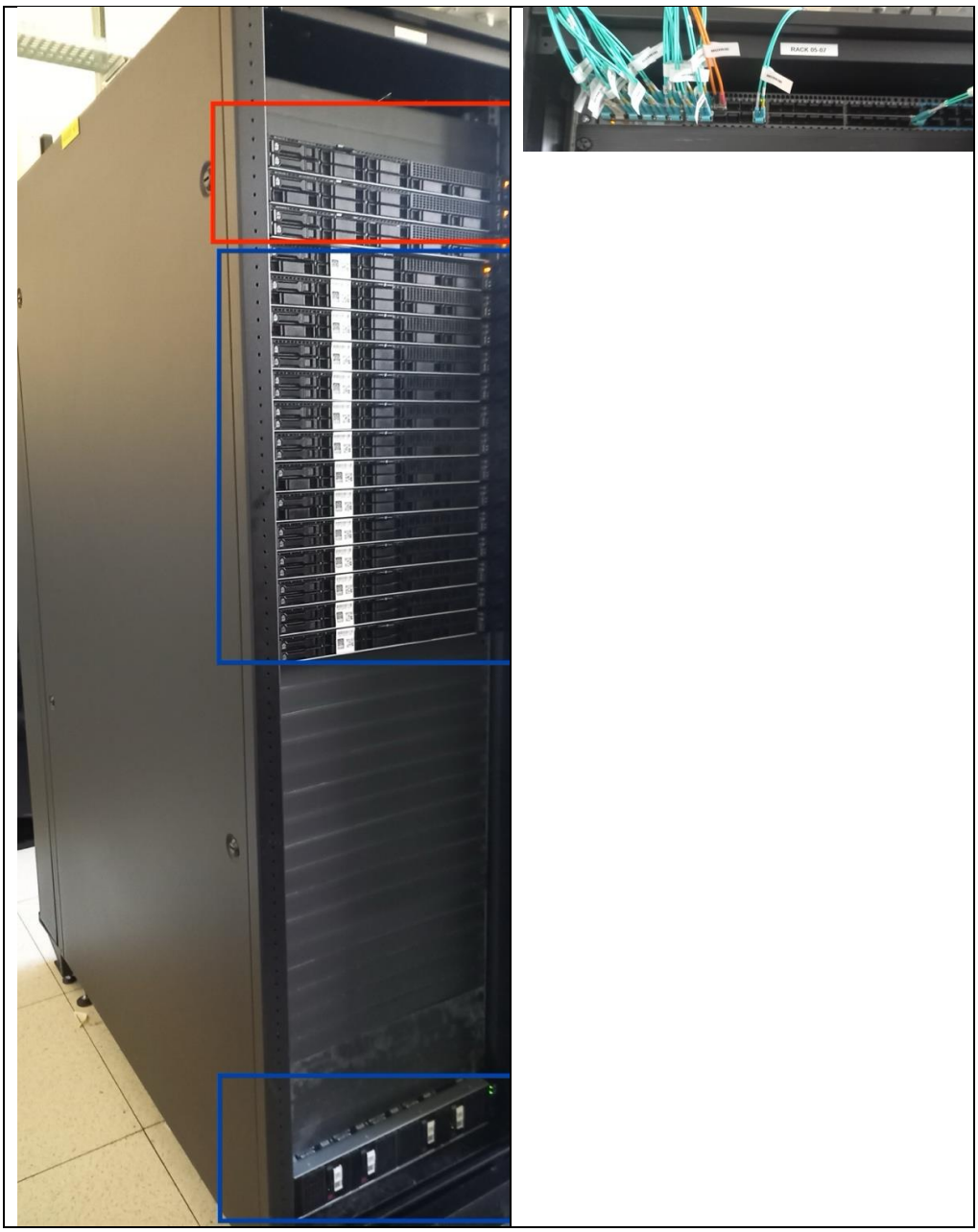
  - Deeper validation on going
    - Would it be better to have a dedicated elog entry for the tests
    - Done with an entry in the elog
      https://galserv.lnl.infn.it:20443/Agata+Electronic/6

  - On going modification of SQM2ADF to handle all possible frames produced by STARE.

Module Origin	Crystal Status Name	Mode	Type	Code	AdF Type	Version	Description
GTS Trigger Match	DATA_100_SC	DA	Data	00 Call	DA00	Simple	0	Normal Data 100 samples triggered by slow control call
	DATA_100_RP	DA	Data	01 Timer	DA01	Simple	0	Normal Data 100 samples triggered by timer (Fixed datarate)
	DATA_100_TL	DA	LTC	10 Loc	DA10	Simple	0	Normal Data 100 samples triggered by localtrigger data from long traces buffer
	DATA_100_TG	DA	Data	02 Loc	DA02	Simple	0	Normal Data 100 samples triggered by localtrigger (datapath)
	DATA_100_GT	DA	Data	03 GTS	DA03	Simple	0	Normal Data 100 samples triggered by gts validation
	DATA_200_SC	DA	Data	A0 Call	DAA0	Extended	0	Normal Data 200 samples triggered by slow control call
	DATA_200_RP	DA	Data	A1 Timer	DAA1	Extended	0	Normal Data 200 samples triggered by timer (Fixed datarate)
	DATA_200_TG	DA	Data	A2 Loc	DAA2	Extended	0	Normal Data 200 samples triggered by localtrigger (datapath)
	DATA_200_GT	DA	Data	AA GTS	DAAA	Extended	0	Normal Data 200 samples triggered by gts validation
LTb Long Traces Buffer	LT_4k_SC	CE	LTC	00 Call	CE00	Simple	0	Long Traces data 4k samples triggered by slow control call
	LT_4k_RP	CE	LTC	01 Timer	CE01	Simple	0	Long Traces data 4k samples triggered by timer (Fixed datarate)
	LT_4k_TG	CE	LTC	02 Loc	CE02	Simple	0	Long Traces data 4k samples triggered by localtrigger (datapath)
	LT_4k_GT	CE	LTC	03 GTS	CE03	Simple	0	Long Traces data 4k samples triggered by gts validation
	LT_4x1k_SC	CE	LTC	10 Call	CE10	Extended	0	4 channel Long Traces data 4k samples triggered by slow control call
	LT_4x1k_RP	CE	LTC	11 Timer	CE11	Extended	0	4 channel Long Traces data 4k samples triggered by timer (Fixed datarate)
	LT_4x1k_TG	CE	LTC	12 Loc	CE12	Extended	0	4 channel Long Traces data 4k samples triggered by localtrigger (datapath)
	LT_4x1k_GT	CE	LTC	13 GTS	CE13	Extended	0	4 channel Long Traces data 4k samples triggered by gts validation
vLTb Very Long Traces Buffer	LT_8k_SC	CE	LTC	A0 Call	CEA0	Extended	0	Long Traces data 8k samples triggered by slow control call
	LT_8k_RP	CE	LTC	A1 Timer	CEA1	Extended	0	Long Traces data 8k samples triggered by timer (Fixed datarate)
	LT_8k_TG	CE	LTC	A2 Loc	CEA2	Extended	0	Long Traces data 8k samples triggered by localtrigger (datapath)
	LT_8k_GT	CE	LTC	A3 GTS	CEA3	Extended	0	Long Traces data 8k samples triggered by gts validation
	LT_100k_SC	CE	LTC	B0 Call	CEB0	Extended	0	Very Long Traces data 8k samples triggered by slow control call
	LT_100k_RP	CE	LTC	B1 Timer	CEB1	Extended	0	Very Long Traces data 8k samples triggered by timer (Fixed datarate)
	LT_100k_TG	CE	LTC	B2 Loc	CEB2	Extended	0	Very Long Traces data 8k samples triggered by localtrigger (datapath)
	LT_100k_GT	CE	LTC	B3 GTS	CEB3	Extended	0	Very Long Traces data 8k samples triggered by gts validation
Spectra Buffer	SPC_100_SC	FA	SPC	01 Call	FA01	Simple	0	Short 100 bin spectra for all channel trigger by slow control call
	SPC_100_RP	FA	SPC	02 Call	FA02	Simple	0	Short 100 bin spectra for all channel trigger by timer
	SPC_4kp_SC	FA	SPC	10 Call	FA10	Simple	0	Long 4k bin spectra for one channel trigger by slow control call
	SPC_8kp_SC	FA	SPC	A0 Call	FAA0	Extended	0	Long 8k bin spectra for one channel trigger by slow control call
System	IDLE				BEDD	Simple	0	IDLE empty message sent each IDLE TIME (set by slow control)
	ERROR				EEEE	Simple	0	On call (trigger/slow control) system was on error
	SYSOFF				DEAD	Simple	0	On call (trigger/slow control) system is off (Digitizer/Readout)

- Other Phase2 related developments: DAQ-Dev Box @ Orsay
    - Operational !
        - Installation/tests of new tools (redis,InfluxDB,docker) OK
        - First benchmarks performed on the new machines bought in 2023-24
            - More CPU / RAM oriented
            - Confirmed about 8khz current psa thanks to more multi-thread
            - Parallel processing added with few 10 kHz reached

    - Next step is to have a full DCOD environment operational
        - More network benchmarks oriented



PSA and Tracking R&D (A. Boston)
No specific report
Performance and Simulation (M. Labiche)
No specific report
Financial Reports (B. Million)
No report

Dissemination (J. Nyberg) : no news.

AGATA Week https://indico.in2p3.fr/event/32956/
Indico ready, registration open; Agenda on-line

AOB : none