AGATA AMB Phone conference 26th November 2024

Sujet : AGATA AMB Nov 2024

Apologies:

LNL Status (J.J. Valiente-Dobon – A. Goasduff)
Minutes status AGATA@LNL 26/11/2024

- 6th Pre-PAC report:
    - 10 new projects + 1 resubmitted one, for a total of 88 days. Three LoIs for measurements with EXOTIC. The high-spin commissioning experiment was thoroughly discussed and tomorrow 26th there will be a dedicated meeting organized by Labiche.
    - The deadline for the coming LNL PAC will be 15th of December. The PAC will be 23rd-24th of January 2025.
    - Still time to send a test experiment for the TP and V2 electronics if considered feasible.
    - During the WS the first results of a RIB production of SPES were shown by the project manager. Confirmed all 2025 only TANDEM and later PIAVE+ALPI for the beginning of 2026 with U beam but also other beams that might be requested by the community.
- Status of the campaign:
    - Start of the campaign was difficult from the accelerator side, source issues and instabilities which prevented us to before the first and second experiment. The Dy Coulex, started well with the hardware trigger set and working properly on the DANTE OR SPIDER but was stopped after a few hours. We had to increase the latency of the GGPs to accommodate for the slow trigger signal of SPIDER (digitizers VX2740)
    - Currently running the last long experiment of this campaign. We have left a small test of 1 day for the beam on/off with the external trigger gate and the self-calibration experiment with in-beam data for 1 day and 1 week of 88Y source. 88Y source is currently being delivered to LNL.
    - Three experiments are passing in backlog (18 days BoT + 10 days beam preparation)

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- Status of the Detectors:
    - 12 ATCs are mounted, 33 capsules were taking data. 3 digitizers are still waiting to have the firmware of the control card reprogrammed (hoping it will solve the issue): 05B/07C/08C.
    - The ATC which was supposed to be replaced before the campaign but was postponed at the last moment because of FET issues on the new ATC (now solved) will be unmounted at the end of the self-calibration measurement and replaced.
- Status of the Infrastructure:
    - The heat exchanger will be installed last week of December. All pieces at LNL.
    - HV: the new AGATA crate was tested and configured. We found issue with 4 HV boards which were identified with the negative polarity by the crate but delivering positive HV. Issue is now corrected, new FW flashed on all boards (programmable ramp down in case of EXT-DIS)
    - Found a detector patch box with water damaged on the pre-amplifier LVPS (ATC01). Box was changed and DB9 connector of 01C was repaired. Crystal is back in the acquisition.
- Status of the mechanics:
    - For the ALPI 2026 campaign, the PRISMA team is working on the mechanical integration of the second arm of PRISMA (already used in 2014, see F.G. PhD thesis (2017) and PRC (2018) and E.F. NIM (2018)). It seems to be feasible but only with a fix angle between PRISMA and the second arm.
    - Mechanical integration of the needed ancillary detectors for the EXOTIC beamline is on-going after the requests made at the Pre-PAC
    - Mechanical integration of PARIS with AGATA at zero degrees is being finalized. The designer (Christine le Gaillard, IJCLab) will be in Legnaro on the 14-15 January 2025 to discuss the final details.
- Status of the electronics:
    - During the current experiment, the electronic was very unstable. Full reboot of the DAQ/Electronic will be done on the first days of December. We went down to 31 crystals taking good quality data:
        - 1 off because a segment card was responding to ccping and not able to initialize the digitizer (01A – GALILEO Digitizer)

        - the other one, the first segment board is very unstable (14B – GALILEO Digitizer)

    - Found procedure to recover the core card not answering to ccping (works 4 times / 4 at the moment) (EMC issues?)
        - Switch off the digitizer
        - Disconnect the core MDR cable
        - Switch ON the digitizer
        - Initialize
        - Reconnect core MDR

    - Padova agreed to give us a 2 months FTE to help on the maintenance and mounting of the electronics. First task of the technician will be to reprogram all the GTS mezzanines from the V0 into fifo to prepare the tree for the V2.

    - The GGP trigger boards have been tested and we have a new release of the GGPs FW to work with it: single ended signals are working well but we have an issue on the LVPS one. Roberto Isocrate will work on it. Production of the board expected for the beginning of 2025. The new FW allows to output the local trigger of the GGPs as a logical signal (TTL or LVDS) to check the coincidences.

    - Modification of the GGP slow control to enable/disable the Fast Reset on the core pre-amplifier was done. → need to implement it after all resync7

- Status of the DAQ:

    - Modification for very low validation rate experiments might be needed, discussion started with the AGATA DAQ team (EXOTIC beam, but also in the future for SPIRAL1, …).

    - We still observe the issue of data loss at the end of the run when validation < 200Hz

    - We have mounted a test bench for the NEDA NUMEXO2 for their integration into XDAQ, to avoid installing the GANIL version of NARVAL @ LNL which would require the intervention of the GANIL Acquisition group. It will be the occasion to solve the NEDA Xilinx driver issue observed in 2018 at low rate. Output of the PSA Filter written in ADF to avoid the encapsulation of the MFM in ADF which was doubling the size of the frame in previous campaign → Definition of a new ADF frame for the DAQ group.

ASC Report / ASC Matters (M. Gorska)

- More to do for the 2025 review. AMB document to be prepared for the next ASC in T1 2025. ACTION : EC to draft the document with the Financial section by BM.
- ACC has to develop the scientific achievement and the next physics case, even in the reduced solid angle by 2030 in line with ARRB minutes

ACC Report / ACC Matters (S. Leoni)

- Action on going on the LNL updated core list autho

GSI Status (K. Wimmer)

No specific report

REPORTS FROM THE WORKING GROUPS

Detector Module (H. Hess)

New detector delivered C023; This is the 3rd GSI detector; the commitment was a delivery before the end of 2024. All GSI detectors delivered on time.
70 detectors in the collaboration.
B006 annealed. This is the first of the second batch but a drop to 70% relative efficiency is measured !

Infrastructure (B. Million)

Please have a look to the Host Lab document !!!!

Front End Electronics (A. Gadea)

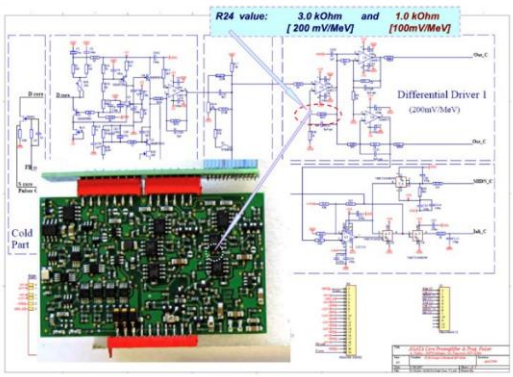
Coordination: last Electronics W.G. VC was on November 14th 2024,
next Electronics W.G. VC meeting on Monday December 9th 2024 at 10:00 CET, 9:00 U.K.

Pending actions:
-Meeting with J.Collado, GANIL, LNL and Padova Colleagues: brainstorming on GTS alignment protocol pending on the maintenance contract.

Status at LNL (A.Goasduff et al.):
33 of maximum of 39 channels working presently in the setup.
Working with Stefano Capra and Alberto Pullia to be able to disable the fast reset of the preamp from slow control; presently the default is disable on core and enable on segment. The idea after that is to use the pulser in the preamp for testing.

Slow control

- pca9671Device SLC already implemented in the GGP server
- Adding the control of the P07:
  - Useless for the segment card (no NAND chip between pca9671 and the MDR)
  - Only effective on the core card.
- Slow control tested with the multimeter,
  0V FR enable ; 3V FR disable
- P07 is getting reset at each resync of the ADC, default value --> FR disable
- To check the fast reset on the core pre-amplifier it is necessary to add a 50W tap on the +5 and/or -5 input of the patch box. Otherwise, the fast reset is disable by default on the pre-amplifier.



Preamplifier Fast Reset control

Heat exchanger installation in on-going. Company came with all the pumps. They will mount everything on a (transportable) platform

We have seen again some core cards stopping to work. They are recovered with the following sequence:

1. Switching off the digitizer
2. Disconnecting the core MDR cable
3. Switching on the digitizer
4. initializing the digitizer

Core problem seems to be caused by something from the preamp on the MDR cable.

33 channels working with 3 digisters in the lab wa

Trigger board add-on ok for the single ended input but issue with the LVDS one (Roberto lsocrate will check)

Action: the Phase 1 Control card firmware is missing. Actions to find it started.

DIGIOPT12 (A.Pullia):
3.7.1 version tests completed.

140 segment cards have been constructed plus 33 core cards.
117 segment cards tested and delivered in 2024 and also 25 core cards.
8 core cards and 22 segment cards untested.
Production yield is very good- some cards needed rework but all have been useable.

Now we will switch to 3.7.1 which has the noisy channel corrected in PCB- all future production will be 3.7.1 . Until now, in version 3.7 it was necessary to correct the noisy channel by hand.

Fast reset selector bit is set in digitiser and sent through MDR to preamp. It can be enabled and disabled in the core but the segments can't be disabled except by adding a resistor through MDR connector.
Until now the chip to send the bit from digitiser to preamplifier has not been mounted.

PACE Status (J.Collado, reported by A.Gadea and V.Gonzalez)
Hardware:
PACE v58 PCB delivered almost 2 weeks late. 10 boards were not OK so total 90 will be complete by end of this week. 80 are available; funding is 50 GANIL, 40 IFIC.

Components for 90 boards have been procured and by Feb 2025 there will be enough components for 140 boards.
Purchasing orders for the mounting of 15 PACE-CAP-v100-t58 by Valencia done.
The GANIL order for the mounting of other 55 PACE-CAP-v100-t58 is being processed by the GANIL administration.
Delivery time has extended from 4 to 12 weeks for the PACE-CAP-v100-t58 boards.

Discussion on the FAT and CAT for he production has been completed.

We have to provide the SD with the firmware and software, the GTS SFP transceiver and TE0808 SoM to Teydisa, such that they can do the FAT.

FAT:
- Conductivity test of the board
- Power up test
- Programing the control and boot FPGAs
- Electrical Test
- Slow control ping test
- Testing the receiving Slow speed lines,
- Testing the high speed lines to the FMC
- Loopback of the GTS hardware

This FAT tests the full boot, programing start-up, data path and GTS hardware.
CAT:
In Valencia, the boards will be mounted in a complete test setup, including DIGIOPT12, and possibly STARE and channel data path and noise test will be performed.
ETSE and IFIC Valencia, as part of the AGATA Electronics W.G., will provide complete report of the CAT test performed in Valencia for the delivered batches.

Partial deliveries on batches with 15 to 20 boards, will be done.

Firmware:
packager latest test files are dated 29/10/24. Olivier Stezoswki and Guillaume Baulieu still seeing issues with formatting channel number and ADF formatting.

http://gal-serv.lnl.infn.it:20443/Agata+Electronic/12

Javier Collado has been simulating the code since the last failure to solve the issues. He has found the problem thanks to the simulation, it is heavy but everything is much clearer. In simulation now comes out the exact format of AdF. The problem was that the signal that marks the intermediate data between odd and even channels so that it is correctly aligned in the header (as in PACE are 64 bit and adf is at 32 bit) was not responding correctly. This weekend he started measuring and two new files have been produced:
“Captured data set with AGATA Ph2 and Co60 Source: 2800 and 2801 AdF normal “

http://gal-serv.lnl.infn.it:20443/Agata+Electronic/13

Addition of new energy code has been added to the firmware contract and the contract is being process via a public call for tender (necessary because of the cost).

Revisión of the Maintenance Contract

Implementation of a new energy IP block on PACE system architecture.

Implement the new energy IP algorithm from NPG, STFC Daresbury Laboratory, provided by Client, into the system architecture as a new element of the Datapath Block IP. The input of the energy IP algorithm provided must be adapted to the dF (dataflow) format of the PACE firmware, and the energy output to agt_evt, to ensure compatibility with the system. Both the

dF format and agt_evt are defined in the AGATA PACE Firmware Base10 (Ph2-RS024A) at sections 10.1.1 and 10.1.3, respectively. Additionally, update the AdF packager formatting in the AGATA PACE Firmware Base10 to send a new 16-bit parameter per channel for each event.
This work shall include updating the Datapath IPbus IP block to control the new energy IP algorithm registers and the corresponding software control counterpart. A total of 4 person-days of work person-days from the commencement date of this Agreement is necessary.
Deliverables: An updated version of the Base10 Firmware code for the AGATA Ph2 PACE SOM FPGA, including a compiled version in the Git repository. A documentation manual outlining the implementation of new energy blocks for the Base10 Firmware. Updated documentation detailing the control definitions for the new energy registers.

PSU and Mechanics: (V.Gonzalez)

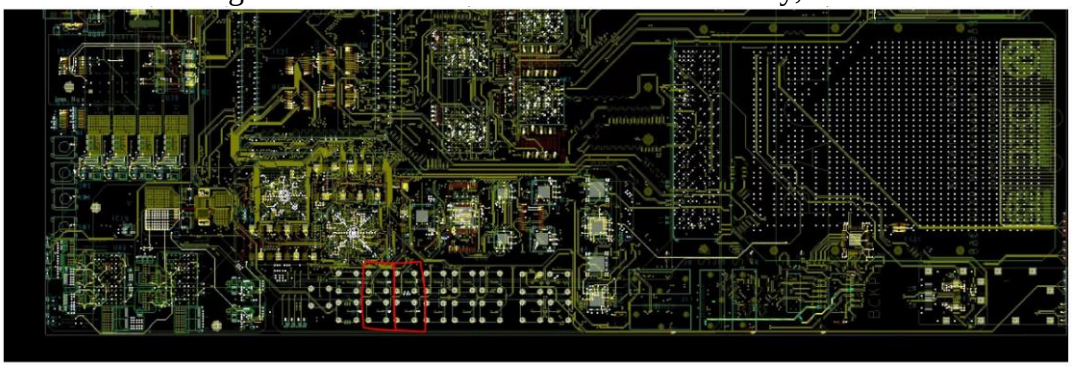
Mechanics production is proceeding normally
On the signal backplane production there was a problem with one component missing which was solved and the signal backplanes will be delivered soon.

PSU problem was shown to be related to grounding, some PCB changes were made, and new design will be ready to go to production this week. 50 will be produced; components exist for 50 but some are obsolete and replacements are needed to go to production of 100 unit.

Thermal tests still under way with help from Nicolas.

Trigger connector has been allocated to allow the FPGA to be connected to a direct (level 0) trigger.

Any of the pairs U12/U13, U15/U14 or U20/U19 would work, in principle it should be a differential signal for the clock tree to understand. Ideally, either of the last two



There are other possibilities but require to add small PCB's to add the connections and have been, in principle, discarded.

STARE Status (N.Karkour, X.Lafay)

All STARES are produced and all STARES that are fitted with SOMs have been delivered.

The manufacturing company has used some tapes of resistors that are incorrectly labelled with their value. 27 cards are working with SOMs and 10 with SOMs are not working (probably resistor problems- 2 of them have this problem which has been seen 3 times now and X.Lafay is working with the test of the other 8 cards).

AGATA simulation bay will help DAQ, UDP decisión etc- ongoing (IPHC, Lyon, Orsay working on this). Now extending the simulation system to include a complete PACE card when available (still using a prototype)

STARE SOMs procurement plan was discussed, but it is messy (many small orders). Expecting a 2nd procurements in 2026/27.
Noted that SOM production batches are not all identical so better to buy in bigger batches to avoid multiple firmware versions(e.g. to accommodate different SOM PLLs)

Software (Ch. Bonnin, N.Dosme)

Working on the test bench as noted in STARE report. Improvements are being made to the topology manager as well.

New processing firmware (Moschos Kogimtzis)
Implementing the energy block. Format for top level VHDL is now agreed with Javier and extra field has been added to record the number of sample used (reduced in pileup situations).
Should be pluggable. Still not clear how to integrate the CFD because the current version of the code has an option to bypass the CFD.

News Testing and Production of phase 2 electronics:

PACE: The first boards should be delivered in December or latest early January.
If the GANIL tendering goes ok, after January, we expect to receive batched of 15-20 boards every 2-3 weeks.

Order of 20 more PACE-CAP-v100-t58 boards possible as soon as the funds from Spain are available if the management agrees.

Data Processing (O. Stézowski)

Coordination:

No regular meeting since last AMB. Next one is scheduled 9/12/2024
Page dedicated to current actions here

Note:
NuPEcc Long range plan published.
ACC to be aware of in particular the Open Science/data section
Beginning of next year I'll try to prepare the questions to be discussed in ACC about this

Production:

- RAM memory to upgrade all current machines
  - Ordering done 16/05/2024
  - Delivered to LNL
- CEPH upgrade
  - 3 new (core) disk arrays to be bought. 2 for CEPH + 1 to be used as anodeds6
    - About 36 000 euros … waiting for final quote from HP
    - should bring CEPH close to 400 [+100] To of safe disk [replica3]
    - hopefully at LNL beginning of September
    - NOTE: 2 other backup systems available on site
      - ancillary disk of LNL,
      - one old globicephala refurbished
  - Order done, waiting for delivery
  - Delivered at Orsay
    - CORE Money : 37 663.59 euros.
    - Under configuration and sent to LNL once ok
- Many issues on analysis1
  - Decision at AW to buy a c6400 like unit (4 nodes using 2U in the rack)
  - Quotes in progress at the speed of HP company …
  - Ordered by GANIL 14/11/2024
    - OC: 17,741.88 euros
    - Waiting for delivery @ Orsay (cannot directly to LNL)
    - Configuration to be done before sending to LNL
- Host lab document
  - Better to wait for tests with the dev daq box
- To help getting data from the grid
  - Docker provided to be used as Grid User Interface
  - https://agata.pages.in2p3.fr/handbook/data/grid/
- Issues with the VOMS serveur which delivers permissions to access the GRID
  - Raised by Johan @ the last AMB
  - We had a meeting @ CCIN2P3 7/11/24
    - Serveur hosted@CC as Virtual Machine, can run as long as needed
    - … but operating system not maintained anymore …
    - … thus likely to be stopped in case of security
    - As for HEP we need to move to another identification system IAM
    - Cannot be hosted at CC
      - We have a meeting next week to see for a solution@Orsay
- Next Data Analysis School scheduled in January in Lyon (InTrans support)
  - https://indico.in2p3.fr/event/34092/overview
  - 16 participants … with speakers
- Solution for experiment with EXOTIC beams under study
  - Modifications of the agapro package to be performed

Phase 2 Developments: Nothing to report

- NARVAL still to be installed on the mini-DAQ box @ Orsay
- We have been informed this morning of new run produced by PACE→to be qualified

PSA and Tracking R&D (A. Boston) (apologize)

Performance and Simulation (M. Labiche)

Analysis of the high energy test on-going.

Financial Reports (B. Million)

Dissemination (J. Nyberg) : no news.

AOB :

Maintenance of the web site; We need to identify a person to replace Johan in this activity.