AGATA Hybrid Preamplifiers with Pulser

ATC

Contents

Introduction

Each Germanium crystal of AGATA will be read out by 36 segment preamplifiers + 1 core preamplifier, connected to flash ADC's through 10-m shielded-twisted-pair cables. The role of preamplifiers is crucial to achieve a good system performance and preserve pulse-shape integrity. A list of requirements for the preamplifiers is shown in Table 1.

Table 1

Type	*Description*
LN	Low noise (gamma spectroscopy grade)
WB	Wide bandwidth (risetime of 20ns)
SFT	Short fall time (50us)
LP + LN	Low power consumption of the cold FET (<20mW) maintaining LN
HS	High Stability of the gain
DO	Differential output buffer
RDT	Reduced deadtime, even with a background of energetic particles (10 to 100 MeV)
CO	Compactness

A. Pullia and G. Pascovici for the AGATA preamplifier group

Solutions to address each of these issues have been discussed in the preamplifier group meetings. Segment preamplifiers are grouped with a three-per-board granularity. So, twelve triples will read out all 36 segments of a crystal. One core preamplifier is instead mounted on a single board. A calibration pulser will be installed on the core-preamplifier board, and used to inject a common test signal to all segments through the segment bulk capacitances. A new fast-reset technology is used in all preamplifiers to reduce the deadtime when the ADC gets saturated.

Choice of the input FET

The choice of the preamplifier input FET is one of the most critical issues of this development. In fact all FETs work cooled in the cryostat with a maximum power budget of 20 mW/FET. Nevertheless the FETs must provide the typical low-noise performance required in gamma-ray spectroscopy as a prerequisite. Note that the typical power consumption of one of such FETs, as observed in most Germanium detector setups, is three times as large. After tests performed in Milano and Cologne we have found that the *n*-channel FET model BF862 manufactured by Philips is adequate. In fact it provides a noise of 0.9keV fwhm on the pulser line while working at 120K with a drain voltage of 2 to 2.6V and a drain current of ≈8mA, i.e. a power consumption <20mW. The results of some of these tests (from D. Weisshar, May 2003) are summarized in Table 2.

Table 2

Shaping time [us]	*Line energy [MeV]*	*Line width [eV fwhm]*	
		IF1320 @ Vds=5.6V	BF862 @ Vds=2.6
3	0.122	1.07	1.08
	1.17	1.99	1.97
	1.33	2.15	2.13
6	0.122	0.98	0.93
	1.17	1.92	1.88
	1.33	1.97	2.02

Circuit architecture

As shown in Fig.1, the preamplifiers have a three-stage structure, comprising a charge-sensing loop (which comprises the cold devices), a passive P/Z stage, and a differential output buffer. An additional de-saturation circuitry is used to swiftly reset the preamplifier when an energetic event or a burst of piled up events put it into saturation. It is also possible to measure the amplitude of the energetic event from the reset time (Time Over Threshold, TOT measurement) as given by the width of the Schmitt trigger comparator signal.

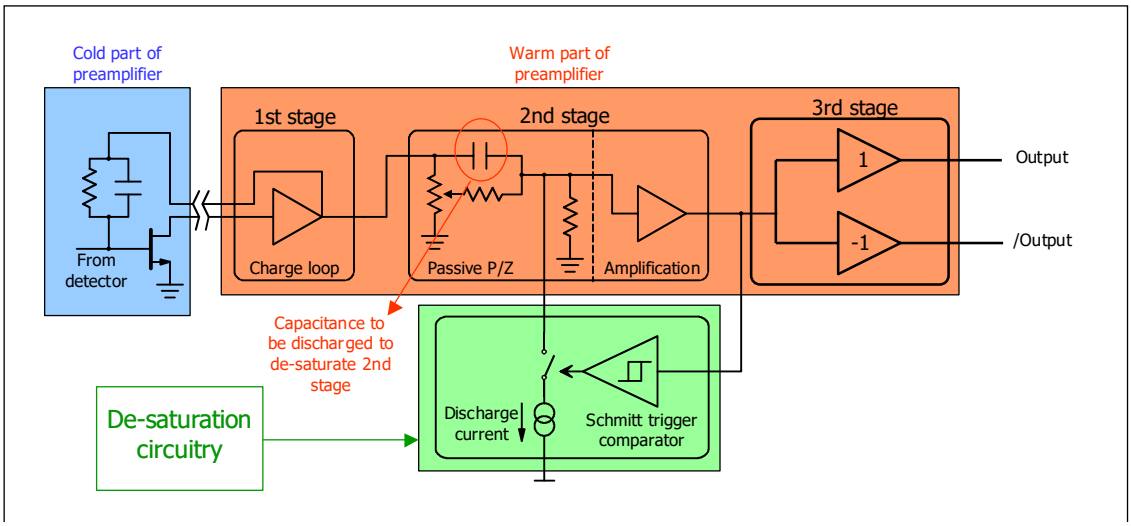

Fig. 1

The simplified schematic diagrams of the three stages are shown in Figs. 2, 3, and 4.

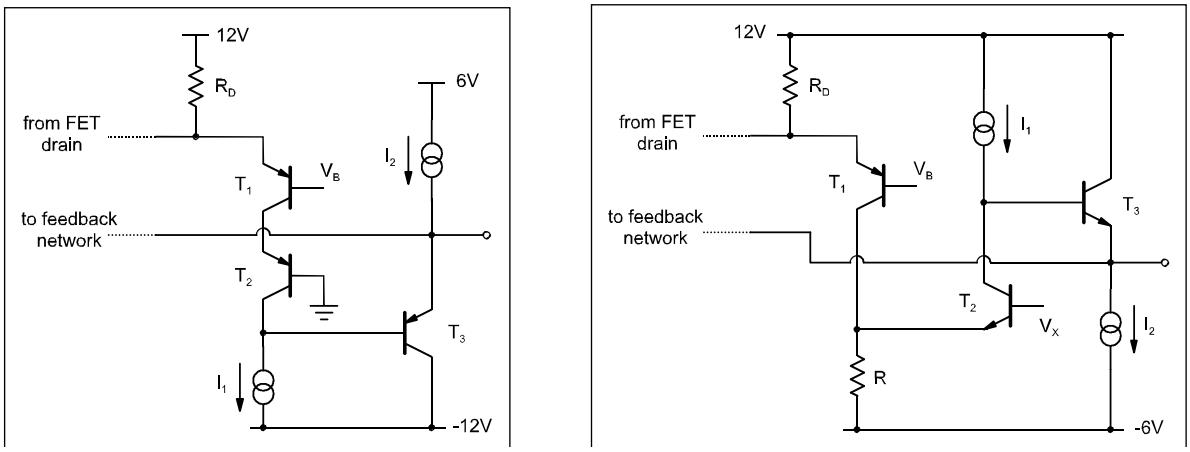

Fig. 2. First stage of segment preamplifier (left) and core preamplifier (right). A 0.5-3pF capacitance (not shown) from the base of T3 to ground is used for loop stabilization.

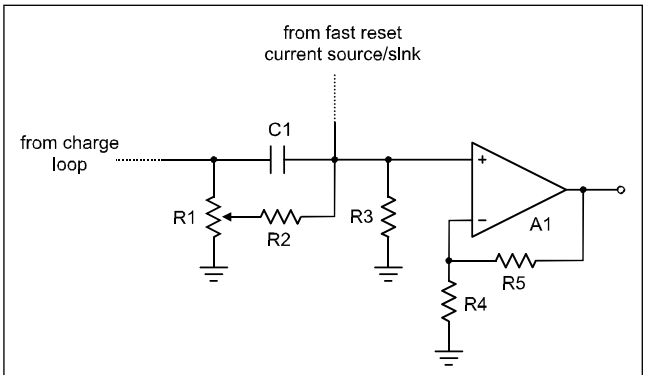

Fig. 3. Passive P/Z stage of segment preamplifiers as followed by the gain amplifier. For the core preamplifier A1 is inverting.

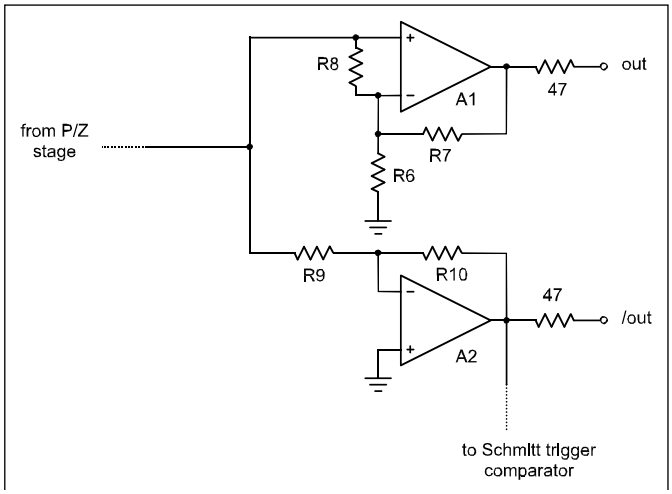

Fig. 4. Balanced differential output stage.

Active fast reset

A new fast reset technology is used to optionally reset the 2nd stage of the preamplifier when the input signals cross over a preset threshold. This is useful to reduce the preamplifier dead time brought about by energetic events that could hit the detector. The fast reset device can be excluded by pulling up a control input signal. As already mentioned the amplitude of the energetic event can be measured from the reset time, or TOT, as provided as the width of the comparator signal (named as "Inhibit signal"). Using this method an energy resolution below 0.05% at 50 MeV of equivalent energy can be obtained. The measurement of the Inhibit signal width is to be performed with an accuracy of ~1ns using either a high frequency clock or interpolation techniques. An example of the signals seen when using the fast-reset mechanism is shown in Fig. 5.

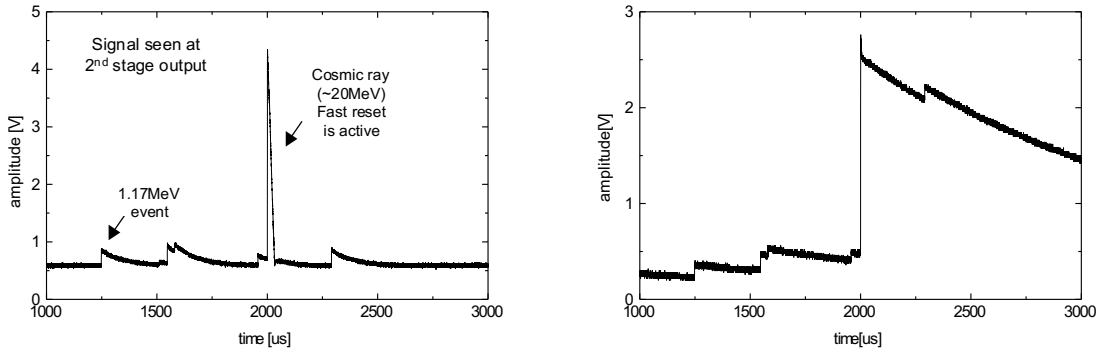

Fig. 5. Signals delivered by a prototype preamplifier with fast-reset device (from A. Pullia and R. Isocrate, Jan 2004). Left side: output of 2nd stage. The fast reset is visible on the 20 MeV cosmic ray. Right side: corresponding signal seen at the 1st stage output. Note that no reset occurs on it.

Control of the fast reset device is made statically or dynamically through a single wire called SHDN. One can handle the SHDN statically keeping it permanently up or down (see following points i and ii) or dynamically (see point iii):

i) Keep the SHDN low to make the fast reset work autonomously. Whenever a signal crosses over a preset threshold the fast-reset transient begins. The fast reset transient

automatically stops as soon as the zero-volt point is reached. The typical triangular shape shown in Fig. 5 (left) is thus obtained. The shape could become trapezoidal for very large signals.

ii) Keep the SHDN high to disable the fast reset.

iii) Try to handle the SHDN dynamically to control the fast reset from the ADC module. At the beginning keep the SHDN high (fast reset disabled). Then, if an over-range condition in the ADC is detected (which means that the signal is too high) pull the SHDN low. This will force the fast reset to begin. As soon as the SHDN is kept low the fast-reset mechanism will be working autonomously, exactly as in i). So it will automatically stop when the zero-volt point is reached. Of course if the SHDN is pulled up before, the fast reset transient will be over before reaching the zero-volt point. In any case the control cycle is over when the SHDN is pulled up, and the system is ready to begin a new cycle as soon as another over-range status occurs.

Programmable Pulser

The Programmable Pulser (PP) is installed in a side of the core preamplifier board. It is a precision pulse generator designed to test the stability and linearity of the system, as well as to estimate the resolution of the segments. The output signal of PP is dc coupled to the source pin of the core j_FET through a resistor divider consisting of a 48.5 Ohm resistor and a grounded 1.8 Ohm resistor. Thereafter the signal reaches each of the 36 detector segments following the path Csg(core)_HV-Coupling-Capacitor_Core-to-segment-bulk-capacitance. A block diagram of the PP is shown in Fig. 6.

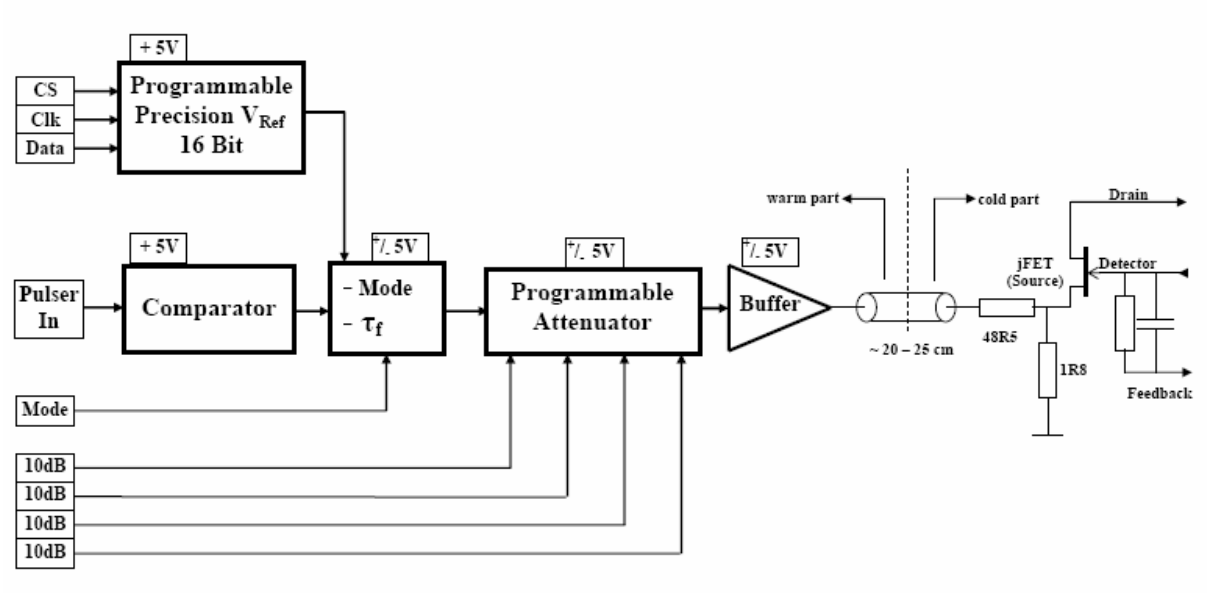

Fig. 6. Block diagram of the Programmable Pulser.

The PP consists of three stages, a programmable reference voltage (Progr_Vref), a chopper triggered by an external signal (Pulser In) and a programmable attenuator which comprises also an output buffer stage (Atten_Buf). The structure of the programmable reference voltage stage is shown in Fig. 7.

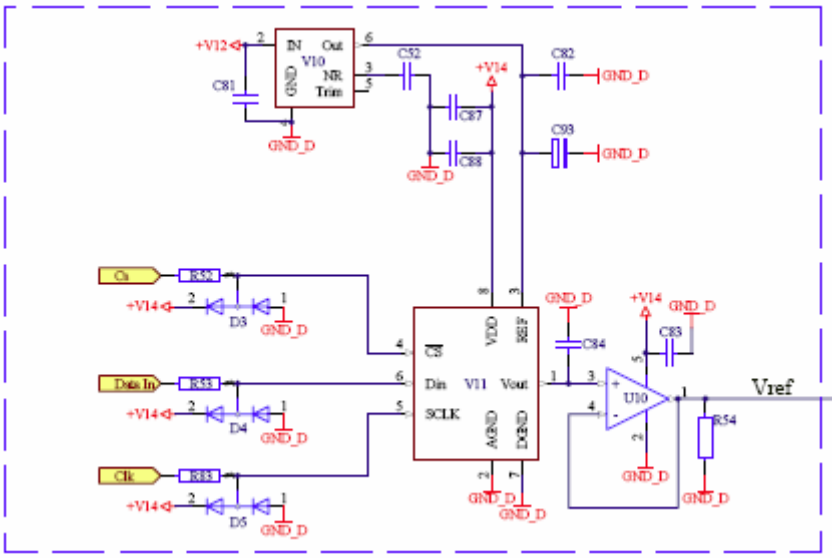

Fig. 7. Programmable reference stage.

The MAX6341ESA (or equivalent ADR444BRZ) is an ultra high precision voltage reference of 4.096 V with a very low temperature coefficient (1-3 ppm/ °C), very low noise (1.5 µV pk-pk) and long-term stability of 30 ppm/1000 hr . The AD5541CR is a 16 bit (+/- 1 bit) serial input, voltage DAC. Data is written to it in a 16-bit word format, via a 3-wire industry_standard serial interface (CS, Clock, Data_In)

The structure of the Chopper_Pulser stage is shown in Fig. 8.

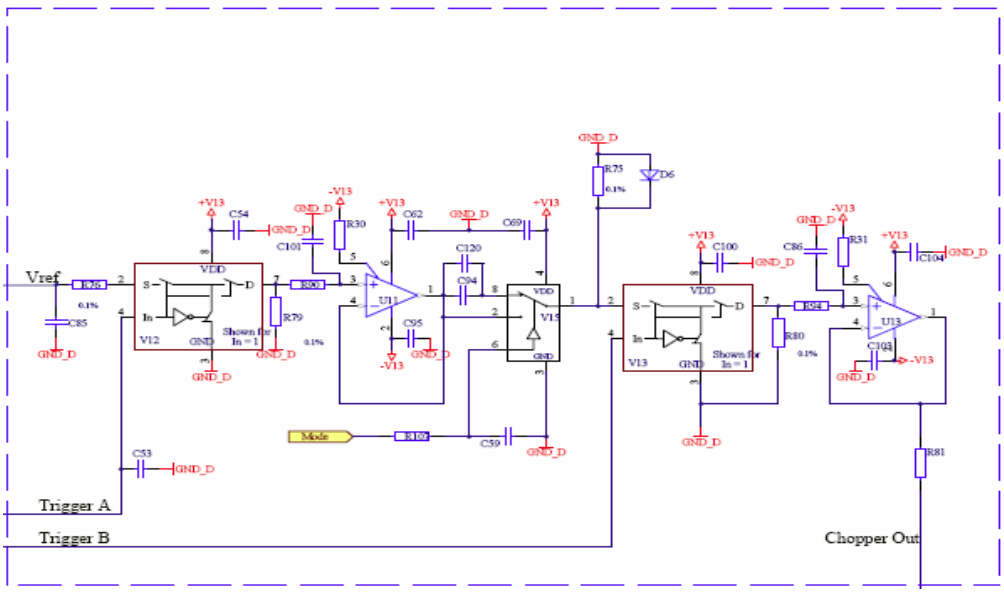

Fig. 8. Chopper stage.

The Chopper builds around ADG751 analog switches, and is triggered by an external LVCOS signal (optionally, LVDS signal). The trigger threshold is set to Vos = 1.25V. The chopper mode of operation is programmable, i.e. a rectangular or an exponential-decay mode can be selected (the decay time is only factory adjustable in the range of 50us to 1ms). This stage comprises also a linear gate circuitry in order to select only one polarity, if the exponential-decay mode was selected.

The programmable attenuator & buffer is shown in Fig. 9.

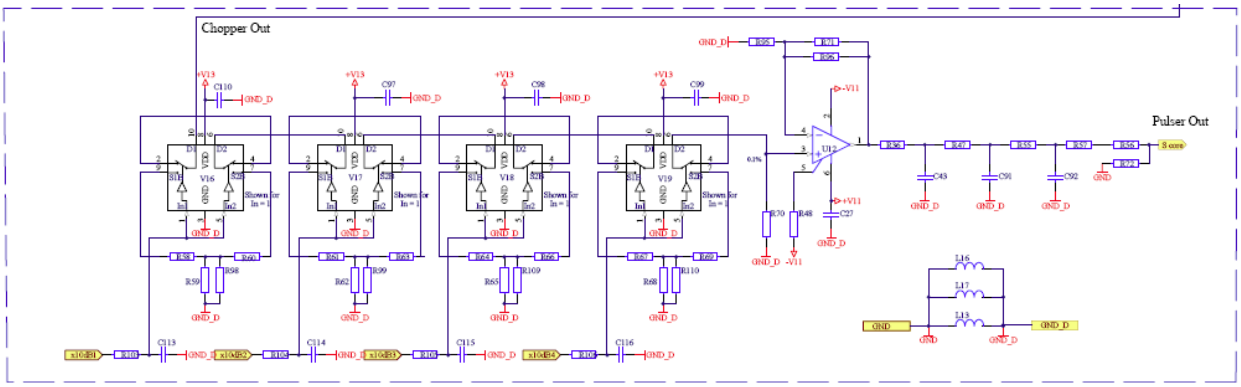

Fig. 9. Programmable attenuator.

The programmable attenuator consists of four stages, each of 10dB thus the coarse attenuation factor can be selected between 0 and 40 dB, with a granularity of 10 dB. The buffer stage (LT1815) can drive a maximum DC current of 20 mA onto a tiny load resistor with a nominal value of 1.8 Ohm, placed in the cryostat between the source pin of the core jFET and internal GND .

Size and pinout (segment preamplifiers)

In Fig. 10 and 11 the size and pinout of the triple segment preamplifiers is shown. The maximum thickness of the board (including components) is 7mm. The lateral trimmers for P/Z adjustment are mounted as shown in the Figure to permit phisical access.

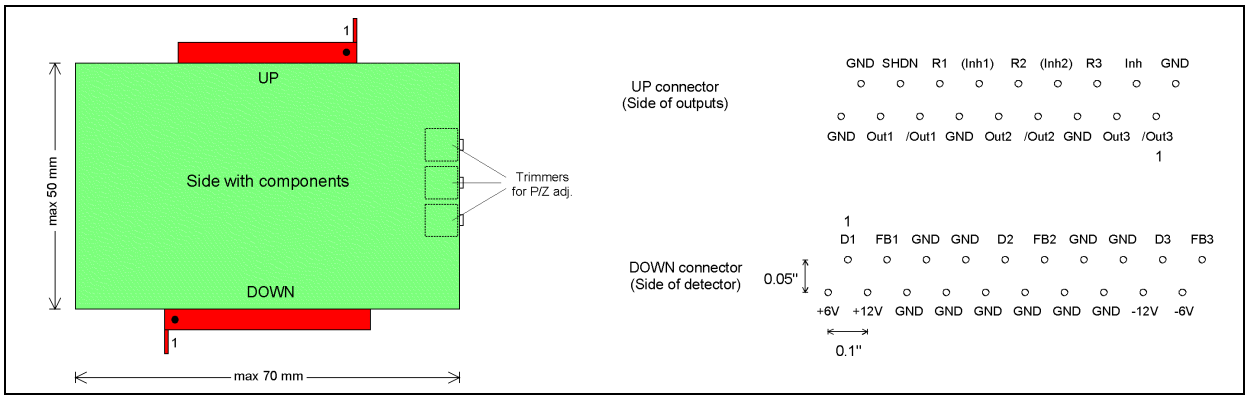

Fig. 10. Signals in parentheses (Inh1) and (Inh2) as well as R1, R2, R3, are shown in the pinout but are not implemented in this version.

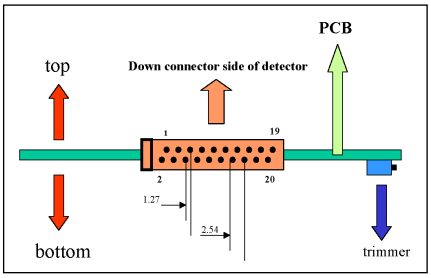

Fig. 11. Bottom view of the board.

We have adopted polarized "Micro-Match" connectors from Tyco Electronics of the type "male on board", shown in Fig. 12. The DOWN connector has 20 vias, the UP connector has 18 vias. Note that a hole must be drilled out on the motherboard so as to house the polarization plastic flange shown in Figs. 10 and 12.

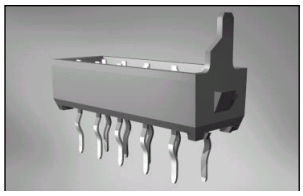

Fig. 12

The DOWN connector serves all connections to the detector (FET drain, feedback) and is also used to provide power supplies (±6V, ±12V) and grounds. The UP connector is used to transmit the analog output signals and transmit/receive the digital service signals. The board plugs in over a fixed motherboard onto a 20-via "female on board" connector of the type of that shown in Fig. 13. A flexible motherboard with a similar female connector (18 vias) plugs in onto the upper part of the preamplifier.

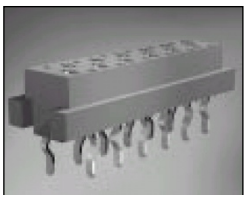

Fig. 13

A complete list and description of the symbols shown in Fig. 10 is reported at the end of this document. In Fig. 14 a photograph of two prototypes of a triple preamplifier is shown (courtesy of B. Cahan, GANIL, and A. Pullia, University/INFN Milano).

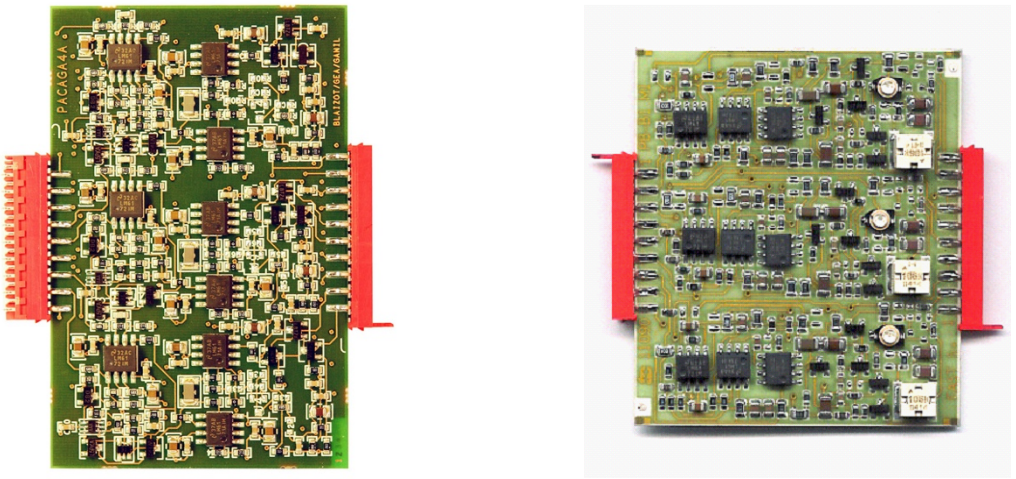

Fig. 14. Photograph of triple segment preamplifier (front view), as developed at GANIL (left) and Milano (right). The P/Z trimmers are mounted on the back and not visible in this picture.

Size and pinout (core preamplifier)

The core preamplifier is built in two versions, a standard version with only one stage with a conversion gain of ~ 100 mV/ MeV ("single core") and an advanced version with two conversion gains, namely one with ~ 200 mV/MeV and another one with only ~ 50 mV/MeV ("dual core").

In Fig. 15(a) and 15(b) the size and pinout of the core preamplifers + pulser are shown, the version with single core in Fig. 15(a) and the version with dual core in Fig. 15(b), respectively. The maximum heights / width are 45 x 62 mm for single core and 45 x 70 mm dual core, respectively. The maximum thickness of the boards is 8 mm.

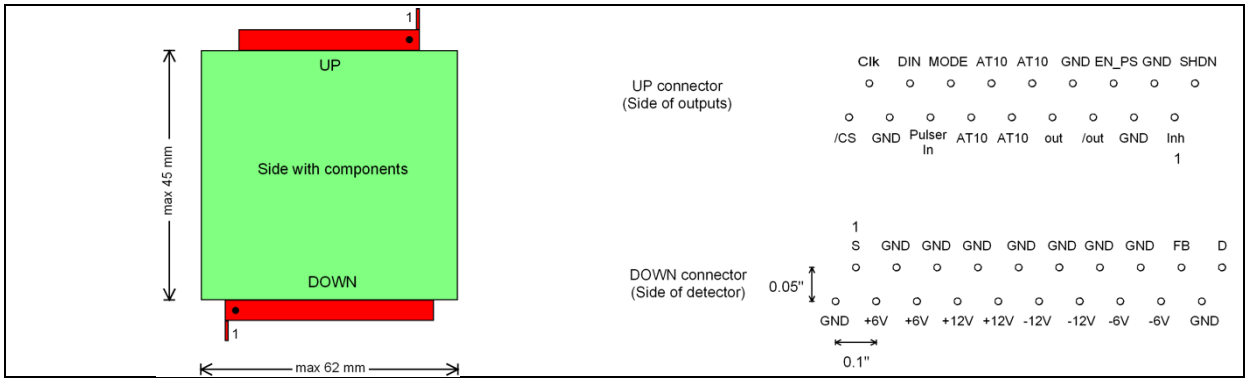

Fig. 15(a)

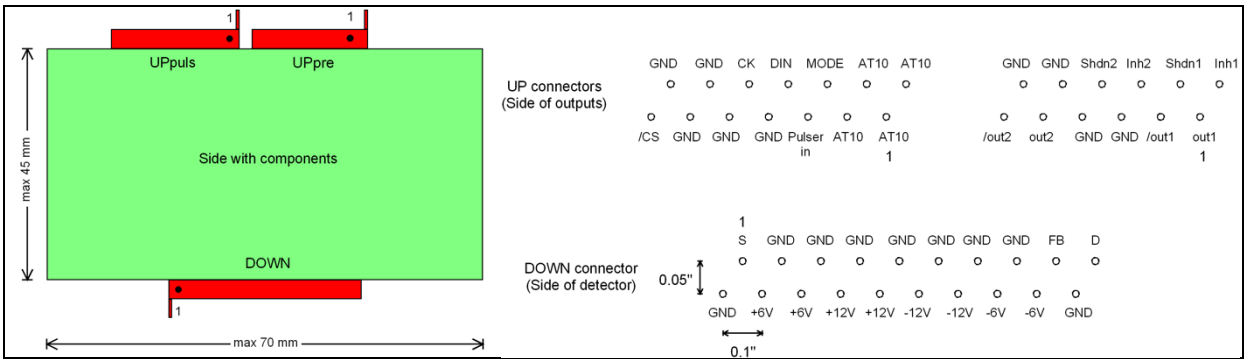

Fig. 15(b)

A complete list and description of the symbols shown in Fig. 15 is reported at the end of this document. In Fig. 16 photographs of prototypes of single/dual core preamplifiers are shown (courtesy of G. Pascovici, IKP Koeln).

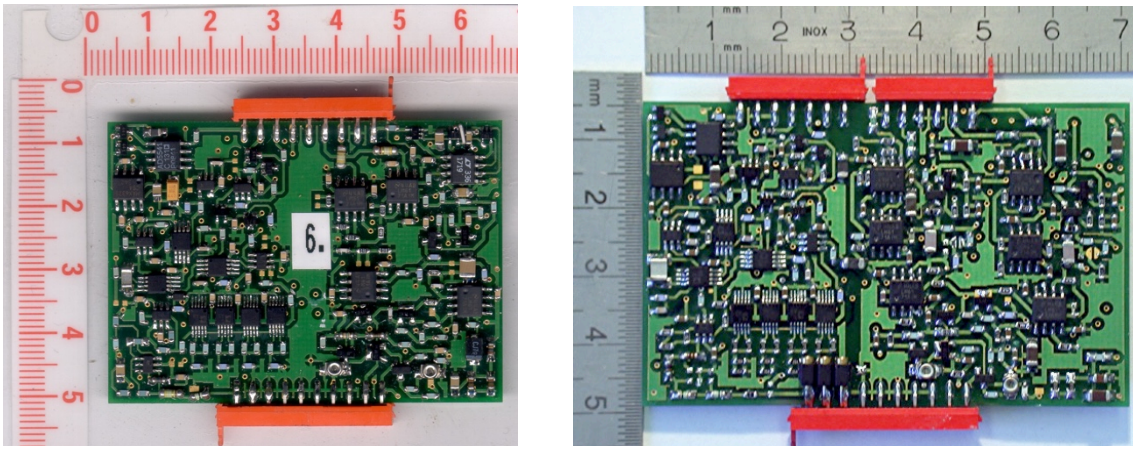

Fig. 16. Photographs of single and dual core preamplifiers (front view) as developed at IKP. The P/Z trimmer is mounted on the back and not visible in this picture.

Preamp Side	12pol Micro Match	14 pol Micro Match	Signal	Cable Name	Digitiser Name
1,14,13,26	5,7,	9,11,12,14	GND	Shield	1,14,13,26
2	3	-	/Out C1	pair 1-	25
15	1	-	Out C1	pair 1+	12
3	-	2	AT10_2	pair 2-	24
16	-	1	AT10_1	pair 2+	11
4	-	4	AT10_4	pair 3-	23
17	-	3	AT10_3	pair 3+	10
5	-	6	MODE	pair 4-	22
18	-	10	CLK	pair 4+	9
6			GND	pair 5-	21
19	-	8	DIN	pair 5+	8
7			GND	pair 6-	20
20	-	13	/CS	Pair 6+	7
8	8	-	SHDN_C2	pair 7-	19
21	4	-	SHDN_C1	pair 7+	6
9		7	/Pulser In	pair 8-	18
22	-	5	Pulser In	pair 8+	5
10	12		/Inh_C2	pair 9-	17
23	10	-	Inh_C2	pair 9+	4
11	6		/Inh_C1	pair 10-	16
24	2	-	Inh_C1	pair 10+	3
12	11	-	/Out_C2	pair 11-	15
25	9	-	Out_C2	pair 11+	2

Specifications

In Table 3 the specifications of the preamplifiers are shown.

Table 3

Property	**value**	**tolerance**
Conversion gain for segments and single core	100 mV / MeV (terminated)*	±10 mV
Conversion gain for dual core	200 mV/MeV (Core Ch. 1) 50 mV/MeV (Core Ch. 2)	±20 mV ±5 mV
Noise	0.8 kev fwhm (0 pF, room T)	
Noise slope	8 eV / pF	±2 eV
Rise time	13 ns (0 pF)	±2 ns
Rise-time slope	~0.4 ns / pF	
Decay time	50 µs	±2 µs
Integral non linearity	< 0.025% (D=3.5V unterminated)	
Output polarity	Differential, Z=100Ω	
Fast reset speed	~10 MeV / µs	
Inhibit output	Single Core: CMOS / Dual Core: LVDS	
Power supply	±6.5V, ±12.5V	±0.5V
Power consumption of input jFET	< 20 mW	
Power consumption (except diff. buffer)	< 280 mW (840 mW for a triple)	
Supplimentary power for differential buffer in very high 'non saturated' counting rates	~700 mW	
Mechanical dimension	~ 70mm x 50 mm x 7 mm (for triple segments and for dual core) ~ 62mm x 45 mm x 7 mm (single core)	

*see Paragraph 'Future upgrade' for Energy Range spec

In Table 4 the power consumption / power supply for a set of 111 preamplifiers (needed to serve one full triple detector setup) are shown.

Table 4

+12V		-12V		+6V		-6V	
Current [A]	Power [W]	Current [A]	Power [W]	Current [A]	Power [W]	Current [A]	Power [W]
1.3	15.6	0.5	6.0	2.0 4.2 *	12.0 25.2 *	1.0 3.2 *	6.0 19.2 *

* high 'non saturated' counting rates

Cables and interface specifications

The signals coming out of the preamplifiers are read out through 26-via LVDS cables with MDR (Mini Delta Ribbon) male connectors on either side. The cable has a "camera-link" format with 11 individually shielded twisted pairs (Pairs 1, 2, ..., 11) and 4 spare pins connected to the shieldings (pins 1, 13, 14, and 26). The pin assignment is defined in Fig. 17 and Table 5.

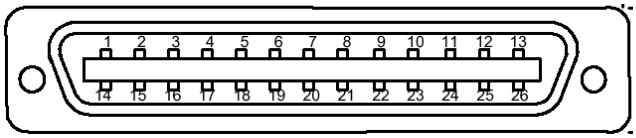

Fig. 17. MDR 26-via male connector

Table 5. Pairs/pins association

Preamp side	*Digitiser side*	*Cable name*	*Preamp side*	*Digitiser side*	*Cable name*	*Preamp side*	*Digitiser side*	*Cable name*	*Preamp side*	*Digitiser side*	*Cable name*
1	1	shield	17	10	pair 3+	8	19	pair 7-	24	3	pair 10+
14	14	shield	5	22	pair 4-	21	6	pair 7+	12	15	pair 11-
2	25	pair 1-	18	9	pair 4+	9	18	pair 8-	25	2	pair 11+
15	12	pair 1+	6	21	pair 5-	22	5	pair 8+	13	13	shield
3	24	pair 2-	19	8	pair 5+	10	17	pair 9-	26	26	shield
16	11	pair 2+	7	20	pair 6-	23	4	pair 9+			
4	23	pair 3-	20	7	pair 6+	11	16	pair 10-			

MicroMatch – MDR Cable Interface

To connect the MicroMatch connectors placed in the upper part of the preamplifier boards with the MDR connectors mounted on the cryostat housing the *ad hoc* motherboards as shown in Figs. 18(a)(b)(c) have been developed for each preamplifier type. A PTFE flat cable is used for flexible interconnection between motherboards and MDR connectors, as seen in Figs. 19(a)(b)(c)(d).

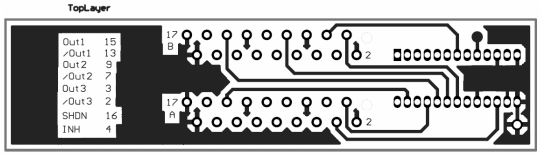

Fig. 18(a) AGATA Triple Segment "Floating" Mainboard

Fig. 18. (b) AGATA Single Core "Floating" Mainboard. (c) AGATA Dual Core "Floating" Mainboard

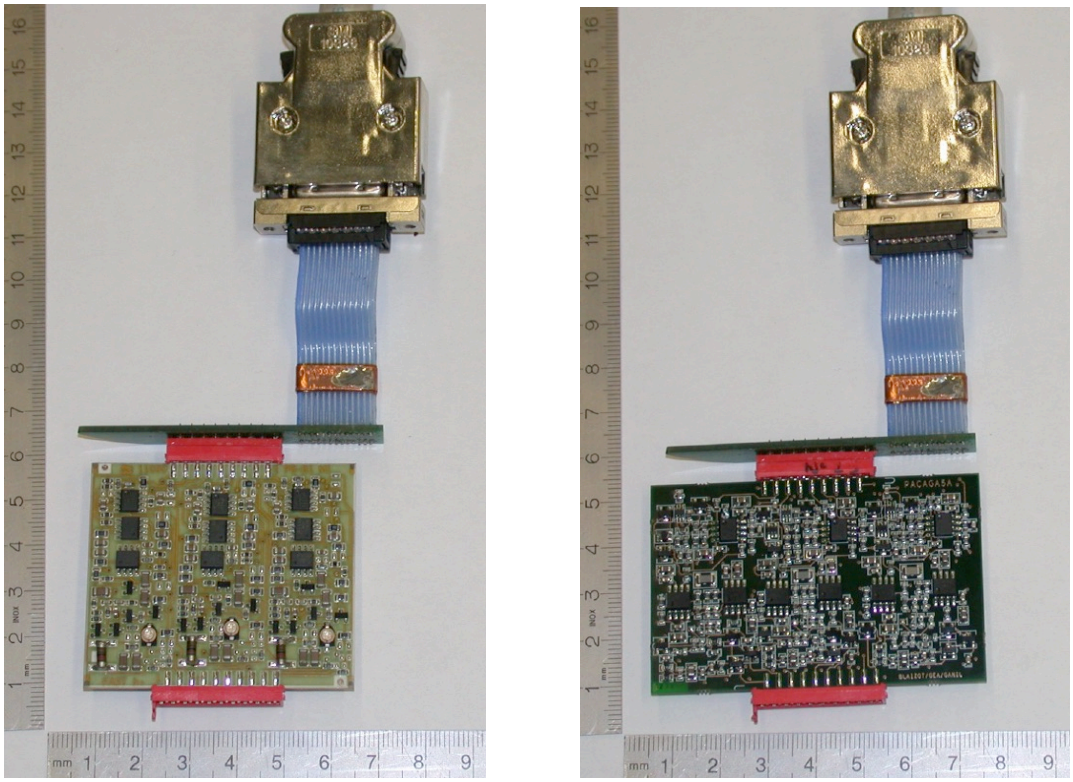

Fig. 19(a) and 19(b): Milano and Ganil Triple Segment Preamplifiers with wiring interface to MDR cable assembly.

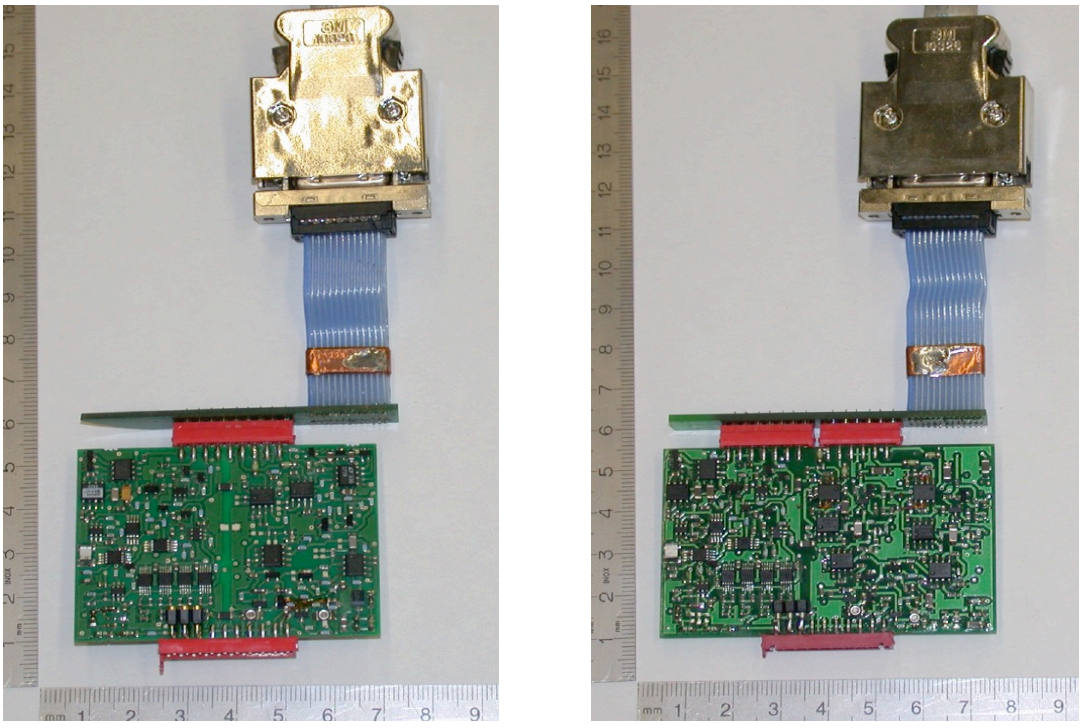

Fig. 19(c) Single Core and and (d) Dual Core Preamplifiers with wiring interfaces to MDR cable assembly

Complete Signal List

Type	*Name*	*Source*	*Type / Format*	*Quantity*
Analog	Segment	Preamp	Analog signal / 1 differential pair	36
	Single Core	Preamp	Analog signal / 1 differential pair	1
	Dual Core	Preamp	Analog signal / 2 differential pairs	2
Digital	Inh_A	Preamp	Digital Signal / +5.x V = High, GND = Low	6
	Inh_B	Preamp	Digital Signal / +5.x V = High, GND = Low	6
	Inh_C	Preamp	Digital Signal / +5.x V = High, GND = Low	1
	SHDN_A	Digitiser	Logic Level / +5.x V = High, GND = Low	6
	SHDN_B	Digitiser	Logic Level / +5.x V = High, GND = Low	6
	SHDN_C	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	AT10_1	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	AT10_2	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	AT10_3	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	AT10_4	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	EN_PS	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	MODE	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	Clk	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	DIN	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	/CS	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	Pulser In	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	Reserved	Preamp	For future expansion	8
	GND	Preamp	GND & Cable shields	28

Note: all Digital Signals and Logic Levels across the interface will be isolated at the Digitizer using the Analog Devices part ADuM1100.

There are six identical connections for the segments, and one for the core.
One cable serves 6 segment preamplifiers (or 2 triple preamplifiers: e.g. preampA tied to segments 1 2 3, and preampB tied to segments 4 5 6). So, 6 such cables are needed to read out all 36 segments of a germanium crystal.
One more cable serves the core preamplifier, and the test pulse generator.

The signals in a Segment Cable

Type	*Name*	*Source*	*Type / Format*	*Q.ty*	*Position*
Analog	Segment	Preamp	Analog signal / 1 differential pair	6	Pairs 1 to 6*
Digital	SHDN_A	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 7+
	SHDN_B	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 7-
	Reserved	-	For future expansion	1	Pair 9
	Inh_A	Preamp	Digital signal / +5.x V = High, GND = Low	1	Pair 10**
	Inh_B	Preamp	Digital Signal / +5.x V = High, GND = Low	1	Pair 11***
Future	Reserved	Preamp	For future expansion	1	Pair 8+
	GND	Preamp	Ground	1	Pair 8-
	GND	Preamp	GND & Cable shields	4	pins 1,13,14,26

*Pair i+ is positive swing, pair i- is negative swing, with i=1, 2,...,6
**Pair 10- swings dynamically, pair 10+ is tied to common ground, i.e. to pins 1,13,14,26
***Pair 11+ swings dynamically, pair 11- is tied to common ground, i.e. to pins 1,13,14,26

The signals in the Single Core Cable

Type	*Name*	*Source*	*Type / Format*	*Q.ty*	*Position*
Analog	Core	Preamp	Analog signal / 1 differential pair	1	Pair 1*
Digital	AT10_1	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 2+
	AT10_2	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 2-
	AT10_3	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 3+
	AT10_4	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 3-
	Clk	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 4+
	MODE	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 4-
	DIN	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 5**
	/CS	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 6**
	SHDN_C	Digitiser	Logic Level /+5.x V= High, GND = Low	1	Pair 7+
	EN_PS	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 7-
	Pulser In	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 8**
Future	Reserved	-	For future expansion	1	Pair 9**
	Inh_C	Preamp	Digital Signal / +5.x V = High, GND = Low	1	Pair 10**
Future	Reserved	Preamp	For future expansion	1	Pair 11***
GND	GND	Preamp	Cable shields & Supply for Logic Isolators	4	Pins 1,13,14,26

*Pair 1+ is positive swing, pair 1- is negative swing
**Pair i+ swings dynamically, pair i- is tied to common ground, i.e. to pins 1,13,14,26
*** for computer-controlled P/Z adjustments, see paragraph 'Future Upgrade'

The signals in the Dual Core Cable

Type	*Name*	*Source*	*Type / Format*	*Q.ty*	*Position*
Analog	Core1	Preamp	Analog signal / 1 differential pair	1	Pair 1*
Analog	Core2	Preamp	Analog signal / 1 differential pair	1	Pair 11**
Digital	AT10_1	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 2+
	AT10_2	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 2-
	AT10_3	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 3+
	AT10_4	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 3-
	Clk	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 4+
	MODE	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 4-
	DIN	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 5***
	/CS	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 6***
	SHDN_C1	Digitiser	Logic Level /+5.x V= High, GND = Low	1	Pair 7+
	SHDN_C2	Digitiser	Logic Level /+5.x V= High, GND = Low	1	Pair 7-
	Pulser In	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 8****
	Inh_C1	Preamp	Digital Signal / +5.x V = High, GND = Low	1	Pair 10****
	Inh_C2	Preamp	Digital Signal / +5.x V = High, GND = Low	1	Pair 9****
GND	GND	Preamp	Cable shields & Supply for Logic Isolators	4	Pins 1,13,14,26

*Pair 1+ is positive swing, pair 1- is negative swing
**Pair 11+ is positive swing, pair 11- is negative swing
***Pair $i_{(+)}$ swings dynamically as LVCMOS signals and pairs $i_{(-)}$ are tied to common ground, i.e. to pins 1,13,14,24
****Pairs $i_{+)}$ and $i_{(-)}$ swing dynamically as LVDS signals

Signal Descriptions

Segment
Differential Analog signal pair. -2.5 V to +2.5 V.

Core
Differential Analog signal pair. -2.5 V to +2.5 V.

Inh_A, Inh_B (Segments) and Inh_C (Single Core)
Active High (set dynamically by preamplifiers A,B and C(single core))
This is a digital signal (CMOS) that will be pulled up if any of the preamplifiers in triples A and B is undergoing a fast reset. It will be pulled down as soon as the fast reset is over. This can be used to inhibit acquisition of false events due to a reset transient. A source termination on the preamp side will be used. Please put no termination resistor on the receiver side to avoid half splitting of the TTL signal. The analog levels for Inhibit_ABC (single core) are detector GND (low) and +5.x V (high). So please use such Power Supply voltages on the isolator on the cable side.
The width of this signal can be used to estimate the amplitude of the energetic event that caused the saturation. Hence this signal should be tied to a precise counter (with the highest possible clock frequency).

Inh_C1 and Inh_C2 (Dual Core)
This are LVDS digital differential signals (ANSI/TIA/EIA-644-A Standard) generating about ~350 mV across the receiver inputs (Z_o ~ 100 Ohm differential input media). Please terminate these lines with 100 Ohm on the receiver side.

SHDN_A, SHDN_B (Segments) and SHDN_C (Single Core and Dual Core)
Active High Logic Level.
Switches off fast reset mechanism in triple preamplifiers A and B.
If this is pulled up the fast reset mechanism will be permanently switched off. If this is pulled down the fast reset mechanism will automatically work in each of the six preamplifiers when needed.
The analog levels for SHDN_ABC are detector GND (low) and +5.x V (high). So please use such Power Supply voltages on the isolator on the cable side.

AT10_1, AT10_2, AT10_3, and AT10_4
Active High Logic Level.
Attenuates pulser amplitude by 10dB.
The analog levels for AT10 are detector GND (low) and +5.x V (high) . So please use such Power Supply voltages on the isolator on the cable side.

EN_PS
Not used in current version of the Single Core.

MODE
Logic Level.
Selects the shape of built-in Pulser. If this is pulled up the built-in pulser provides a positive exponential decay. If this is pulled down the built-in pulser provides a square wave.

Clk, DIN, /CS

Digital Signals (Clock, Data In, Chip Select) used to set the pulser fine gain.
These signals implement a simple, low-frequency, 3-wire interface through which the 16-bit input of DAC AD5541 from Analog Devices is supplied, which sets the fine gain of the pulser. The maximum clock frequency is 25MHz but it is advisable to use a substantially lower frequency (e.g. 1 MHz). The protocol of this interface can be found on the data sheet of AD5542. It is advisable to use only large numeric values (in the range from 50 to 100% of the full scale) for fine-gain corrections. Otherwise the long-term stability of the pulser could worsen significantly. Use instead AT10 and/or AT20 for coarse-gain setting. The analog levels for Clk, DIN, /CS are detector GND (low) and +5.x V (high). So please use such Power Supply voltages on the isolator on the cable side.

Pulser In

Active Low and High Digital Signal.
This is a digital signal (LVCMOS in Single Core and LVDS in Dual Core). The trigger threshold is set to V_{os} = 1.25V. Its negative edge will generate a positive transition of the pulser output signal and its positive edge will generate a negative transition of the pulser output signal. (In **Differential Mode**, the negative output signal is attenuated with ~30dB)

IMPORTANT NOTES:

1) All detector GND's carried to the receiver along the cable must be connected at the receiver end to the cable shields found on pins 1, 13, 14 and 26 of the MDR connector.
2) All digital signals transmitted from the receiver to the detector should enter the cable through a source series termination resistor of 75 Ohms. Instead, no termination resistor should be put at the detector side to avoid half splitting of the TTL signal.
3) All Logic Levels (see column "Format" in Complete Signal List) should be bypassed to ground with 1uF capacitors either at the transmitter or at the receiver sides.

FUTURE UPGRADE

(*i) LVDS transmission for Pulser_In, INH_C1 and INH_C2 (opt) ⇔ correspondingly, their former return GND lines will be turned into LVDS active lines!*

Grounding and interconnection of preamplifiers

The AGATA Charge Sensitive Preamplifiers are mounted in a triple cryostat, holding three segmented, encapsulated HP_Ge detectors [1]. In order to improve the S/N ratio the detectors as well the cold parts of the preamplifiers are cooled with liquid nitrogen at a desired temperature. As shown in Fig.20, the cold parts of the charge sensitive preamplifiers are connected to the interior ground of the triple cryostat while the warm part to its exterior ground. To ensure a very solid ground for all preamplifiers a special main board was very carefully designed (for one detector is showing in Fig. 21). Unfortunately, one can very hardly get a sufficiently solid connection between the two grounds points, due to its prohibitive thermal shunt.

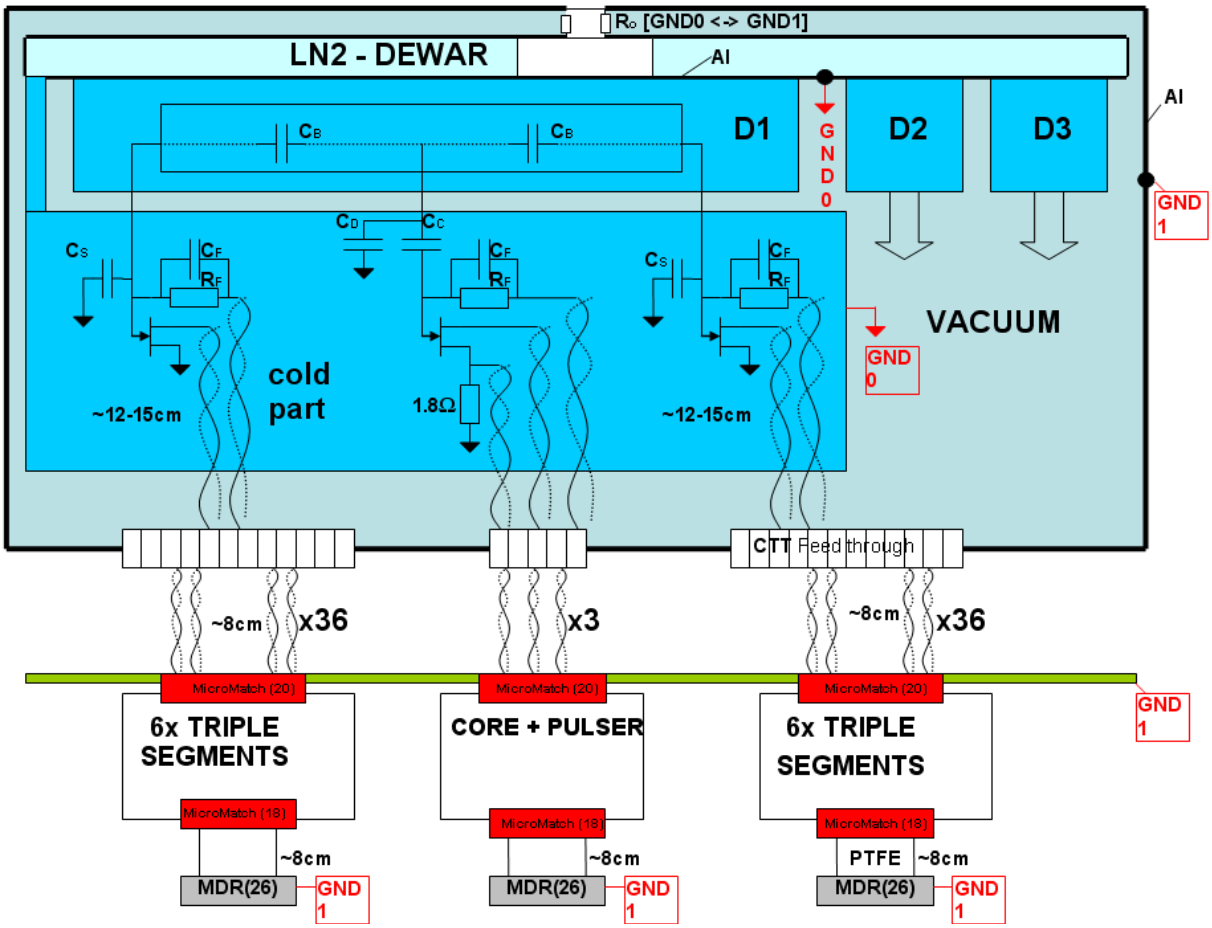

Fig. 20. Scheme of principal electrical connections in a triple cryostat-preamplifier assembly. D1, D2 and D3 are the three 36-folded segmented/encapsulated detectors.

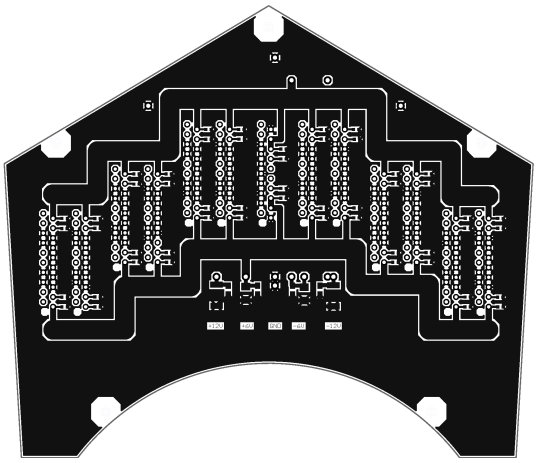

Fig. 21. Layout of the motherboard where (36+1) preamplifiers are plugged in (top view).

Please note that if, at the FADC level, a 14 bit fast ADC with a dynamic range of +/- 1 V is used then the ADC channel width is about 60 µV, therefore the signal routing and the grounding of mixed signal at this level is a very delicate and important issue [2].

[1] D. Weisshaar et al AGATA 3-WAY CRYOSTAT for 36-fold segmented, encapsulated HPGe-detectors, white paper, Jan. 2004
[2] G. Pascovici AGATA GROUNDING , GSI, Feb. 2005
[3] I. Kojouharov, J. Gerl, Integral Detector Support System (IDSS), GSI, Feb. 2005