ADC: mise en oeuvre

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Roscoff, septembre 2018

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1. Choisir un ADC
2. Evaluer un ADC
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   - ✓ la tenue aux radiations
3. Utiliser un ADC
   - ✓ la fluctuation de l'instant d'échantillonnage
   - ✓ la CEM
   - ✓ l'impédance d'entrée des ADC
4. Exemples d'utilisation d'ADC @ IN2P3

1. Choisir un ADC

« La préhistoire »

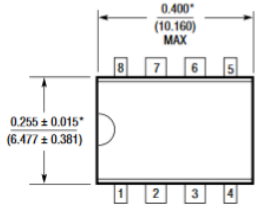
- 1954: Vacuum Tube ADC “DATRAC”:
  - **11-bit**
  - **50-kSPS**
- Designed by Bernard M. Gordon at EPSCO
- 50 x 40 x 60 cm3
- 68 kg
- 500W
- 8500 $

http://www.analog.com/media/en/training-seminars/design-handbooks/Data-Conversion-Handbook/Chapter1.pdf

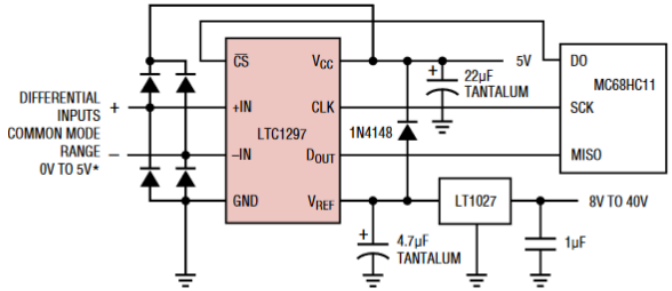
Retour vers le Futur …

1954

1994



12-Bit Differential Input Data Acquisition System



❑ Année	1954	→ 40ans ←	1994
❑ Résolution:	11 bits	--	12 bits
❑ Fréq. d'échantillon.:	50kS/s	--	50kS/s
❑ Taille:	120k cm^3	÷ 600 000	0,2 cm^3
❑ Poids	68 kg	÷ 7 000	10g ?
❑ Puissance	500W	÷ 17 000	30mW
❑ Prix	8500 $	÷ > 8 500	< 1 $

Les principaux fabricants d'ADC

AKM Semiconductor {Audio ADCs/DAC IC Manufacturer}

Analog Devices {Analog-to-Digital Converters/Digital-to-Analog Converter ICs}

Cirrus Logic {Audio A/D and D/A converters, CODEC Manufacturer}

Fairchild Semiconductor {ADCs/DAC IC Manufacturer} → OnSemi en 2015

Holtek Semiconductor Inc. {DAC/ADC ICs}

Intersil {ADCs/DAC IC Manufacturer}

Linear Technology {ADCs/DAC IC Manufacturer}

Maxim Integrated Products {ADCs/DAC IC Manufacturer}

Microchip {Delta-Sigma/Dual Slope/Binary/BCD ADC ICs}

National Semiconductor {ADCs/DAC IC Manufacturer}

NEC {D/A Converter for Audio System}

NJR Corporation {ADC-DAC-V/F-F/V Converter ICs}

Renesas Technology America, Inc {D/A R2R, Multiplying, A/D Converter}

Sony {A/D Converter 1:2 De-Multiplex, TTL Output, Sample & Hold, D/A Converter}

Thaler Corp. {A/D Converter Manufacturer. ADC 18-26 bits}

Texas Instruments 'TI' {ADC-DAC-Voltage/Freq Converter IC Manufacturers}

Wavefront Semiconductor {48kHz 24-bit stereo audio ADC, low-cost 24-bit DAC IC Manufacturer}

Wolfson Microelectronics
{Mono, Multi-channel and Stereo ADCs}

Pas d'évolution depuis 2014 !
Liste à jour ?

2780 références chez Farnell

http://www.interfacebus.com/Analog_DAC.html

Analog Devices: « Number One » ??

- ✓ Analog Devices: 1291 références (604 en 2014)
  - ✓ Precision and General purpose ADCs (<=10MSPS) (786)
  - ✓ High speed ADCs (> 10MSPS) (505)

Precision and General Purpose ADC Finder

Resolution (Bits)	ADC Throughput Rate (SPS)					
	<1K	1 - 100k	100 - 250k	250 - 450k	450k - 1M	1M - 10M
18 - 24	✔ (46)	✔ (37)	✔ (21)	✔ (17)	✔ (29)	✔ (28)
14 - 17	✔ (40)	✔ (24)	✔ (64)	✔ (40)	✔ (63)	✔ (81)
8 - 13	✔ (1)	✔ (54)	✔ (57)	✔ (27)	✔ (67)	✔ (90)

High-Speed ADC Finder

Resolution (Bits)	ADC Throughput Rate (MSPS)			
	10 - 50	50 - 100	100 - 250	250+
>/=16	✔ (26)	✔ (26)	✔ (27)	✔ (3)
14 - 15	✔ (31)	✔ (44)	✔ (66)	✔ (25)
12 - 13	✔ (37)	✔ (43)	✔ (57)	✔ (24)
10 - 11	✔ (15)	✔ (20)	✔ (26)	✔ (3)
</=9	✔ (7)	✔ (9)	✔ (9)	✔ (7)

http://www.analog.com/en/products/analog-to-digital-converters.html

SELECTION TABLE FOR 18 TO 24 BIT, 1 MSPS TO 10 MSPS

Sort by newest | Choose parameters | Quick Filter | Reset Table | Download to Excel | Help | Maximize Filters

Part #	Hardware	Resolution (Bits) (bit)	Throughput Rate (SPS)	# Channels	Full Power BW (Hz)	Vsupply Pos (min) (V)	Max Pos Supply (V) (V)	Power Dissipation (W)	US Price 1000-4999 ($ US)
	0 Values ...	4 Values Selected	1M - 10M	0 Values Selec...	23.4 - 2G	1.22 - 12	1.7 - 16.5	142u - 4.05	0.95 - 833.21
AD7960		18	5 MSPS	1	28 MHz	4.75 V	5.25 V	21 mW	$31.00
AD7986		18	2 MSPS	1	19 MHz	4.75 V	5.25 V	29 mW	$29.95
AD7984		18	1.33 MSPS	1	-	2.375 V	2.625 V	14 mW	$28.29
AD7982		18	1 MSPS	1	10 MHz	2.375 V	2.625 V	8.6 mW	$23.28
AD7643		18	1.25 MSPS	1	50 MHz	2.3 V	3.6 V	80 mW	$19.50
AD7641		18	2 MSPS	1	50 MHz	2.5 V	2.5 V	92 mW	$29.33
AD7760		24	2.5 MSPS	1	1.35 MHz	4.75 V	5.25 V	958 mW	$24.90

Aide au choix et mise en oeuvre

Design Center

Find Analog Devices' design resources here: Reference Designs, Design Tools, Simulation Models, Evaluation Boards, Device Drivers, packaging, etc.

Search within Design Center

Circuit Design Tools & Calculators

Get product selection and design assistance using our online and downloadable tools.

- LTspice
- Amplifier & Linear Tools
- Clock & Timing Tools
- Converter Tools
- Power Management Tools
- RF & Synthesis Tools

Simulation Models

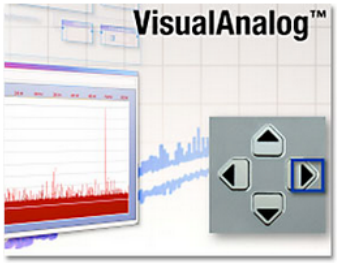
Collection of product simulation models used in industry standard simulation tools.

- SPICE Models
- IBIS Models
- MathWorks Behavioral Models
- BSDL Models
- S-Parameters
- Sys-Parameter Models for Keysight Genesys

Reference Designs

Packaging, Quality, Symbols & Footprints

Visual Analog™

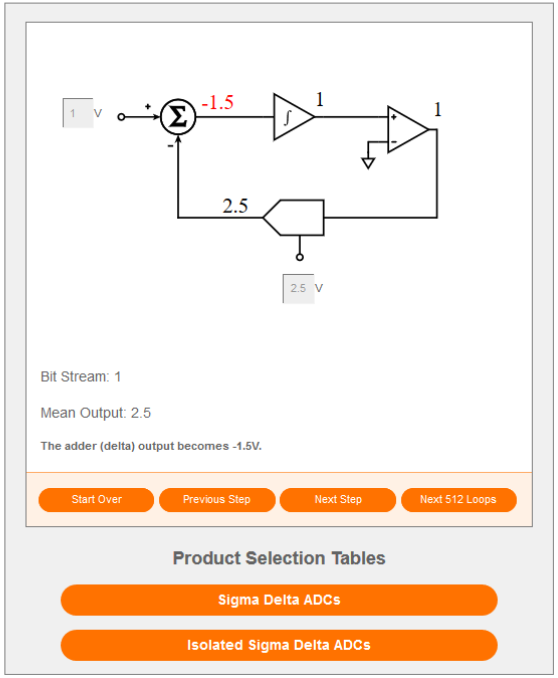


For designers who are selecting or evaluating high speed ADCs, VisualAnalog™ is a software package that combines a powerful set of simulation and data analysis tools with a user-friendly graphical interface. Many designers are familiar with ADCAnalyzer - a tool that models ADC performance with varying input frequencies and sample rates. VisualAnalog takes this concept further by allowing designers to customize their input signal and data analysis. An input signal can be constructed from sine waves, noise sources, and vector data to see how an ADC will perform in real world conditions. The data analysis functions are expanded from the basic FFTs that are available in ADCAnalyzer as well. Customizable calculations allow designers to predict adjacent channel power ratio (ACPR) and display I/Q constellation plots on simulated ADC outputs or data collected from evaluation boards. VisualAnalog™ is also used as a controller for a new data capture board (HSC-ADC-EVALCZ).

Sigma-Delta ADC Tutorial

An interactive illustration showing the behavior of an idealized sigma-delta A/D converter.

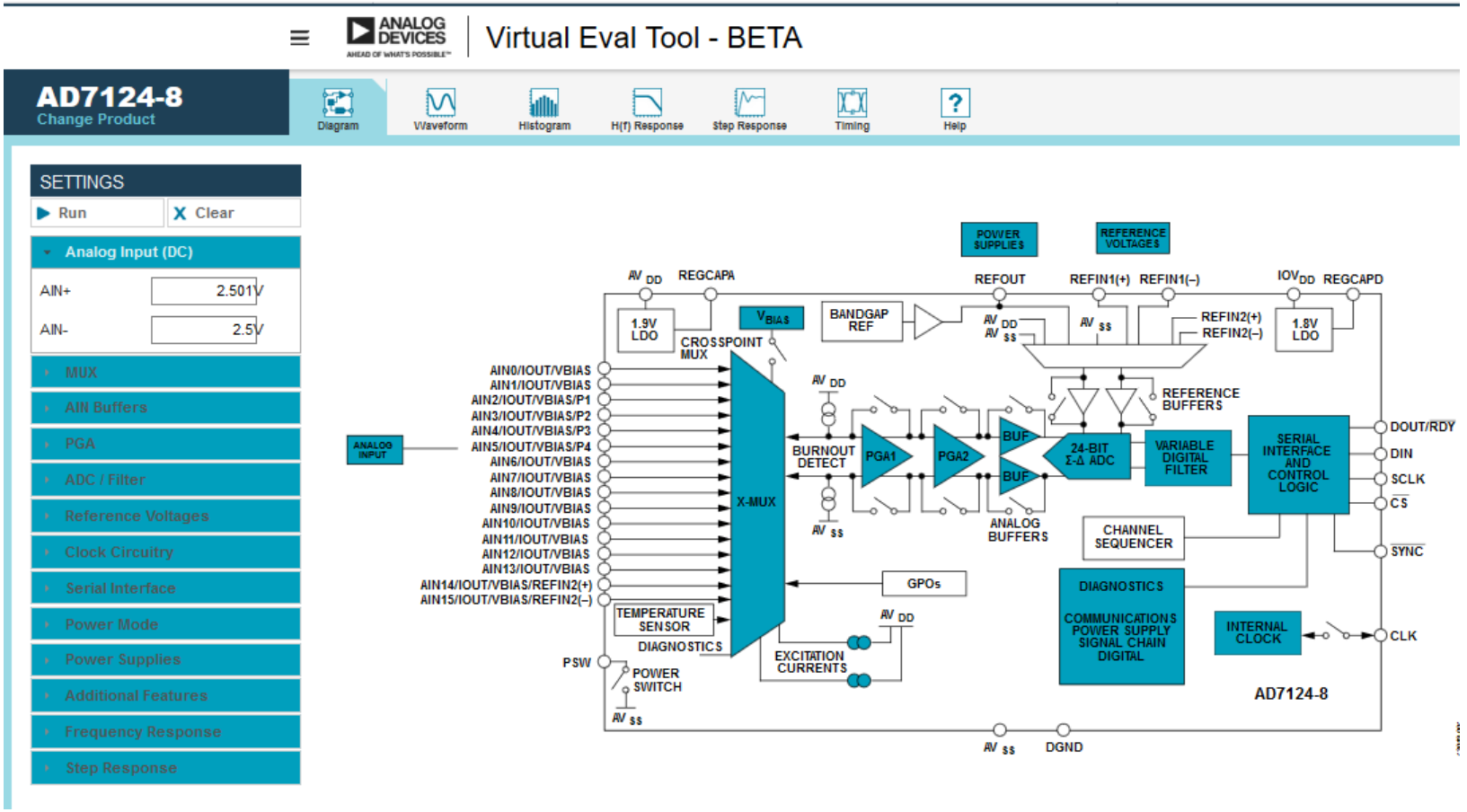
Instructions | Related Information



Aide au choix et mise en oeuvre

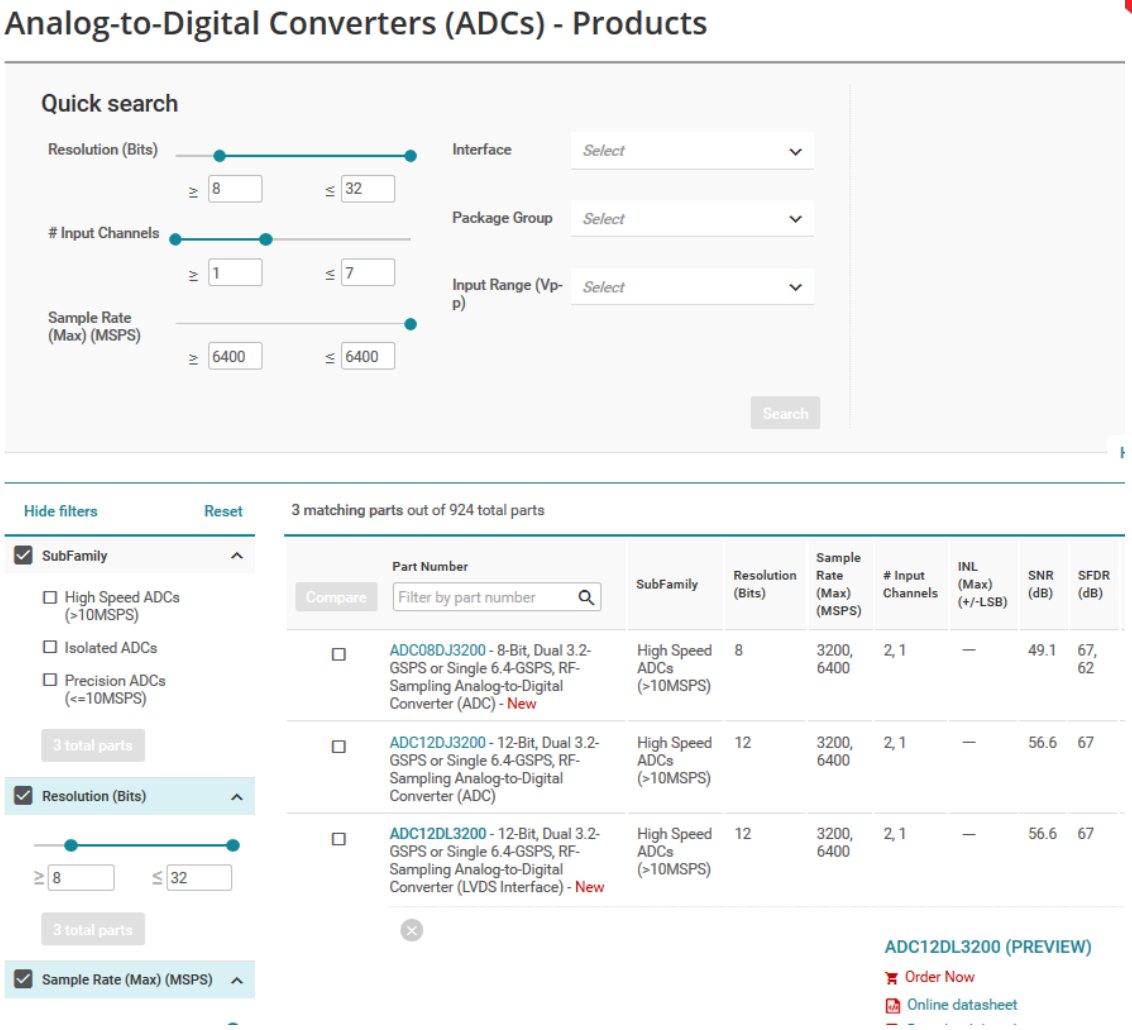
http://beta-tools.analog.com/virtualeval/

Ex ADIsimADC



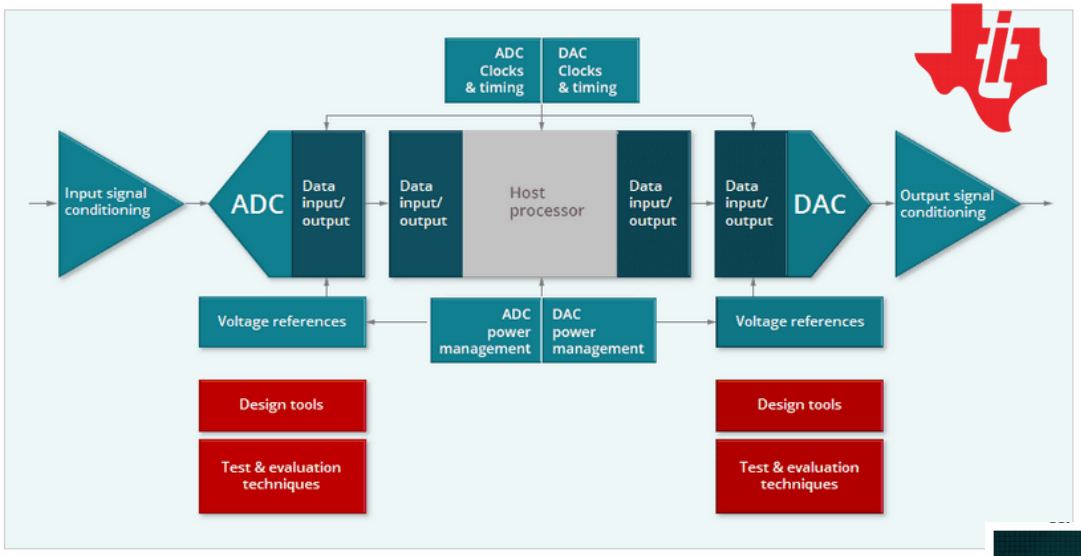
Texas instruments

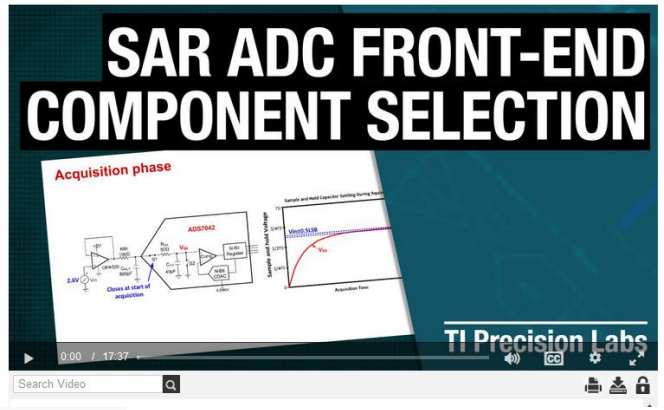
- ✓ 913 références en 2018 (774 en 2014, 380 en 2009)



Aide au choix et mise en œuvre

Data Converters – Learning center





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http://www.ti.com/data-converters/learning-center.html#ADCbasicsapplications

Maxim Integrated

- ✓ Maxim Integrated Products: 578 références (563 en 2014, 433 en 2009)
  - ✓ Display-Oriented ADCs (33)
  - ✓ High-Speed ADCs (> 5Msps) (71) : max 8-bit 7,5GS/s (Max1191 de 2003 !!)
  - ✓ Precision ADCs (≤ 5Msps) (474): 8 à 24 bits (idem 2014)

Peu d'évolution

maxim integrated™

High-Speed ADCs (> 5Msps)

Hide Controls — **Total Parts: 73**

	Input Chan.	Resolution (bits)	Sample Rate (Msps) max ≥	Sample Rate (Msps) max ≤	AC Specs (MHz) @ f_{IN}	SFDR (dBc) min	ENOB (bits) min	SINAD (dB)	SNR (dB)	THD (dB)	DNL (±LSB)	INL (±LSB)	Full Pwr. BW (MHz) min	I_{CC} (mA) typ	Data Bus Interface	Industry Qualified	Package/Pins	Budgetary Price
Current Selections:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Parametric Selection Controls:	☐1 ☐2 ☐4 ☐8	☐6 ☐8 ☐10 ☐12 ☐14 ☐16	2200	2200	1600	93	11.4	77.4	79.2	-44.5	1	3	2800	1375	☐µP/10 ☐µP/12 ☐µP/14 ☐µP/16 ☐µP/8 ☐Demuxed ☐LVDS ☐LVPECL ☐Selectable Dual/Mux'd CMOS ☐Serial ☐Serial LVDS	☐Automotive - AECQ100	☐CTBGA/144 ☐LQFP/48 ☐QFN/68 ☐SBGA/192 ☐SBGA/256 ☐SSOP/28 ☐SSOP/36 ☐TQFN-CU/40 ☐TQFN/28 ☐TQFN/40 ☐TQFN/48 ☐TQFN/56	$50.03 @1k
			7.5	7.5	15	38	5.8	36.4	37	-93	0.1	0	55	23.5				$2.97 @1k
Hidden Columns: 9 (Default)	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide
Compare ☑All ☑None — Sort by: Part Number: ▲▼ Default = Newest First	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼
☑ MAX19527 Octal, 12-Bit, 50Msps, 1.8V ADC With Serial LVDS Outputs	8	12	50	50	19.3	84	11	68.2	68.5	-81	0.3	0.5	500	158	Serial LVDS	-	CTBGA/144	$45.07 @1k
☑ MAX19515 Dual-Channel, 10-Bit, 65Msps ADC	2	10	65	65	70	77	-	59.6	60.1	-79	0.2	0.25	850	47	Selectable Dual/Mux'd CMOS	Automotive - AECQ100	TQFN/48	$7.52 @1k
☑ MAX19516 Dual-Channel, 10-Bit, 100Msps ADC	2	10	100	100	70	83	-	59.5	60	-79	0.2	0.25	850	63	Selectable Dual/Mux'd CMOS	-	TQFN/48	$11.28 @1k
☑ MAX19517 Dual-Channel, 10-Bit, 130Msps ADC	2	10	130	130	70	82	-	59.4	59.8	-78	0.2	0.25	850	82	Selectable Dual/Mux'd CMOS	-	TQFN/48	$16.90 @1k
☑ MAX1437B Octal, 12-Bit, 50Msps, 1.8V ADC With Serial LVDS Outputs	8	12	50	50	20	93	11.4	69.7	70.1	-93	0.25	0.3	100	348	Serial LVDS	-	TQFN/68	-
☑ MAX19507 Dual-Channel, 8-Bit, 130Msps ADC	2	8	130	130	70	77	-	49.3	49.8	-72	0.1	0.1	850	82	Selectable Dual/Mux'd CMOS	-	TQFN/48	$9.27 @1k
☑ MAX19506 Dual-Channel, 8-Bit, 100Msps ADC	2	8	100	100	70	77	-	49.3	49.8	-72	0.1	0.1	850	63	Selectable Dual/Mux'd CMOS	-	TQFN/48	$6.16 @1k
☑ MAX19505 Dual-Channel, 8-Bit, 65Msps ADC	2	8	65	65	70	77	-	49.3	49.8	-72	0.1	0	850	85	Selectable Dual/Mux'd CMOS	-	TQFN/48	$4.11 @1k
☑ MAX109 8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs	1	8	2200	2200	1600	50.3	-	42.1	44	-46.6	0.25	0.25	2800	1375	µP/8 Demuxed LVDS	-	SBGA/256	-
☑ MAX1213N 1.8V, 12-Bit, 170Msps ADC for Broadband Applications	1	12	170	170	100	87	-	67.1	67.2	-	0.3	0.55	700	400	µP/12 LVDS	-	QFN/68	-

Autres fabricants d'ADC

- **Audio** (≤ 200kS/s, ≥ 16bits):
  - ✓ AKM Semiconductor
  - ✓ Cirrus Logic
  - ✓ Holtek Semiconductor Inc. {16 voies avec µ-processeur et interface SPI ou USB}
  - ✓ NEC
  - ✓ Wavefront Semiconductor {48kHz 24-bit stéréo audio ADC}
  - ✓ Wolfson Microelectronics {ADCs/DAC IC Manufacturer}

- **Vidéo** (≥ 30MS/s, 8bits):
  - ✓ Intronics Inc.

Données de 2014 !!

- **Affichage**
  - ✓ Intronics Inc. (LCD/LED Display)
  - ✓ NJR. (LCD Display)
  - ✓ Sony {ADC 1:2 De-Multiplex, TTL Output, SampleHold, D/A Converter} → obsolète
- **Rad Hard**
  - ✓ e2v{10 bits – 2.2 GHz}
  - ✓ ST micro. (12/14 bits – 50/20 MS/s)
- **Autre**
  - ✓ Thaler Corp. {ADC à rampe 18-26 bits très lent }
  - ✓ Intronics Inc. (Flash, Pipeline, ΔΣ, SAR)
  - ✓ Intersil {ADCs/DAC IC Manufacturer}
  - ✓ Linear Technology
    - ✓ Pipeline 16bits-160MS/s-1,45W
    - ✓ 16bits ΔΣ avec interface I2C
  - ✓ Microchip {ΔΣ, SAR, Dual Slope/Binary/BCD ADC} pas grand choix

Innovations @ ANALOG DEVICES

CIRCUITS MIXTES

Les CAN et CNA d'Analog Devices parés pour la 5G et la radio logicielle

L'américain introduit simultanément un double CAN de 14 bits à 3 Géch./s et un double CNA de 16 bits à 12 Géch./s. Avec notamment en ligne de mire les stations de base 4G/5G et les radios définies par voie logicielle.

Le convertisseur A/N AD9208

Analog Devices, l'indéboulonnable numéro un mondial des circuits de conversion de données, renouvelle sa gamme, déjà bien étoffée, de convertisseurs A/N et N/A rapides. Avec notamment en ligne de mire les stations de base 4G/5G multibandes et les systèmes de radio logicielle (SDR, Software-defined radio).

D'un côté, l'AD9208 est un convertisseur A/N d'architecture pipelinée différentielle, à cadence d'échantillonnage de 12 Géch./s, l'AD9172 est susceptible de synthétiser un signal dont la fréquence est de 6 GHz. Une valeur suffisamment élevée pour permettre, dans les chaînes d'émission, de faire l'impasse sur un étage de conversion de fréquence FI vers RF.

Sur la puce trouvent place des éléments tels que des NCO 48 bits, des filtres interpolateurs, une interface JESD204B (sous-classe 1) à 15 Gbit/s... La consommation totale du circuit est de 2,55 W à 12 Géch./s. L'AD9172 est proposé dans un boîtier BGA de 144 billes, dont les dimensions sont de 10 x 10 mm. Par quantité de 1000 pièces, son prix unitaire est de 240$. Parmi les marchés ciblés figurent les infrastructures de communication sans fil, les applications militaires (radars, brouilleurs), l'instrumentation et les équipements de test automatisé.

PHILIPPE CORVISIER

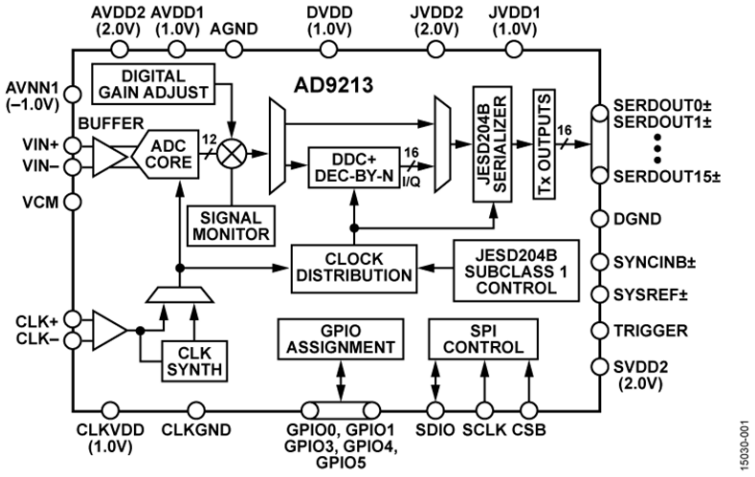
Magasine ElectroniqueS n°82, mai 2017

High Speed Converter Innovations on 28 nm CMOS

Introducing the first of a new line of RF converters designed for GHz bandwidth applications such as 4G/5G multiband wireless communications base stations, multi-standard production test systems, and defense electronics. Based on 28 nm CMOS technology, these ADCs and DACs provide best-in-class bandwidth, power and dynamic range to cover the largest number of signal bands.

View high speed converter chip designs

AD9213: 12-Bit, 10.25 GSPS, RF Analog-to-Digital Converter



- High instantaneous dynamic range
  - Noise spectral density 154dBFS/Hz
  - SFDR 68dBc (1GHz, −1dBFS)
- Low power consumption: 5.1W at 10Gsps
- Integrated Input Buffer (6.5GHz input bandwidth)
  - 1.4V p-p full-scale input with RIN=50 Ω
  - Overvoltage protection
- 16-lane JESD204B output (up to 16 Gbps line rate)
- Multichip sync capable with 1 sample accuracy
  - DDC NCO synchronization included
- Fast overrange detection for efficient AGC
- Integrated DDC
  - Selectable decimation factors
  - 16-profile settings for fast frequency hopping
- Optional on-chip PLL clock multiplier
- On-chip temperature sensor
- On-chip negative voltage generators
- Low CER <1e−16
- 12 mm × 12 mm BGA
- **240$ par 1000 pièces (AD9172)**

http://www.analog.com/en/products/analog-to-digital-converters/standard-adc/high-speed-ad-10msps/AD9213.html#product-overview

2. Evaluer un ADC:

⇨ les principes de mesure

Document de référence

IEEE Std 1241-2000

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

Contents

Source: Norme IEEE [IEEE]

Critical ADC parameters

Typical applications	Critical ADC parameters	Performance issues
Audio	SINAD, THD	Power consumption. Crosstalk and gain matching.
Automatic control	Monotonicity Short-term settling, long-term stability	Transfer function. Crosstalk and gain matching. Temperature stability.
Digital oscilloscope/waveform recorder	SINAD, ENOB Bandwidth Out-of-range recovery Word error rate	SINAD for wide bandwidth amplitude resolution. Low thermal noise for repeatability. Bit error rate.
Geophysical	THD, SINAD, long-term stability	Millihertz response.
Image processing	DNL, INL, SINAD, ENOB Out-of-range recovery Full-scale step response	DNL for sharp-edge detection. High-resolution at switching rate. Recovery for blooming.
Radar and sonar	SINAD, IMD, ENOB SFDR Out-of-range recovery	SINAD and IMD for clutter cancellation and Doppler processing.
Spectrum analysis	SINAD, ENOB SFDR	SINAD and SFDR for high linear dynamic range measurements.
Spread spectrum communication	SINAD, IMD, ENOB SFDR, NPR Noise-to-distortion ratio	IMD for quantization of small signals in a strong interference environment. SFDR for spatial filtering. NPR for interchannel crosstalk.
Telecommunication personal communications	SINAD, NPR, SFDR, IMD Bit error rate Word error rate	Wide input bandwidth channel bank. Interchannel crosstalk. Compression. Power consumption.
Video	DNL, SINAD, SFDR, DG, DP	Differential gain and phase errors. Frequency response.
Wideband digital receivers SIGINT, ELINT, COMINT	SFDR, IMD SINAD	Linear dynamic range for detection of low-level signals in a strong interference environment. Sampling frequency.

COMINT = communications intelligence
DNL = differential nonlinearity
ENOB = effective number of bits
ELINT = electronic intelligence
NPR = noise power ratio
INL = integral nonlinearity
DG = differential gain error

SIGINT = signal intelligence
SINAD = signal-to-noise and distortion ratio
THD = total harmonic distortion
IMD = intermodulation distortion
SFDR = spurious free dynamic range
DP = differential phase error

Source: Norme IEEE [IEEE]

Banc de test statique

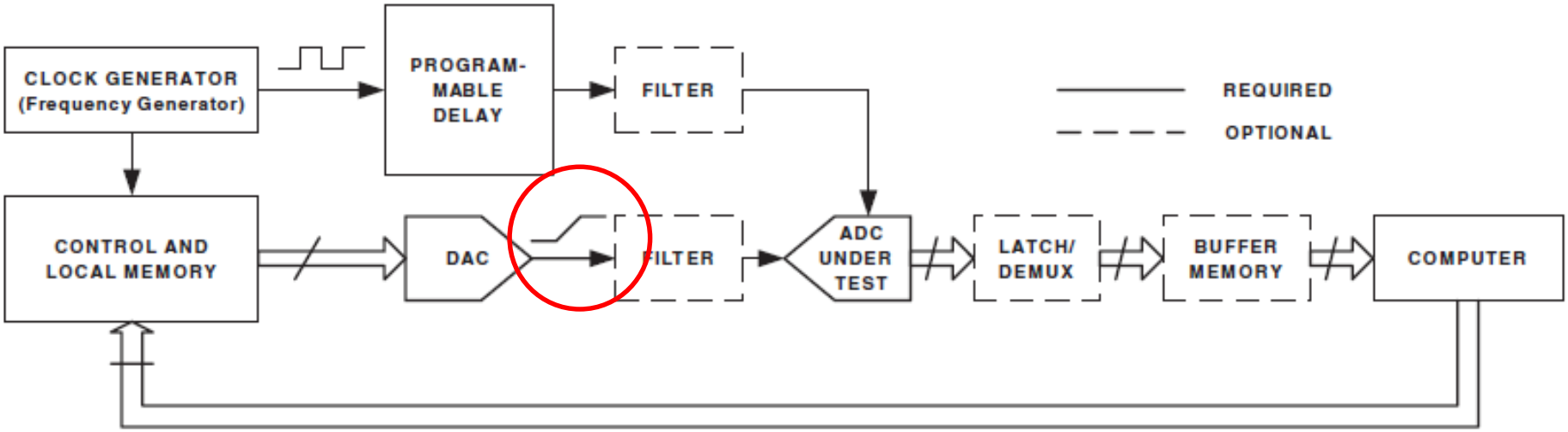


Figure 4—Setup for arbitrary signal testing

Variation lente du signal d'entrée par rapport à la fréquence d'horloge.

Filtrage basse fréquence du signal injecté préconisé.

Filtrage de l'horloge pour réduire le jitter préconisé.

Source: Norme IEEE [IEEE]

Test avec un signal Rampe

- Temps de montée de la rampe >> période de l'horloge
- Δv entre chaque cout d'horloge de l'ADC << au pas de quantification (pour déterminer la DNL)

Ex: ADC 12bits @ 40MHz sur 1V → Δv en 25ns << 250µV
Avec Δv=100µV, durée de la rampe: 25ns * 1V/100µV = 250µs

- Si possible, faire *n* mesures sur chaque palier pour réduire le bruit de $\sqrt{n}$.

4.1.6.2.1 Comments on number of samples to be averaged per transition level for a given confidence level

The precision of the measured values of the code transition levels depends on the total number of histogram samples measured. Increasing the number of samples decreases the uncertainty while ramping the input. The larger the total, the lower the uncertainty. Nonlinearity of the ramp input signal would produce errors in the code transition levels. Noise on the ramp signal or the ADC under test will cause uncertainty in the measured code transition levels. Specifically, the uncertainty in LSBs due to noise in the estimate of a transition level is approximated by Equation (61).

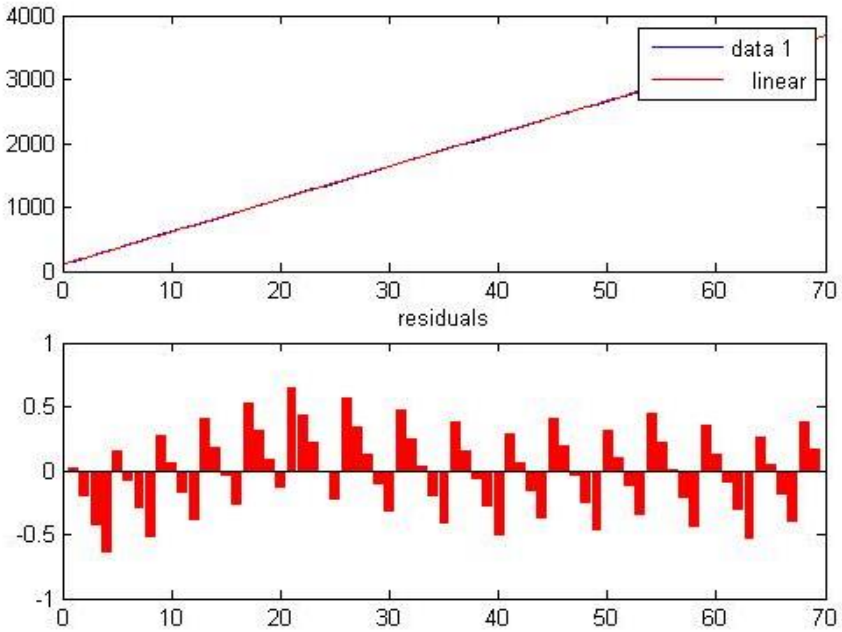
$$\varepsilon \approx \sqrt{\frac{\sigma}{H}} \qquad (61)$$

where

σ is the standard deviation of the noise, in units of ideal code bin widths (LSBs),

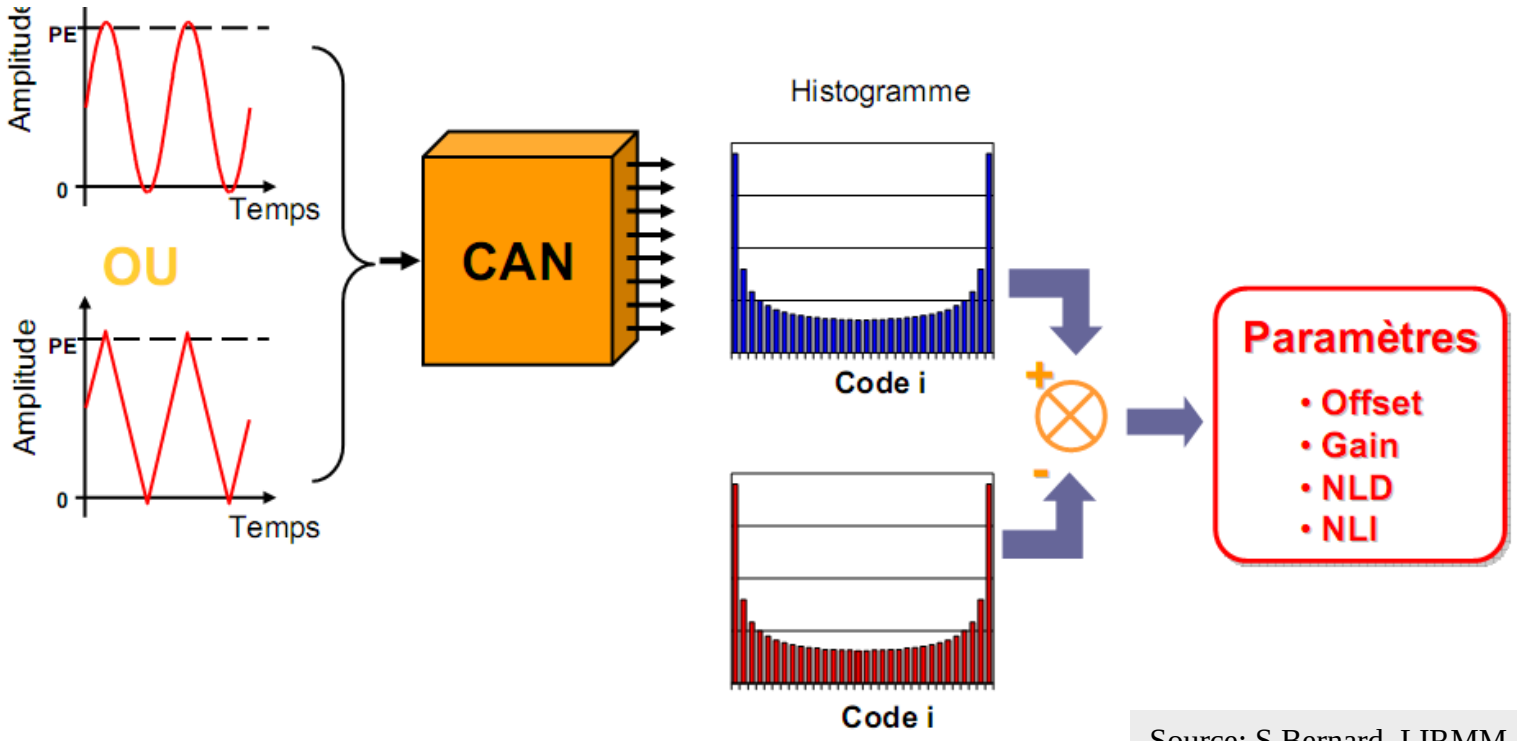
H is the average number of histogram samples received in each of the code bins that share the given transition level.

Source: Norme IEEE [IEEE]



Test par histogramme

- **Principe :**
  - ✓ Signal d'entrée sinusoïdal ou linéaire (triangle, rampe)
  - ✓ Construire l'histogramme expérimental = Fréquence d'apparition des codes de sortie
  - ✓ Comparer cet histogramme avec l'histogramme idéal



Source: S.Bernard, LIRMM [BER]

Test par histogramme

- **Principe :**
  - ✓ Signal d'entrée sinusoïdal ou linéaire (triangle, rampe)
  - ✓ Construire l'histogramme expérimental = Fréquence d'apparition des codes de sortie
  - ✓ Comparer cet histogramme avec l'histogramme idéal

☹ Nombre d'échantillons

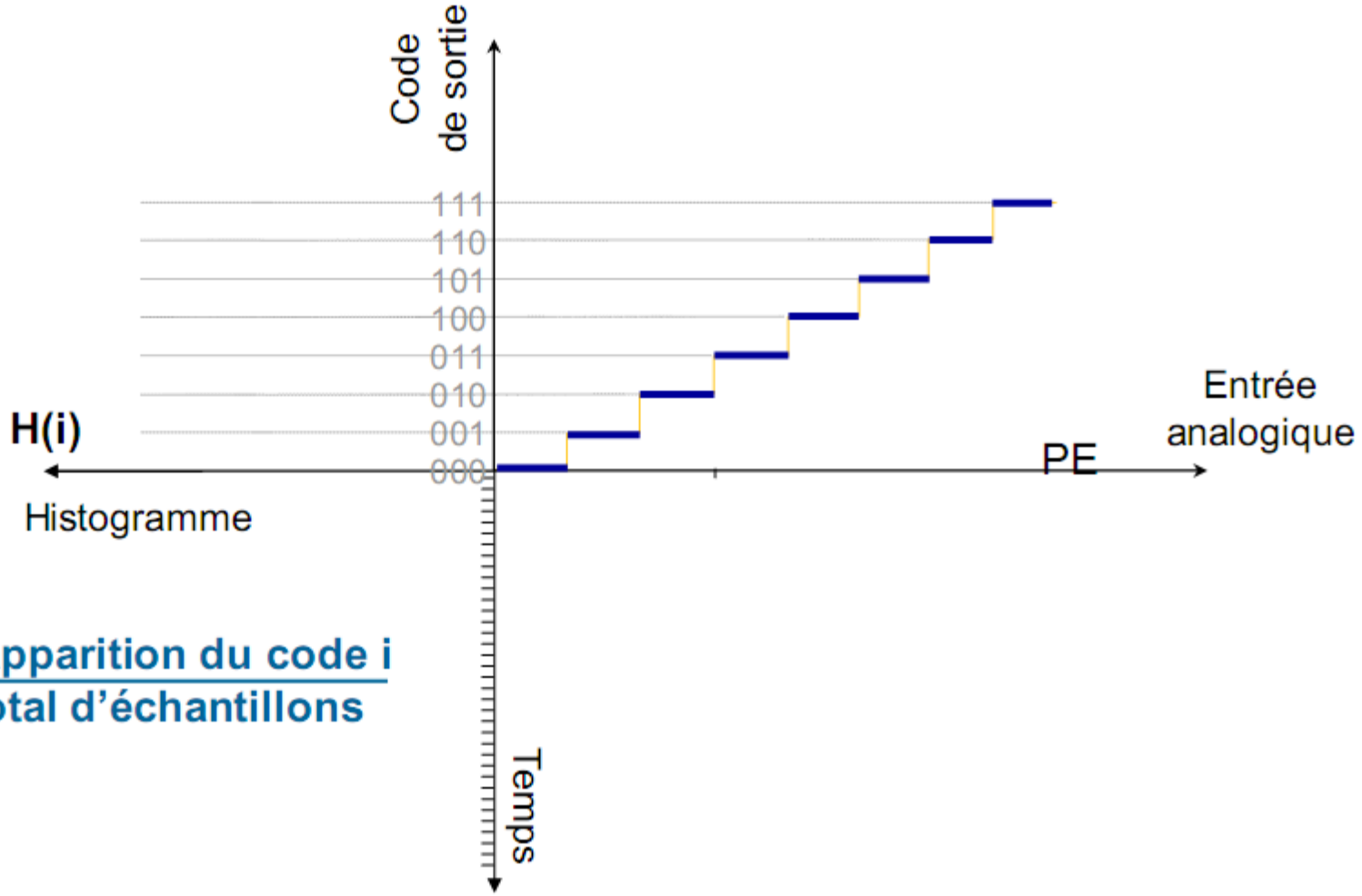
☹ Pas de paramètres Dyna.

☺ Précision

☺ Application Indus.

Source: S.Bernard, LIRMM [BER]

Test par histogramme

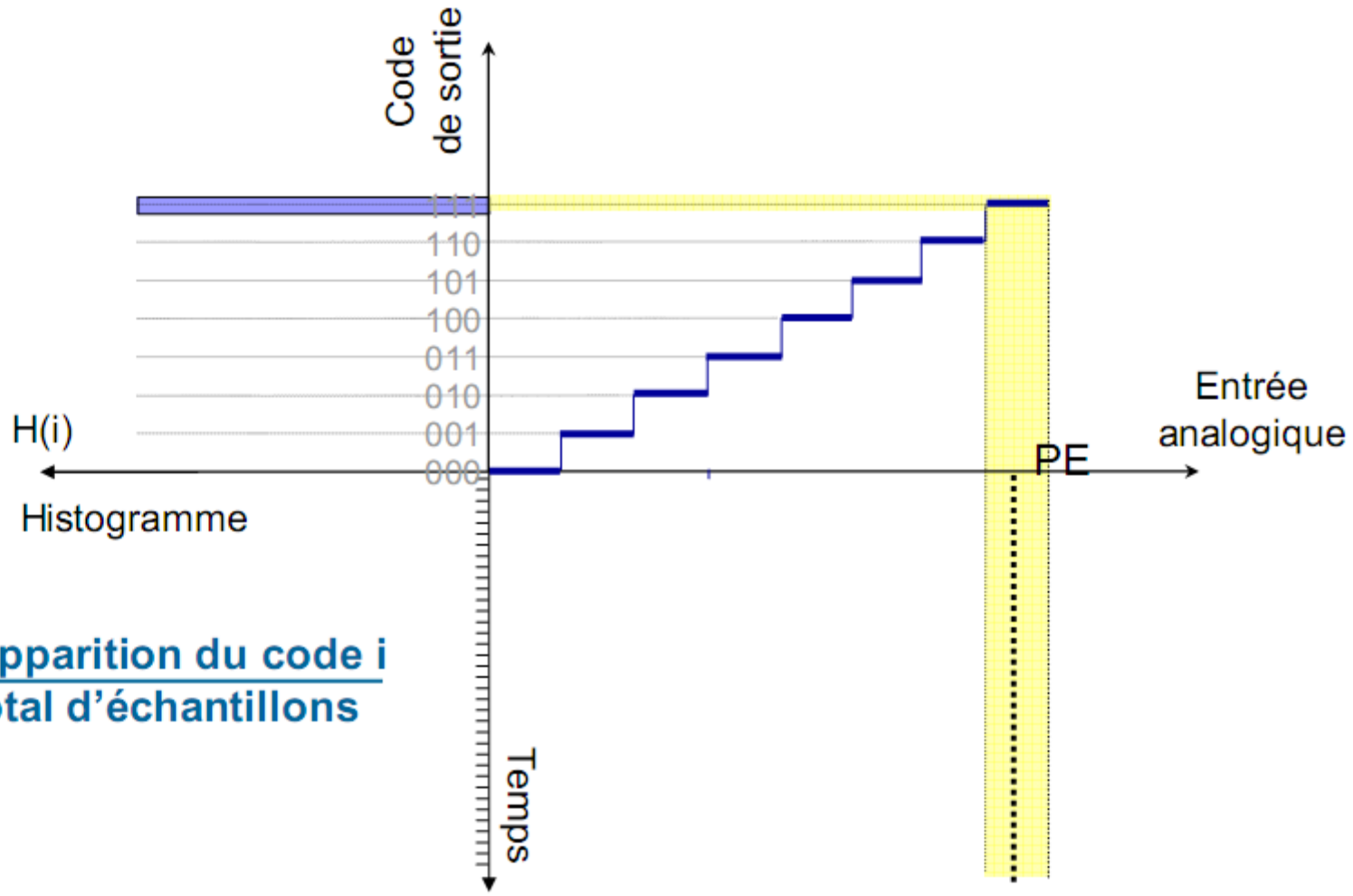


$$H(i) = \frac{\text{nbr d'apparition du code i}}{\text{nbr total d'échantillons}}$$

Source: S.Bernard, LIRMM [BER]

Test par histogramme

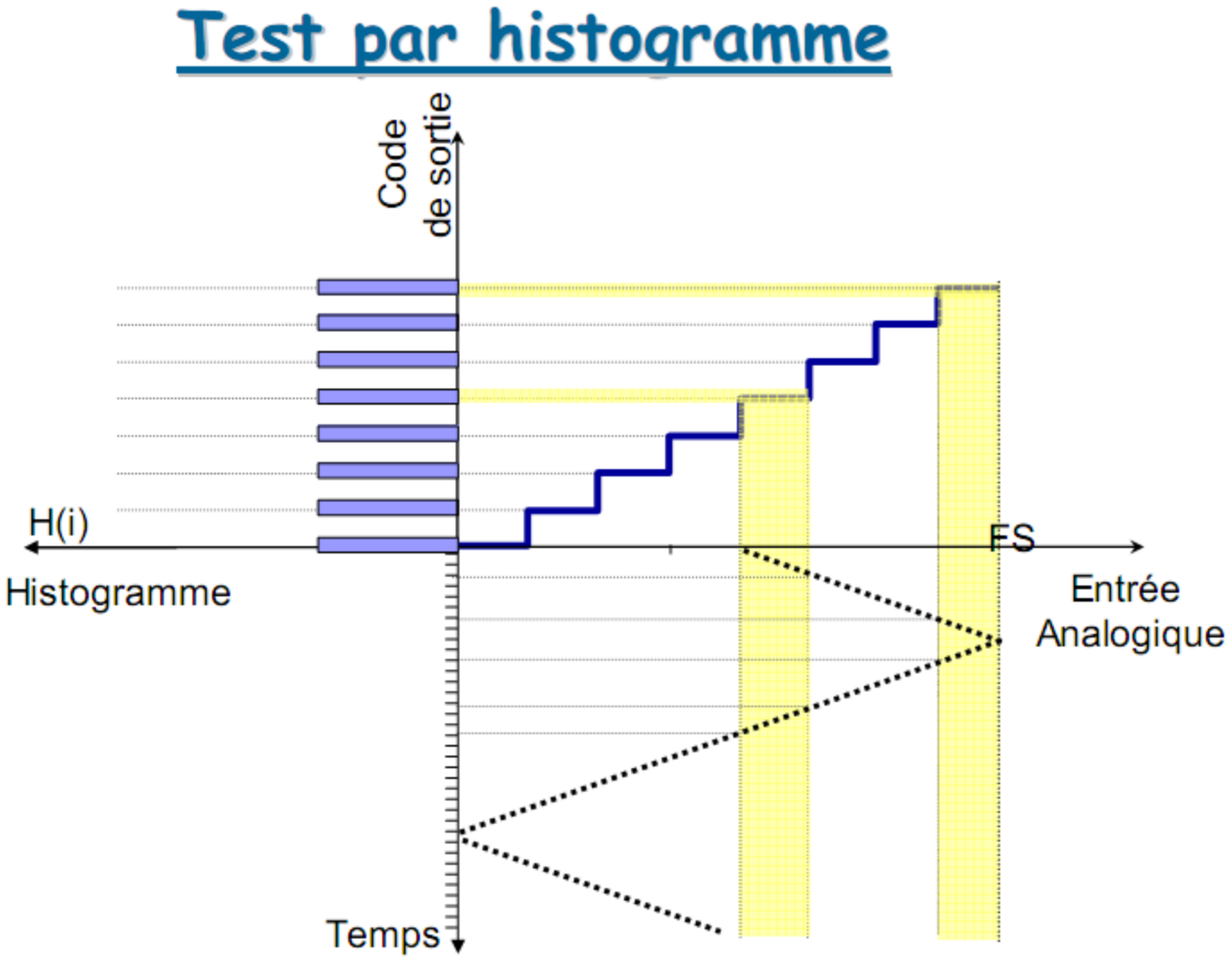
Test par histogramme



$$H(i) = \frac{\text{nbr d'apparition du code i}}{\text{nbr total d'échantillons}}$$

Source: S.Bernard, LIRMM [BER]

Test par histogramme



Source: S.Bernard, LIRMM [BER]

Test par histogramme

4.1.6.2 Alternate code transition location method based on ramp histogram

In this approach, a histogram of code occurrences is generated in response to an input signal level which ramps linearly between the extremes of the full-scale range of the ADC. After a sufficiently large number of samples [determined from Equation (61)], the histogram of the output provides an accurate measure of the differential nonlinearity of the ADC. Integral nonlinearity can be directly computed by numerically integrating the differential nonlinearity data.

The input ramp should be generated synchronously with the sampling clock, by a high-resolution DAC or arbitrary waveform generator with suitable linearity. Absolute signal level measurements can be made at the terminal codes to compute offset and gain errors. The statistics of this process, as noted in the comments below, can be used to calculate how many hits per bin should be used to achieve a given confidence level based on the equivalent input noise level.

The location of the code transitions, $T[k]$, can be extracted by manipulating the data that is collected in a histogram test with a ramp input. The code transition levels are given by Equation (56)

$$T[k] = C + A \cdot H_c[k-1] \qquad \text{for } k = 1, 2, \ldots, (2^N - 1) \tag{56}$$

where

A is a gain factor,

C is an offset factor,

Source: Norme IEEE [IEEE]

Test par histogramme

$H_r[j]$ is equal to $\sum_{i=0}^{j} H[i]$,

$H[i]$ is the number of histogram samples received in code bin i,

S is equal to $\sum_{i=0}^{2^N-1} H[i]$ = the total number of histogram samples.

The values of C and A can be computed directly from the collected data and the direct measurement of $T[1]$ and $T[2^N-1]$. The expressions for A and C are given by Equation (57) and Equation (58).

$$A = \frac{(T[2^N - 1] - T[1])}{(S - H[2^N - 1] - H[0])} \quad (57)$$

$$C = T[1] - \left(\frac{H[0] \times (T[2^N - 1] - T[1])}{(S - H[2^N - 1] - H[0])} \right) \quad (58)$$

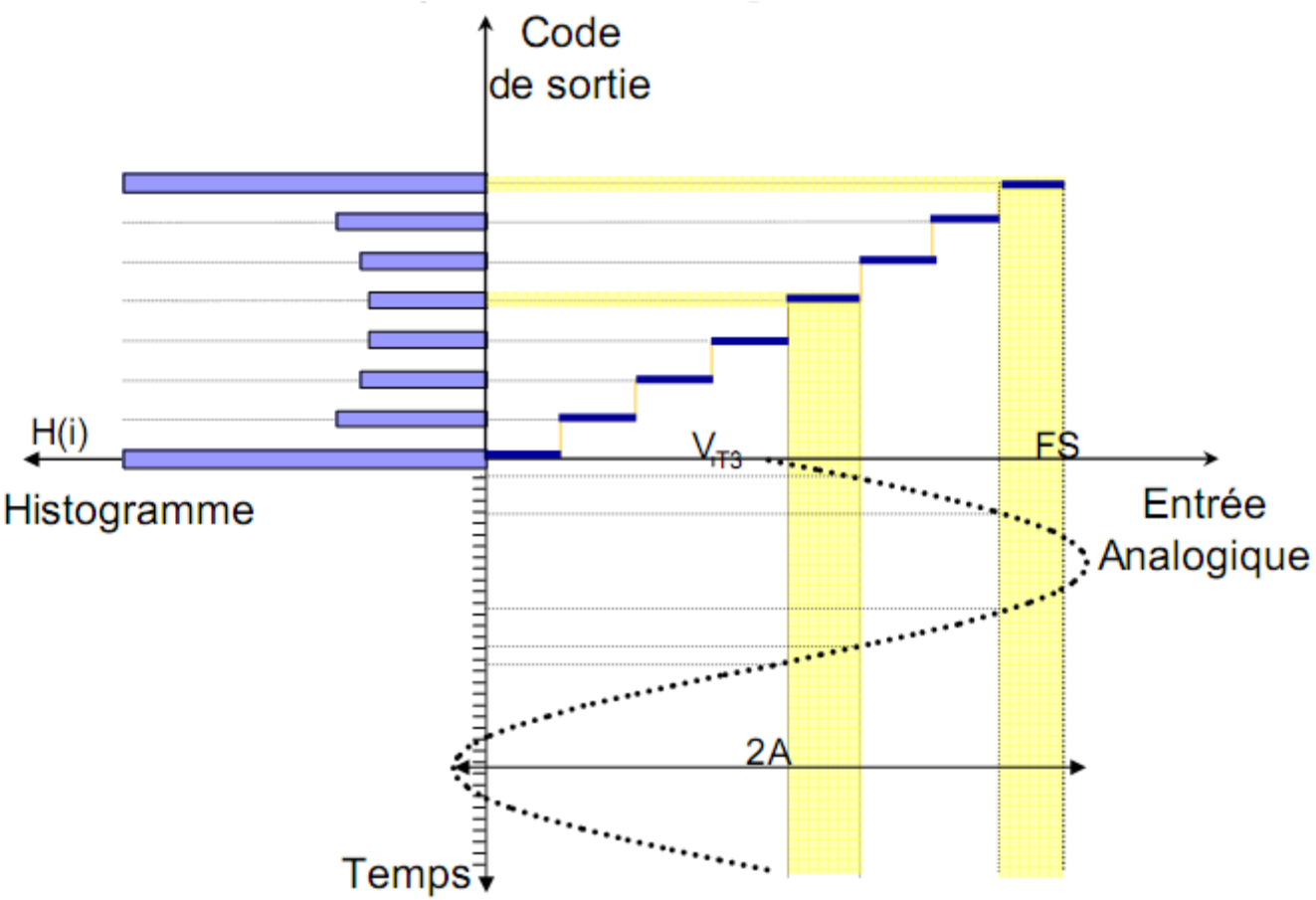
It should be noted that if code bins 0 and 2^N-1 are excluded (defined as having zero width) then the expressions reduce to Equation (59) and Equation (60).

$$A = \frac{(T[2^N - 1] - T[1])}{S} \quad (59)$$

$$C = T[1] \quad (60)$$

Source: Norme IEEE [IEEE]

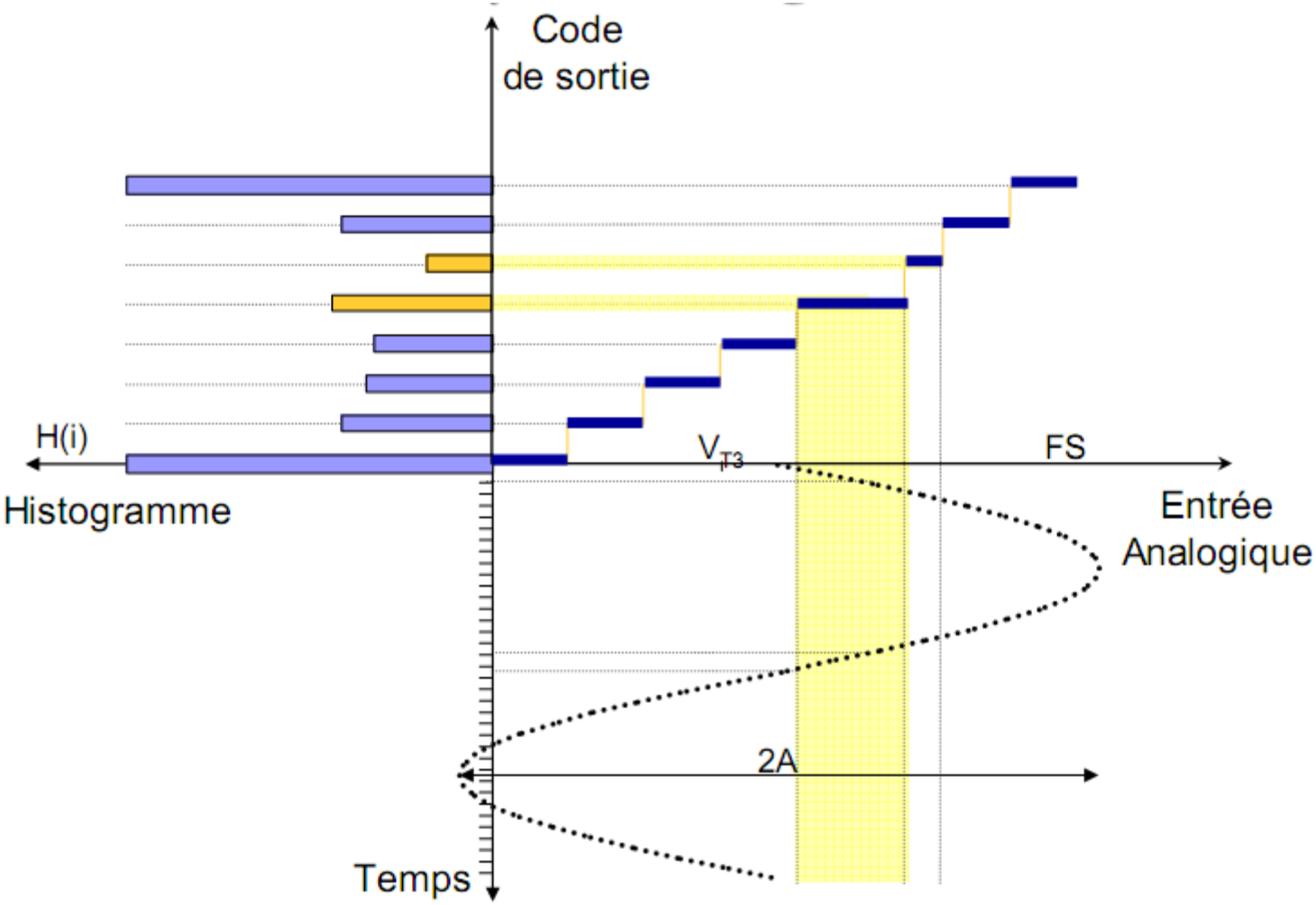
Test par histogramme



$$H^{réf}(i) = \frac{N_T}{\pi}\left(\arcsin\left[\left(\frac{2i-2^n}{2^n}\right)\cdot\frac{PE}{A_{in}}\right] - \arcsin\left[\left(\frac{2i-2^n-2}{2^n}\right)\cdot\frac{PE}{A_{in}}\right]\right)$$

Source: S.Bernard, LIRMM [BER]

Test par histogramme



Source: S.Bernard, LIRMM [BER]

Banc de test dynamique

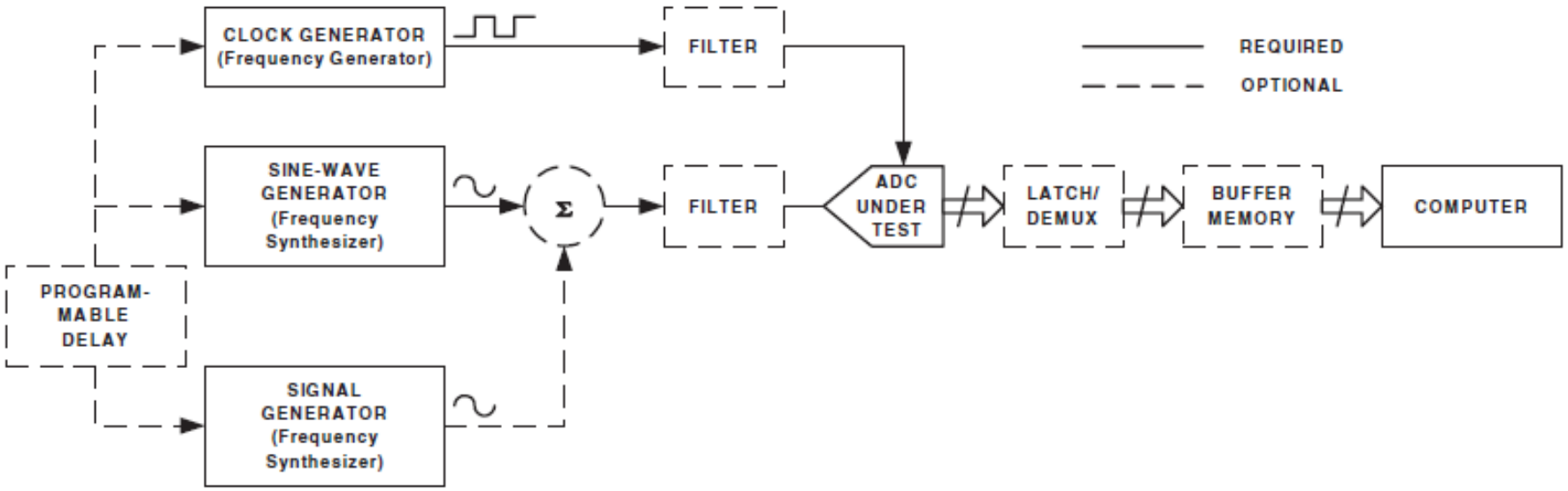


Figure 3—Setup for sine wave testing

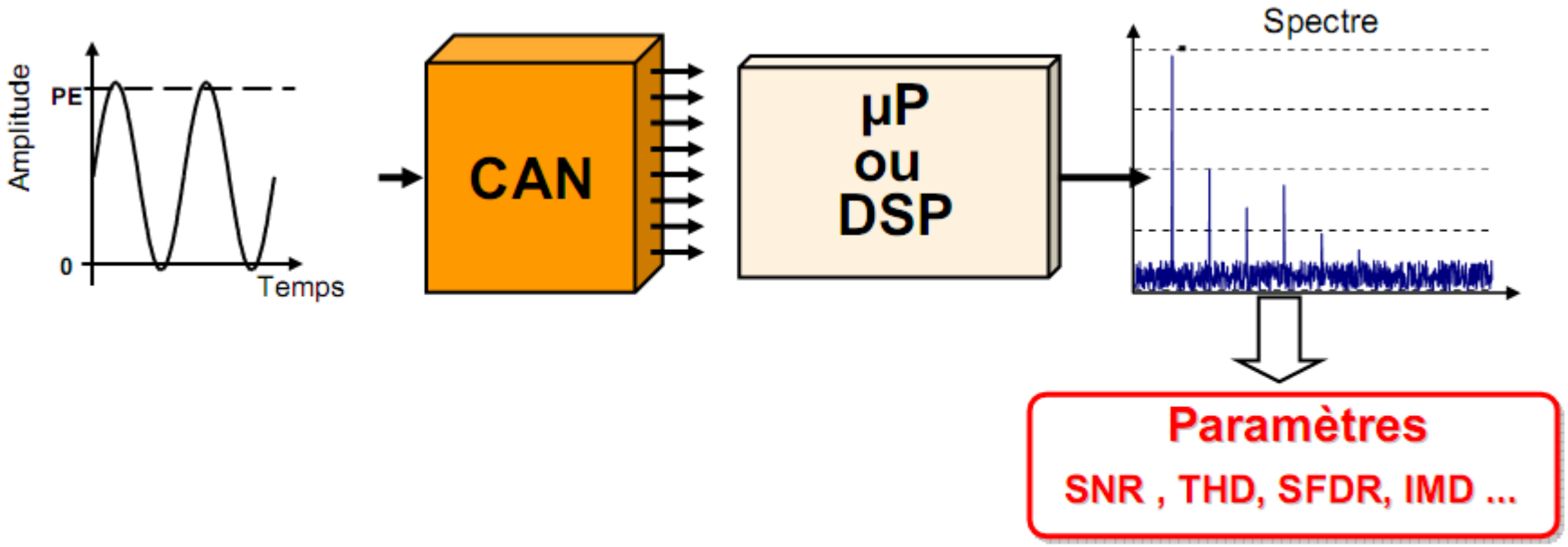
De la « pureté » fréquentielle du signal sinusoïdal d'entrée dépend la précision de la mesure.

Un filtrage sélectif sur la fréquence de test est généralement nécessaire → plusieurs filtres requis pour balayer une plage en fréquence.

Filtrage de l'horloge pour réduire le jitter.

Source: Norme IEEE [IEEE]

Test par FFT



☹ Sensible à la Synchro.

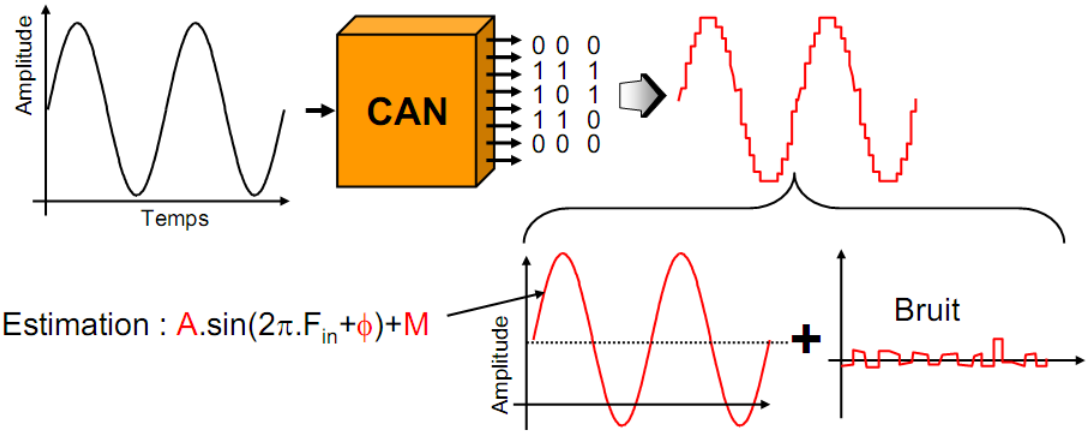
☹ Pas de paramètres Stat.

☺ Rapide

☺ Application Indus.

Source: S.Bernard, LIRMM [BER]

Régression sinusoïdale (1)



- **Principe :**
  - ✓ **Signal d'entrée sinusoïdal (1.sin(2π.Fin+ϕ))** → Signal « parfait »
  - ✓ **Estimer le signal sinusoïdal de la forme (A.sin(2π.Fin+ϕ)+M) vu à travers le convertisseur**
  - ✓ **Les paramètres M, A donnent respectivement la valeur du gain et de l'offset du CAN sous test**

☹ **Complexité**
☹ **Temps de calcul**
☹ **Peu utilisé**

Fonction sous ***sfit4*** MATLAB:
→ estime l'erreur rms par rapport à sinusoïde idéale
→ estime l'ENOB =log2(2^n_bits/(X.erms*sqrt(12)))

☺ **Précision**

Source: S.Bernard, LIRMM [BER]

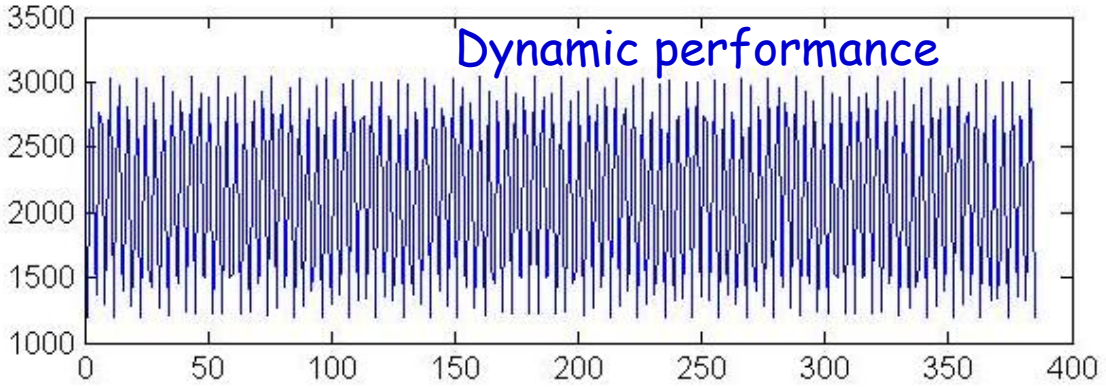
Régression sinusoïdale (2)

Fonction sous ***sfit4*** MATLAB:

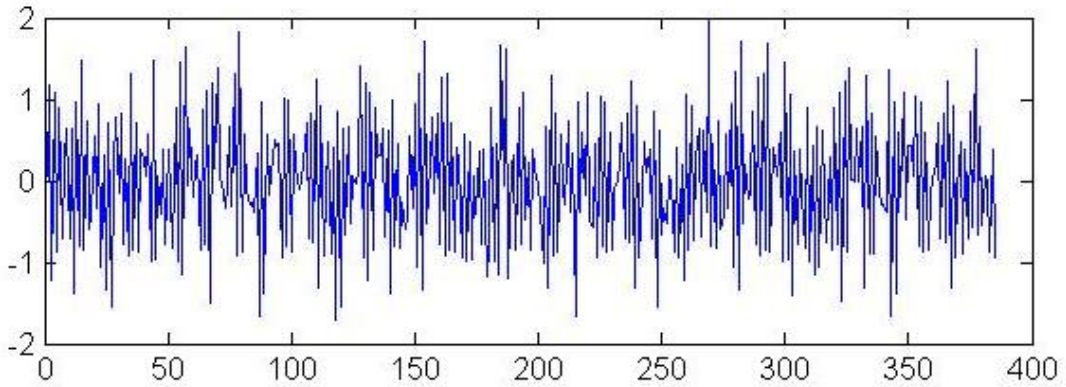
→ estime l'erreur rms par rapport à sinusoïde idéale

→ estime l'ENOB =log2(2^n_bits/(X.erms*sqrt(12)))

```
%SFIT4  IEEE-STD-1241
Standard four parameter
fit of a sine wave to
measured data
```



ENOB=10.5 @ 10.625MHz



Autres bancs de test

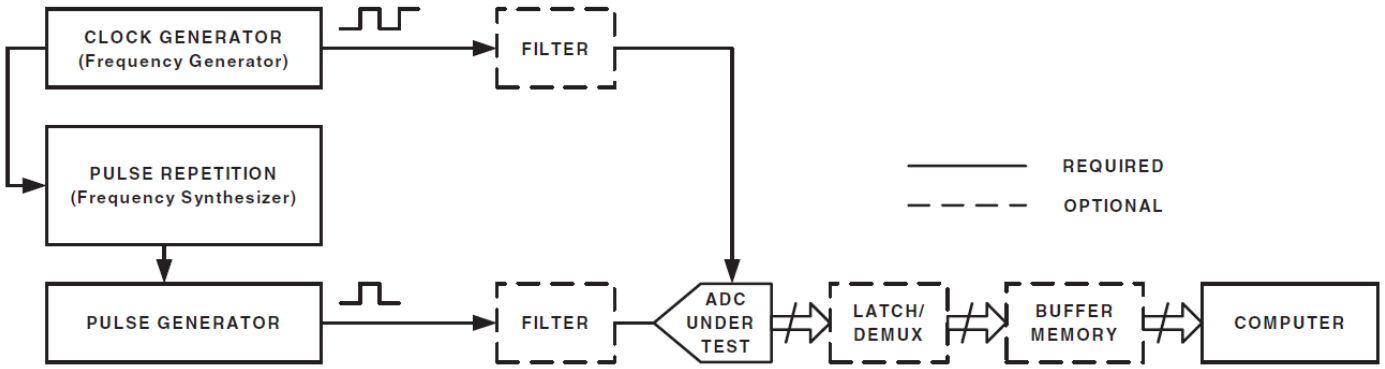


Figure 5—Setup for pulse and step signal tes

Locating code transitions using a feedback loop

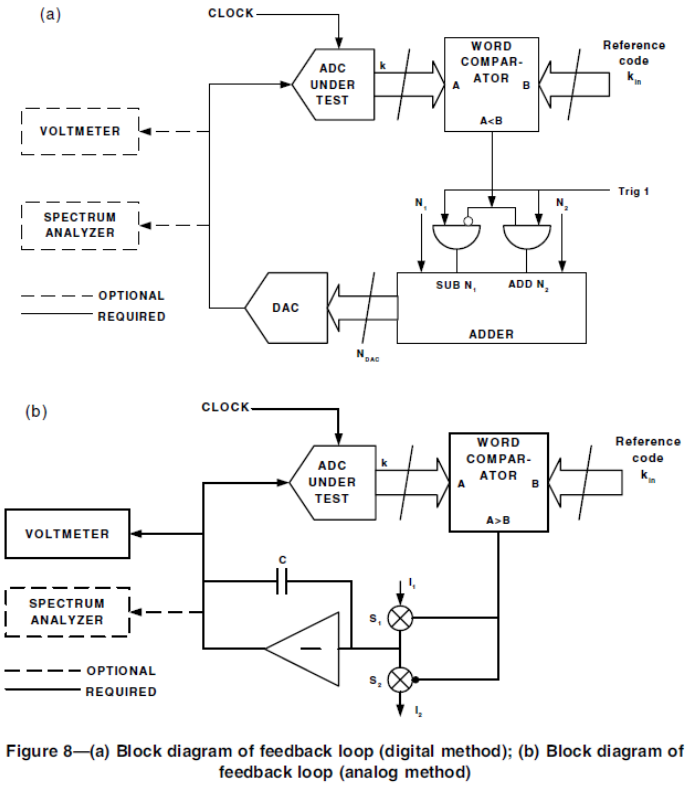
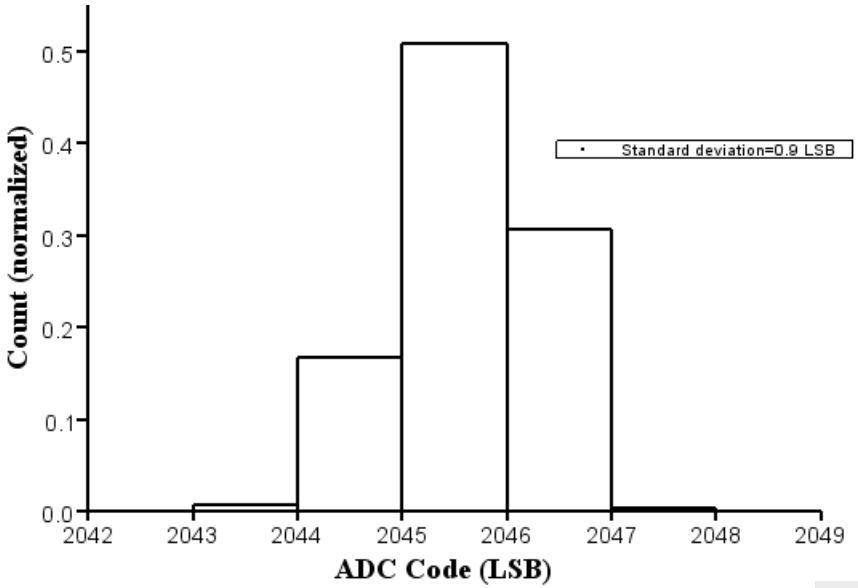


Figure 8—(a) Block diagram of feedback loop (digital method); (b) Block diagram of feedback loop (analog method)

Mesure du Bruit

Méthode utilisée @ LPC:

- Mettre un signal fixe à l'entrée de l'ADC; filtrer très basse fréquence
- Acquérir les données en sortie de l'ADC
- Tracer l'histogramme de distribution des codes; déterminer la déviation standard
- Effectuer cette mesure pour différentes valeurs de tension d'entrée.
- Cette mesure de bruit peut être réalisée sur toute la gamme avec le test de la rampe et *n* mesures par paliers

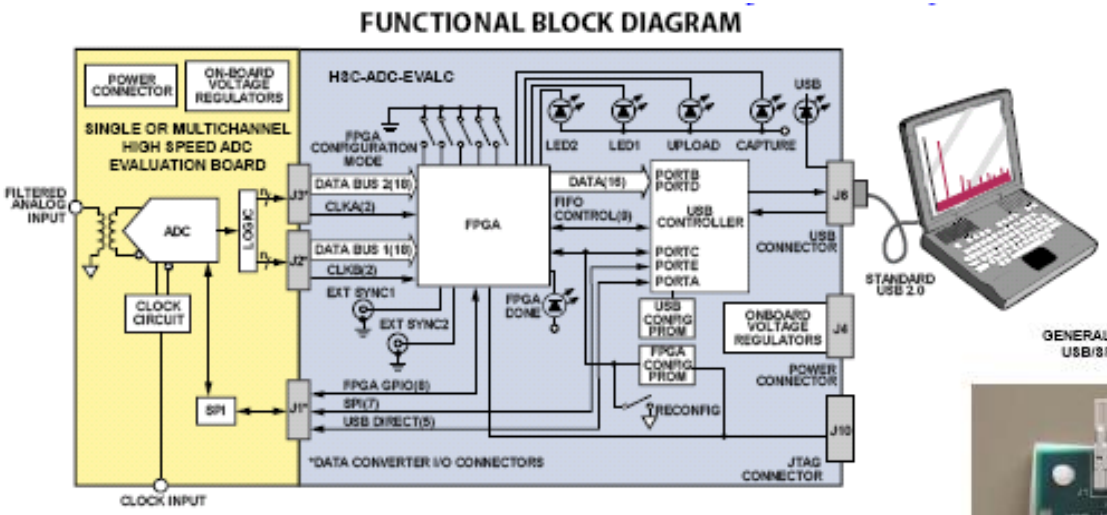


Source: LPC-Clermont

2. Evaluer un ADC:

⇨ des cartes d'évaluation

Exemple de carte d'évaluation: AD



- **1 carte support de l'ADC à tester + 1 carte générique d'acquisition**
- **Logiciel d'analyse/affichage des données: VisualAnalog**

VisualAnalog.exe

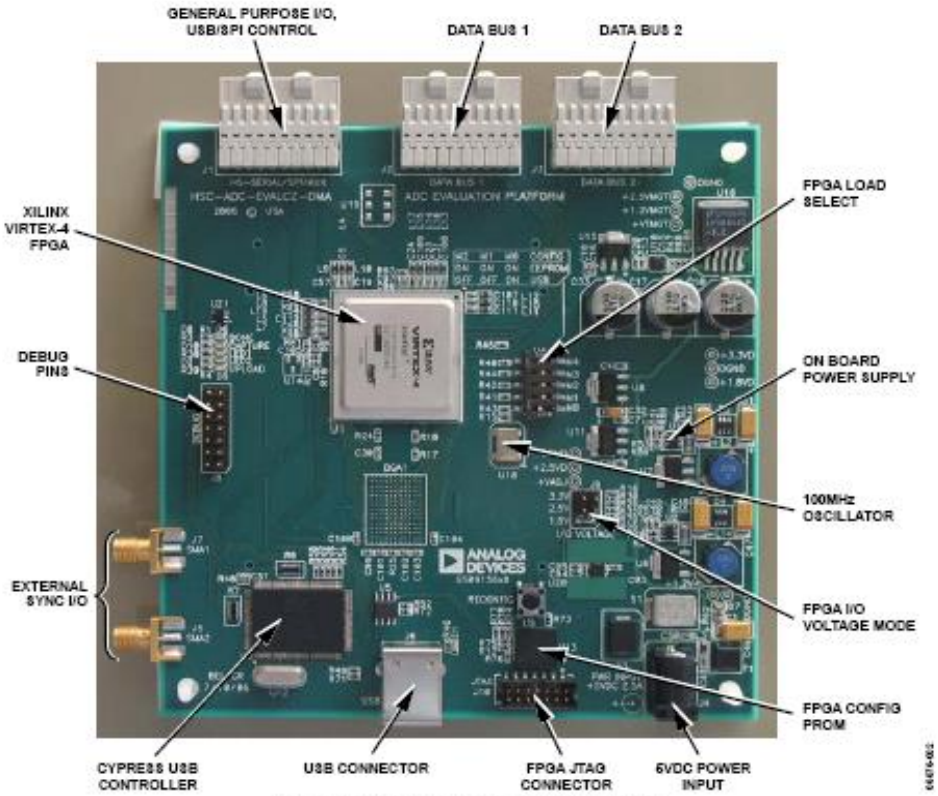


Figure 3. HSC-ADC-EVALC Components (Top View)

Exemple de carte d'évaluation: Linear T. & Maxim

- **Linear Technology: DC718B - QuickDAACS USB Controller for QuickEval-II Evaluation Kits**

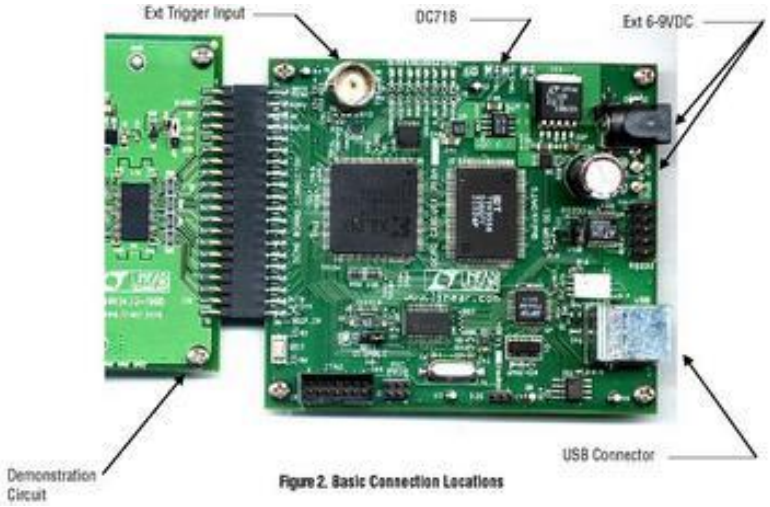
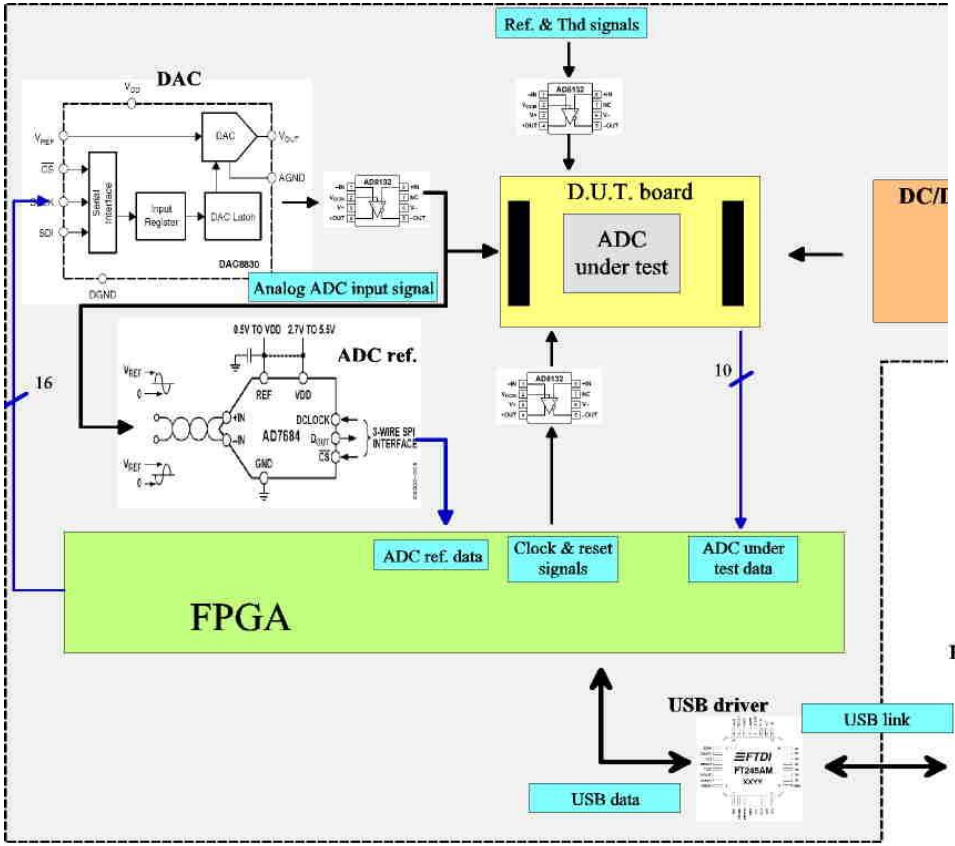


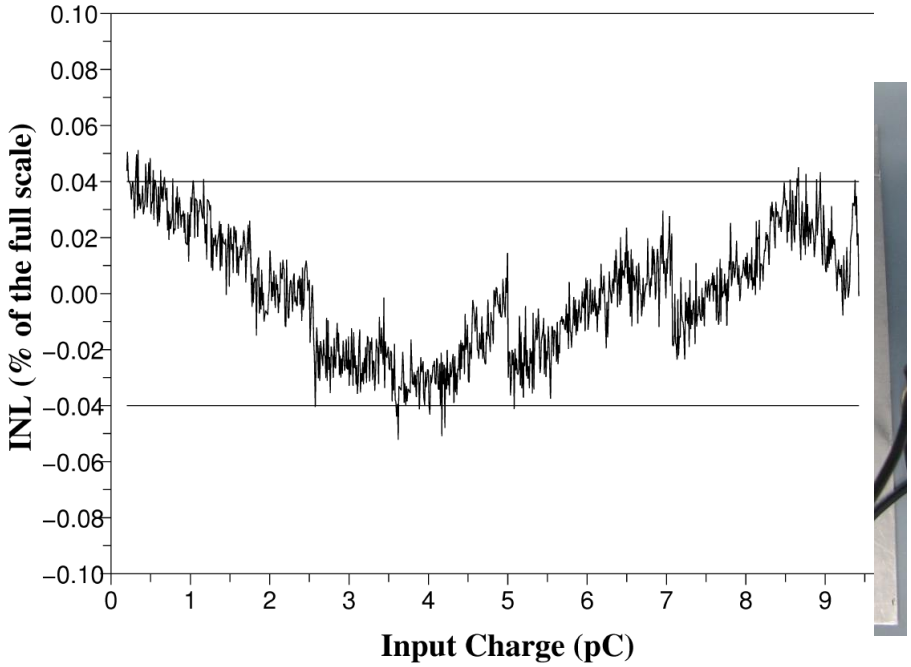
Figure 2. Basic Connection Locations

- **Maxim: *68HC16 Module***

Banc de test dédié @ LPC

- Banc de test générique, piloter par PC/LabView via USB, avec:
  - ADC AD7684 différentiel, 16 bits, 100kS/s → ADC de référence
  - DAC 16 bits + FPGA +USB driver → signal d'entrée type « rampe »





PC/LabView interface control

2. Evaluer un ADC:

⇨ tenue aux radiations

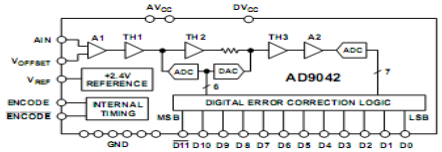
Tenue aux radiations

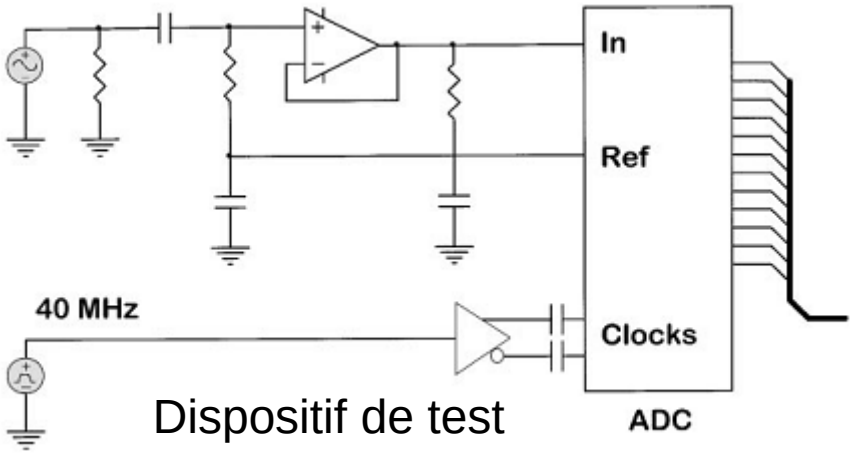
- Les ADC en milieu radiatif sont sensibles:
  - à la dose ionisante:
    - ✓ dérive de la consommation en courant
    - ✓ dérive de la précision
    - ✓ du temps de conversion
    - ✓ de la référence de tension interne
    - ✓ …
  - aux phénomènes de latch-up (SEL: Single Event Latch-up) si la technologie est CMOS (la plus répandue aujourd'hui) ou BiCMOS
  - aux SEU (Single Event Upset)
  - aux SET (Single Event Transient)
  - aux SEFI (Single Event Fonctional Interrupt)

Source: D.Danglan et F.Malou (CNES) [DAN]

Tenue aux radiations: exemple de l'AD9042 (1)

- ADC AD9042 12bits - 40MS/s utilisé pour les calorimètres électromagnétiques d'Atlas et CMS
  - architecture pipeline
  - technologie bipolaire XFCB 1.0 (eXtra Fast Complementary Bipolar).
  - doit tenir à dose jusqu'à 300 krad pour Atlas et 1 Mrad pour CMS
  - Définition avec Analog Devices du processus de test:





Dispositif de test

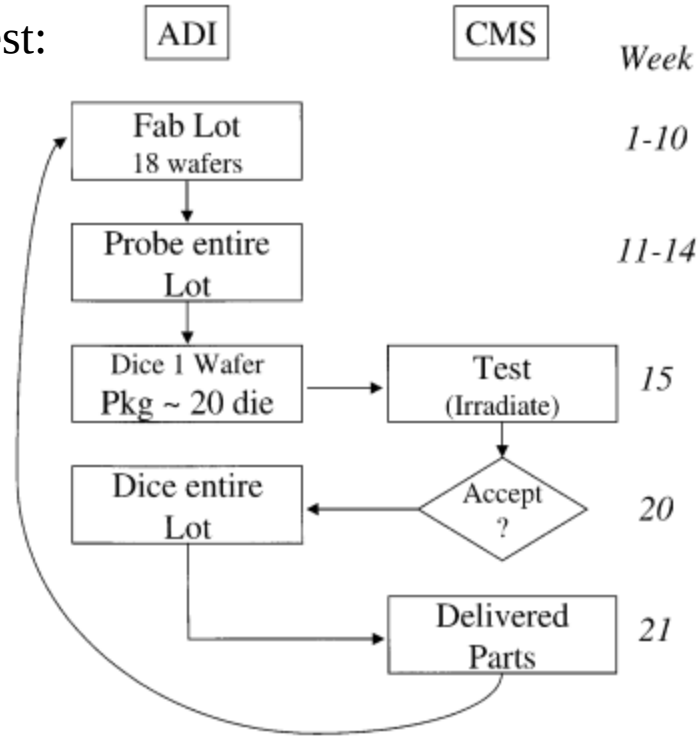


Fig. 1. ADC process flow for CMS.

Source: P.Denes [CMS2]

- 1 cycle = 21 semaines
- 32 ADC x 16 wafers = 512 ADC testés

Tenue aux radiations: exemple de l'AD9042 (3)

❑ Mesure du gain

✓ Augmentation de la tension de référence avec la dose → baisse du gain ADC

✓ Utilisation possible d'une référence externe rad-hard et/ou correction off-line

10^{13}p/cm^2 ⇔ 1Mrad

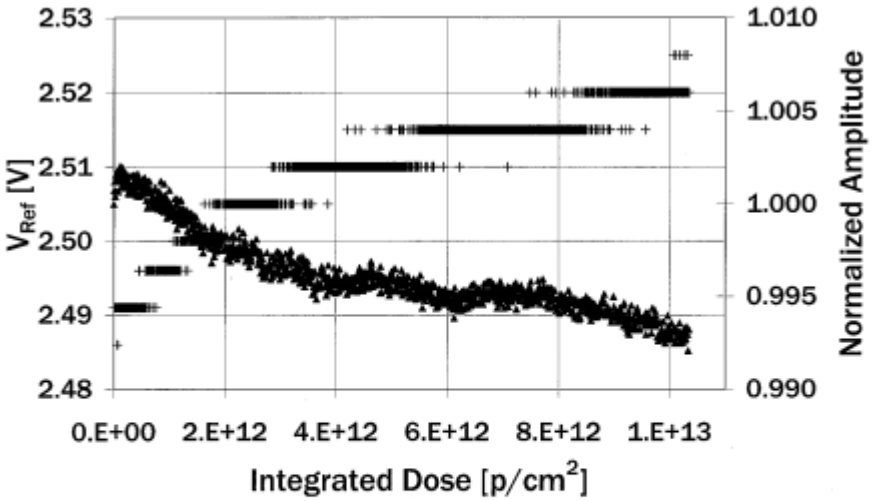


Fig. 7. Amplitude and voltage reference change during irradiation. The crosses indicate the measured value of the ADC voltage reference on the left-hand scale, and the triangles indicate the normalized change in amplitude for a 5 MHz full-scale sine wave on the right-hand scale.

Source: P.Denes [CMS2]

Tenue aux radiations: exemple de l'AD9042 (4)

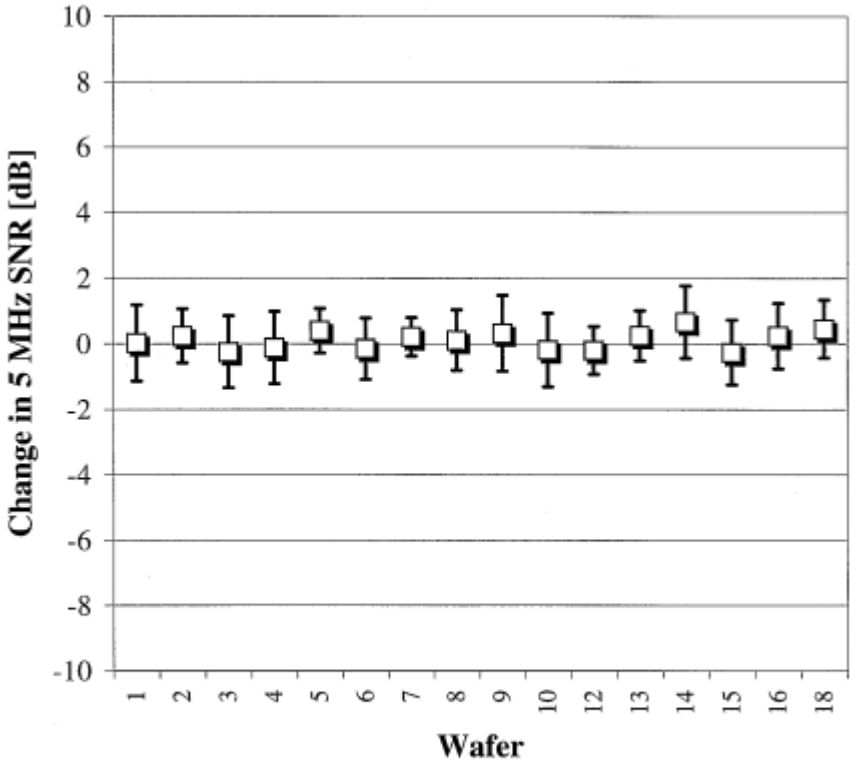


Fig. 5. Change in 5 MHz SNR for ADCs exposed to 10^{12} p/cm^2 as a function of wafer number. The open squares represent the average of the ADCs irradiated, and the error bars the RMS.

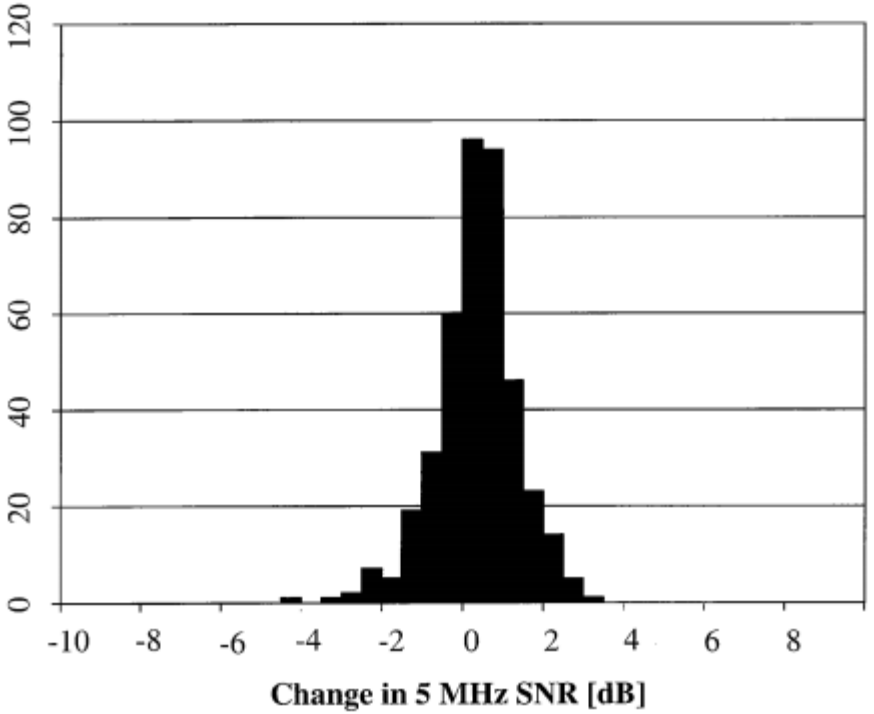


Fig. 6. Change in 5 MHz SNR for all ADCs exposed to 10^{12} p/cm^2, i.e. a histogram of the data in Fig. 5.

10^{13}p/cm^2 ⇔ 1Mrad

SNR moyen mesuré de 63 dB contre 68 dB théorique

➢ système de test à améliorer

Source: P.Denes [CMS2]

Tenue aux radiations: exemple de l'AD9042 (2)

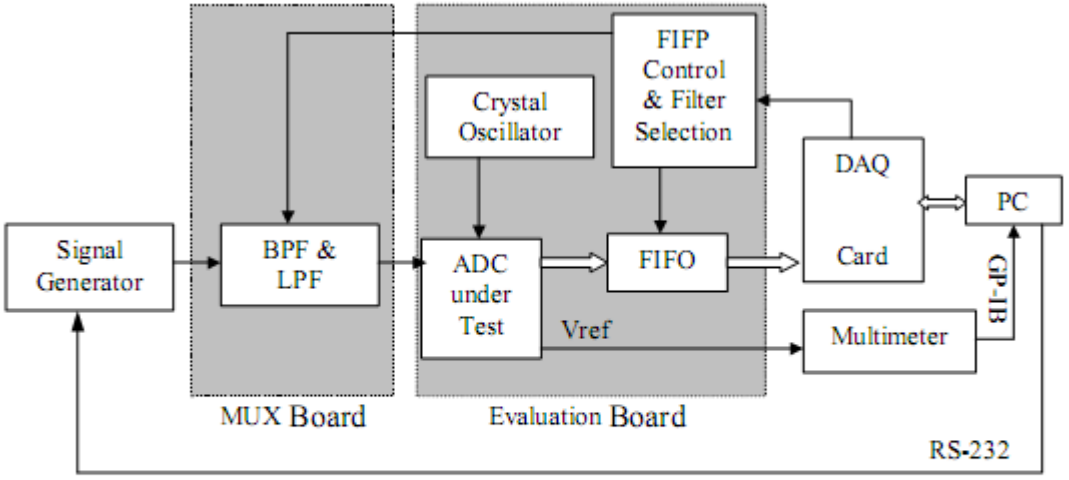
❑ Mesure du SNR de l'ADC AD9042:

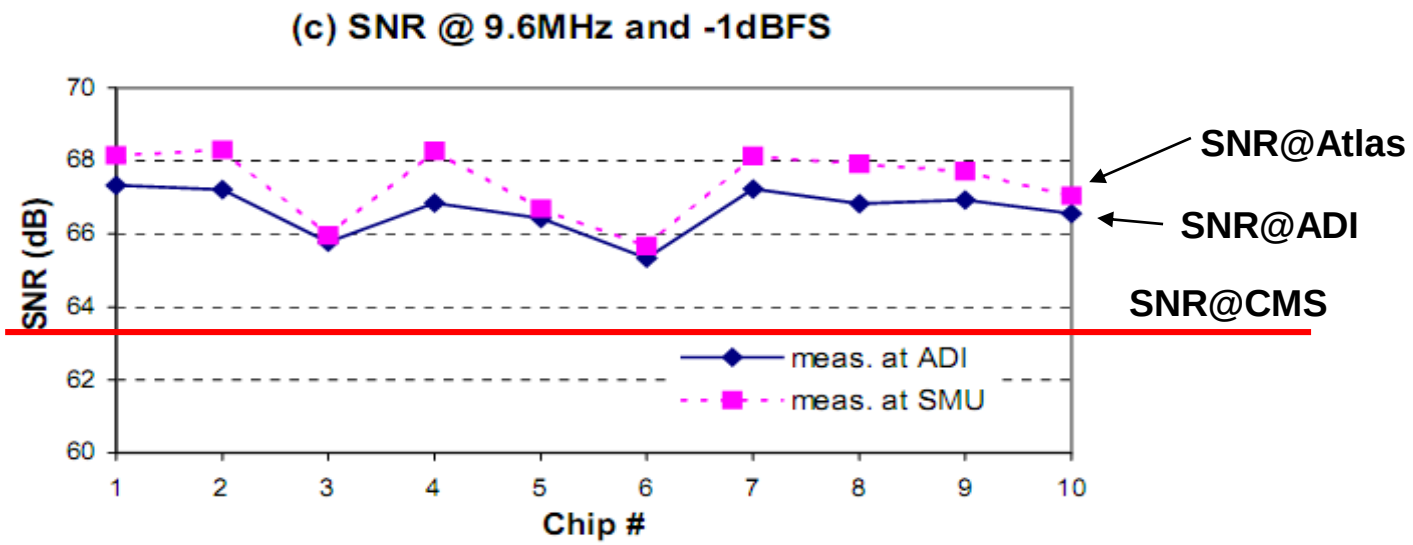
- ➢ le SNR de l'ADC est de 68 dB; le banc de test doit donc être très bas bruit:
  - ✓ signal d'entrée très bas bruit et très faibles harmoniques
    - → générateur Rohde-Schwartz + filtre passe-bande
  - ✓ très faible jitter de l'horloge (4 ps rms: bruit équivalent de 1 LSB)
    - → XO-400 crystal oscillator (Vectron International): jitter de 0.5 ps rms
    - → 1:2 buffer MC10EP11 de On Semiconductor C. jitter de 0.2 ps rms
  - ✓ très bas bruit du PCB et système complet
    - → PCB 4 couches: 1 plan de masse, 1 plan d'alim. divisé en 2 (analog & digital)
    - → support de qualité
    - → connectique SMA

Source: T.Liu et al. [SMU]

Tenue aux radiations: exemple de l'AD9042 (5)

- Amélioration du dispositif de test de circuits :





Exemple d'ADC certifié « spatial »

- ADC AT84AS008 de e2v (ex ATMEL):
  - Principales caractéristiques:
    - ✓ 10 bits – 2.2GS/s – Techno. SiGe
    - ✓ ENOB: 8bits@1.7GS/s, 7.7bits@2.2GS/s
    - ✓ SNR: 51 dB à 2.2G/s
    - ✓ 4,2W/±5V
    - ✓ prix: 1300$/1000 pièces

  - Evaluation spatiale:
    - ✓ évaluation performances entre -55/+125°C et Vcc min et Vcc max
    - ✓ endurance 3000h à 125°C sur 20 pièces
    - ✓ chocs mécaniques et thermiques, vibrations, cycles thermiques
    - ✓ essais en radiations en dose cumulée jusqu'à 150krads à un débit de 50rad/h
    - ✓ essais en radiations sous ions lourds: SEL, SEFI, SEU

Source: e2v [AT84] et D.Danglan/F.Malou (CNES) [DAN]

3. Utiliser un ADC:

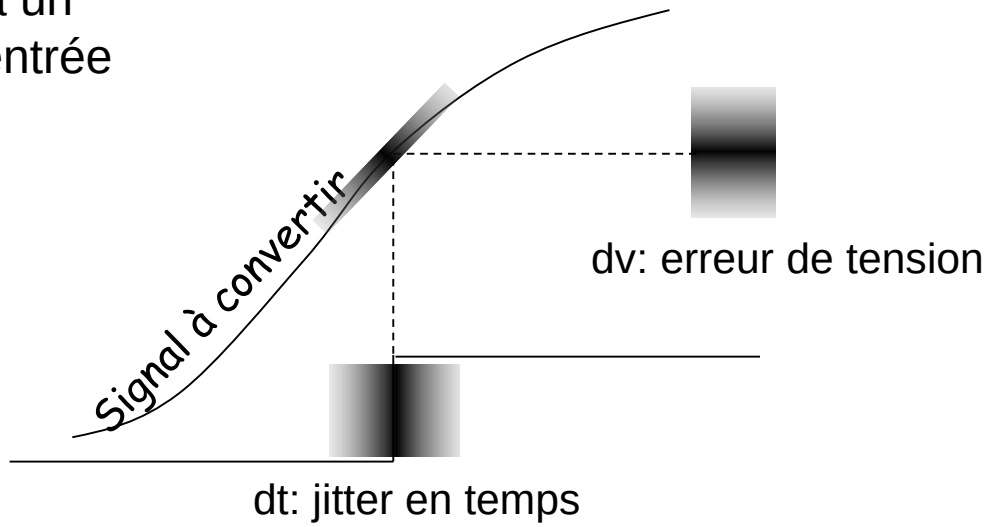
⇨ la fluctuation de l'instant d'échantillonnage

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Définitions

APERTURE (SAMPLING) DELAY: délai de temps entre la commande d'ouverture de l'interrupteur d'échantillonnage et son ouverture effective.

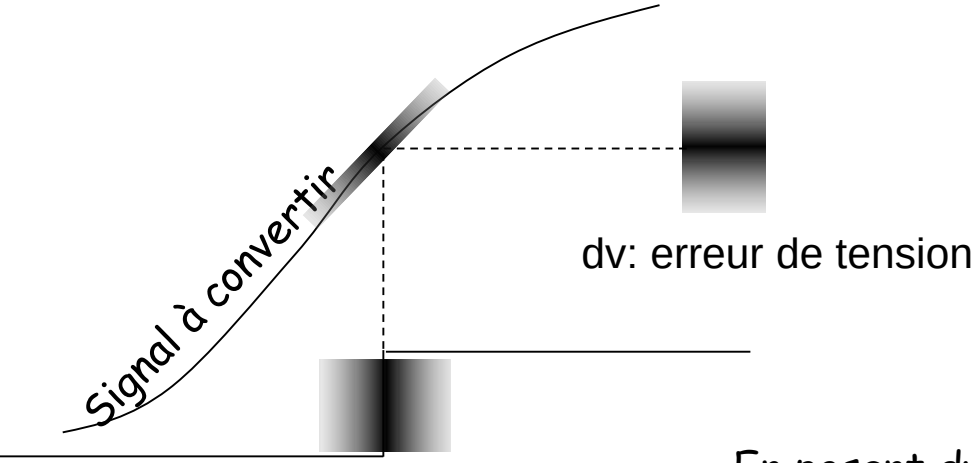
APERTURE JITTER: variation du Apperture delay d'un échantillon à un autre. Cette variation est vue en entrée comme un bruit.



Source: B.Brannon et A. Barlow (AD) [BRA] et J.Lecoq [LEC]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Relation entre l'erreur d'instant d'échantillonnage et l'erreur de tension échantillonnée



Considérons un signal d'entrée v(t) sinusoïdal:

$$v(t) = A\sin(2\pi \cdot f \cdot t)$$

L'erreur de tension est la dérivée en temps:

$$\frac{dv}{dt} = A \cdot 2\pi \cdot f \cos\cdot(2\pi \cdot f \cdot t)$$

L'erreur est max pour cos(2πft)=1 soit t=0:

$$\left.\frac{dv(0)}{dt}\right|_{MAX} = A \cdot 2\pi \cdot f$$

En posant dv = V_{ERR}, l'erreur de tension introduite par la variation de temps dt = t_a est donnée par (valeurs rms) :

$$V_{ERR} = A \cdot 2\pi \cdot f \cdot t_a \quad \text{ou} \quad t_a = \frac{V_{ERR}}{A \cdot 2\pi \cdot f}$$

- L'erreur augmente linéairement avec la fréquence du signal d'entrée.
- L'origine de la fluctuation en temps t_a est le bruit du signal d'horloge.

Source: B.Brannon et A. Barlow (AD) [BRA] et J.Lecoq [LEC]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Détermination de l'erreur d'instant d'échantillonnage maximale acceptable pour un ADC

Soit un signal Vin = A.sinωt converti avec un ADC de résolution N.
L'erreur maximale tolérable est:

$$V_{ERR}\big|_{\max} = \frac{2 \cdot A}{2^N}$$

$$t_a = \frac{V_{ERR}}{A \cdot 2\pi \cdot f} \quad \Rightarrow \quad t_a\big|_{\max} = \frac{V_{ERR}\big|_{\max}}{A \cdot 2\pi \cdot f} = \frac{1}{2^N \cdot \pi \cdot f}$$

Exemples !

L'audio: 20kHz, 16 bits..... Δt=200 ps
La vidéo: 100MHz, 8 bits ..... Δt=12 ps
La Hi-Fi: 20kHz, 20 bits..... Δt=12 ps
NEW audio.....24 bits..... Δt=0,8 ps
Oscillo. 2GHz, 8 bits..... Δt=0,5 ps

Source: B.Brannon et A. Barlow (AD) [BRA] et J.Lecoq [LEC]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Contribution de l'erreur d'instant d'échantillonnage sur le SNR

$$SNR = -20\log\left[(2\pi \cdot f \cdot t_a)^2 + \left(\frac{1+\varepsilon}{2^N}\right)^2\right]^{1/2}$$

contribution du jitter

autres contributions (DNL, bruit quantification, bruit thermique…

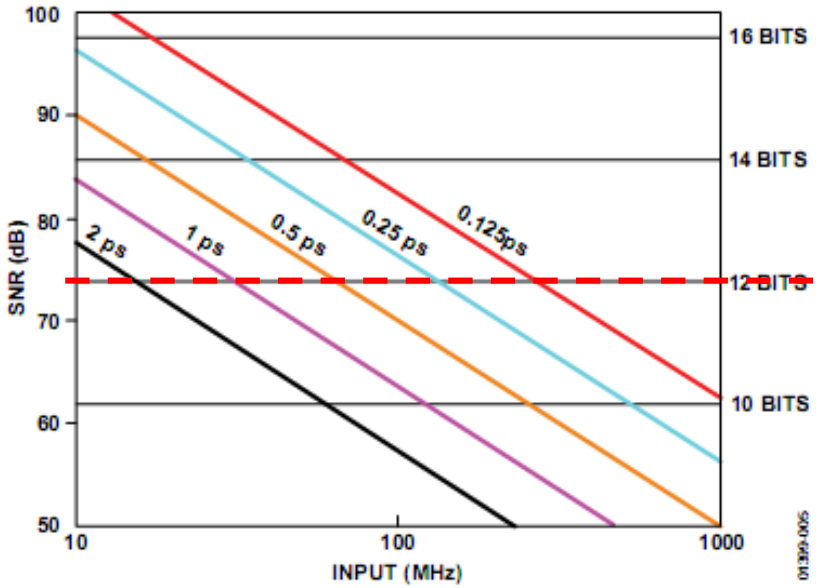


Figure 5. Signal-to-Noise Ratio Due to Aperture Jitter

SNR (dB) max. théorique pour un ADC à N bits (bruit de quantification):

SNR= 6,02 . N + 1,76

soit 74 dB pour un ADC 12 bits

Limite théorique SNR ADC 12 bits

Source: B.Brannon et A. Barlow (AD) [BRA]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Détermination de t_a à partir des mesure de SNR

$$SNR = -20\log\left[\underbrace{(2\pi \cdot f \cdot t_a)^2}_{} + \underbrace{\left(\frac{1+\varepsilon}{2^N}\right)^2}_{}\right]^{1/2}$$

La valeur de t_a peut être évaluée en effectuant 2 mesures de SNR.
Avec f suffisamment bas:

$$SNR\big|_{low\cdot f} \approx -20\log\left(\frac{1+\varepsilon}{2^N}\right)^2 \quad \Rightarrow \quad \varepsilon \approx 2^N \cdot 10^{\frac{-SNR}{20}} - 1$$

A haute fréquence on obtient:

$$t_a = \frac{\sqrt{\left(10^{\frac{-SNR\big|high\cdot f}{20}}\right) - \left(\frac{1+\varepsilon}{2^N}\right)^2}}{2\pi \cdot f}$$

Source: B.Brannon et A. Barlow (AD) [BRA]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Exemple d'évaluation de t_a

- ADC AD9256, 14 bits à 125MS/s
- kit d 'évaluatation Analog Devices

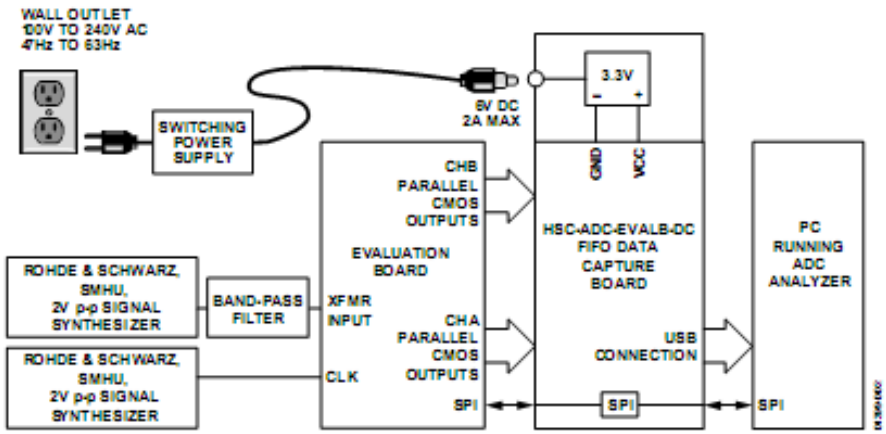


Figure 2. Aperture Uncertainty Measurement Setup with AD9246 Customer Evaluation Board

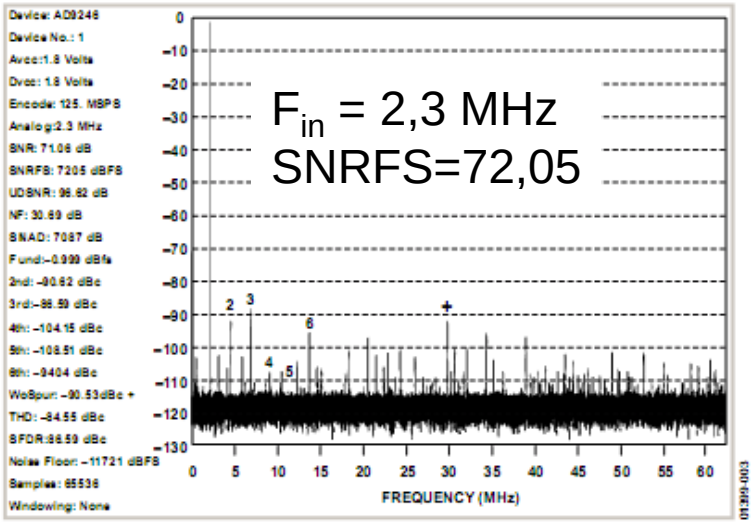


Figure 3. 2.3 MHz FFT

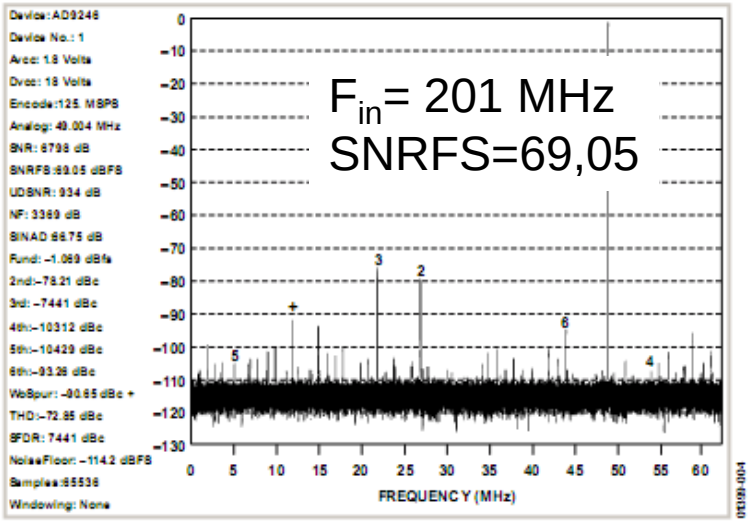


Figure 4. 201 MHz FFT

A partir des 2 mesures on obtient: **t_a = 197 fs**

Remarque: la valeur obtenue t_a est la somme quadratique des contributions du générateur et de l'ADC lui-même. Si la contribution du générateur est connue, on peut en déduire celle de l'ADC.

Source: B.Brannon et A. Barlow (AD) [BRA]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Dégradation du SNR vs aperture jitter

- SNR (dB) max. théorique pour un ADC à N bits (bruit de quantification):

  SNR= 6,02 . N + 1,76 soit 49,9 dB pour un ADC 8 bits

- Dégradation du SNR vs *clock jitter:*

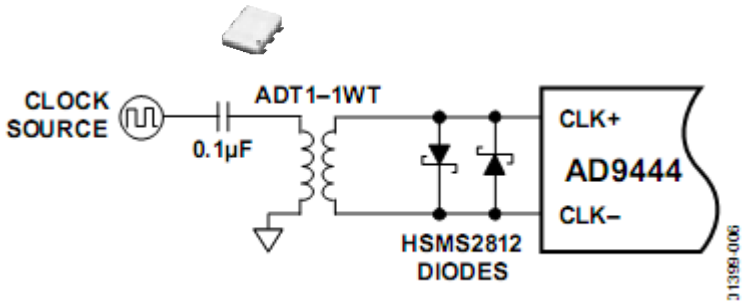
Allowable Clock Jitter (fs.)	Total SNR Due to Quantization Noise and Jitter (dB) $SNR = 10 \log \left(\frac{1}{\frac{1}{10^{\frac{SNR_J}{10}}} + \frac{1}{10^{\frac{SNR_Q}{10}}}} \right)$
142	48.5
259	48.2
354	47.8
447	47.4
541	46.9
640	46.4
747	45.8
862	45.2
989	44.5

Source: J.Catt (NS) [CATT]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Mise en œuvre de l'horloge

- Signal d'horloge sinusoïdal différentiel
  - recommandé pour ADC rapide
    - ✓ jitter réduit par rapport signal logique
    - ✓ utilisation de transformateur RF « balun » pour distribution de l'horloge
    - ✓ adaptation d'impédance interne



- Signal d'horloge logique différentiel
  - LVDS jusqu'à 1,5 GS/s ADC rapide (ADC081500 de NS)
  - adaptation d'impédance interne
  - routage sensible des signaux
  - attention au distribution d'horloge
  - utilisation de circuit dédié type AD9510 (jitter 350 fs)

Cumul des jitter

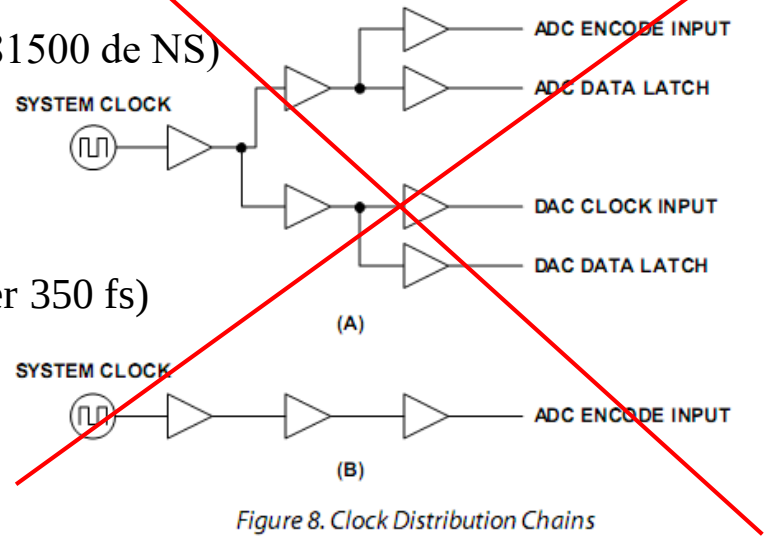


Figure 8. Clock Distribution Chains

Table 1.

Gate Type	Jitter
FPGA[1]	33 to 50 ps
74LS00	4.94 ps
74HCT00	2.20 ps
74ACT00	0.99 ps
MC100EL16 (PECL)	0.70 ps
AD9510 Clock Synthesis and Distribution	0.22 ps
NBSG16 (Reduced Swing ECL)	0.20 ps

Source: B.Brannon et A. Barlow (AD) [BRA] & J.Catt (NS) [CATT]

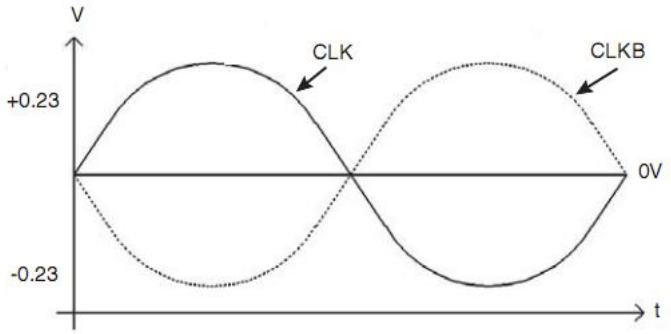
Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Mise en œuvre de l'horloge

- Exemple: ADC AT84AS008 de e2v (Atmel)
  - 10 bits – 2,2 GS/s
  - Extrait datasheet:

Typically, using a sinewave oscillator featuring –135 dBc/Hz phase noise, at 20 KHz from carrier, a global jitter value (including ADC + generator) of less than 200 fs RMS has been measured. If clock signal frequency is at fixed rates, it is recommended to narrow band filter the signal to improve jitter performance.

Figure 8-5. Differential Clock Inputs (Ground Common Mode): Recommended



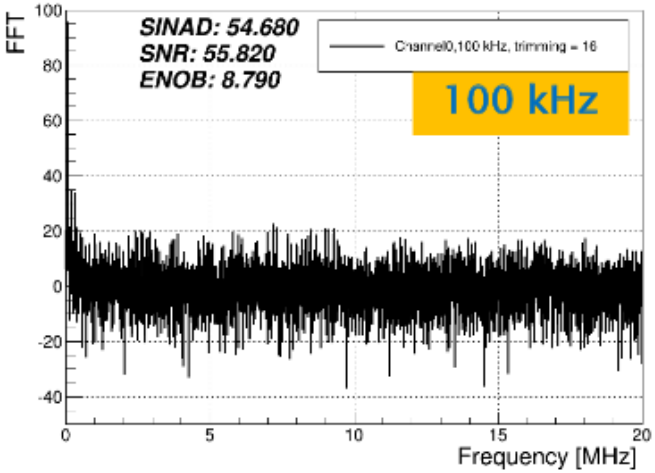
dBc: in telecommunications, this indicates the relative levels of noise or sideband peak power, compared to the carrier power.

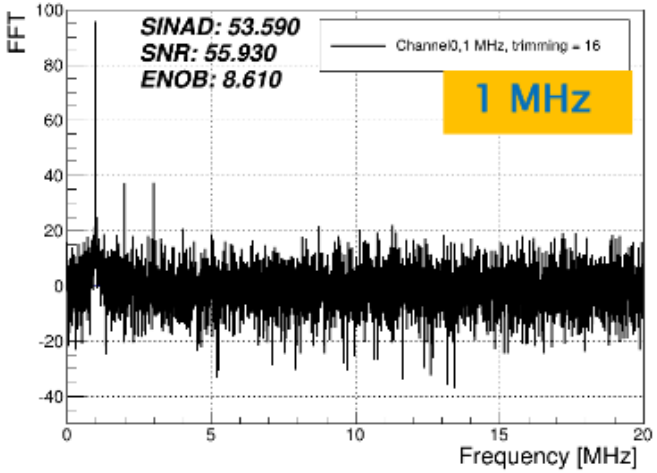
Source: e2v [AT84]

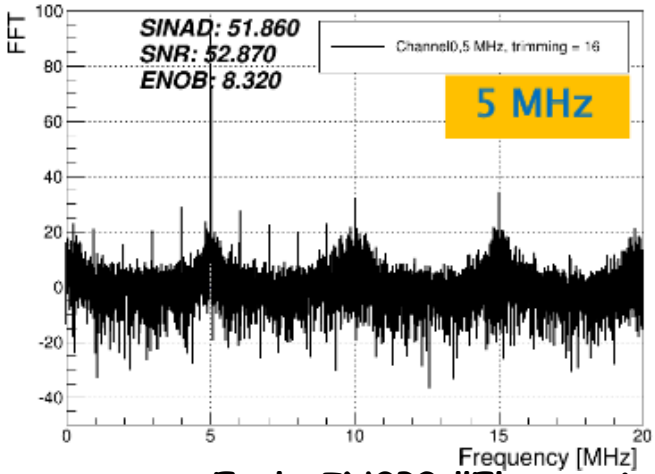
Chercher l'erreur ??

Dynamic specifications

- Dynamic performance of the ADC are determined from the FFT for an incoming sinus signal: 100KHz, 1MHz and 5MHz
- These results integrate all the limitations:
  - Reduce dynamic range
  - Spikes
  - Jitter (next slides)



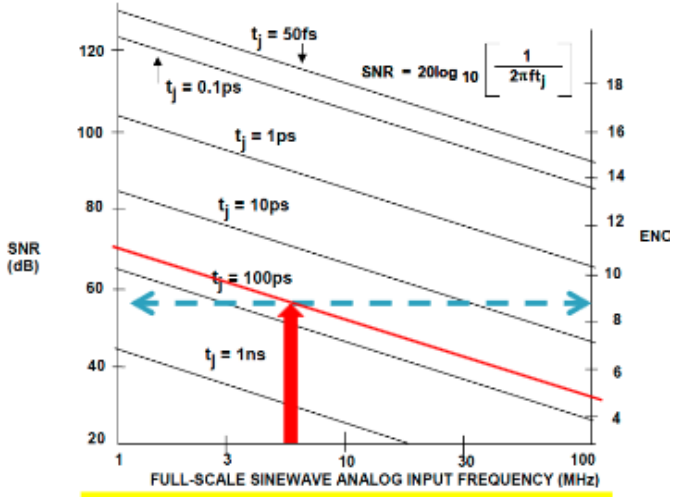




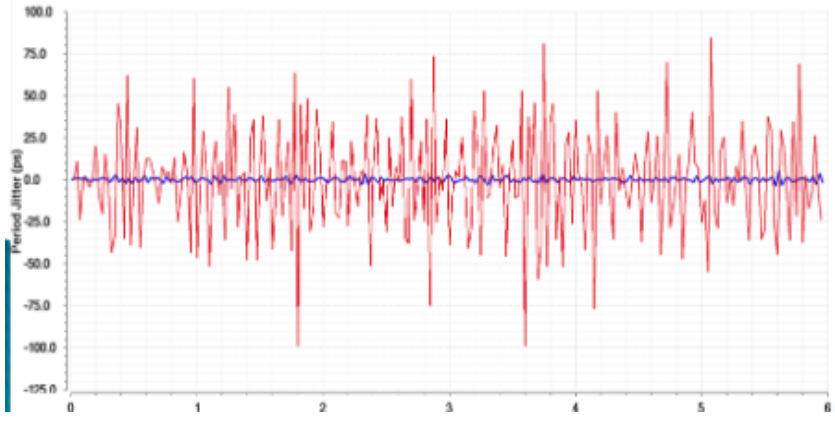
Chercher l'erreur ??

ENOB: Source & Solutions

- Source of ENOB reduction
  ➔ sampling clock jitter
  - 1 to10 ps jitter is needed to reach expectations
  - Simulation studies of 2nd prototype:
    - RMS jitter **30 ps** or ±100 ps peak to peak
- Solution:
  - Modifying the architecture of the sampling pulse generator inside the chip



Theoretical limitations as a function of jitter



Present problem for jitter
New jitter simulated

3. Utiliser un ADC:

⇨ la CEM

Quelques notions de CEM

Quelques conseils d'un experts CEM: Alain Charoy AEMC en 2005

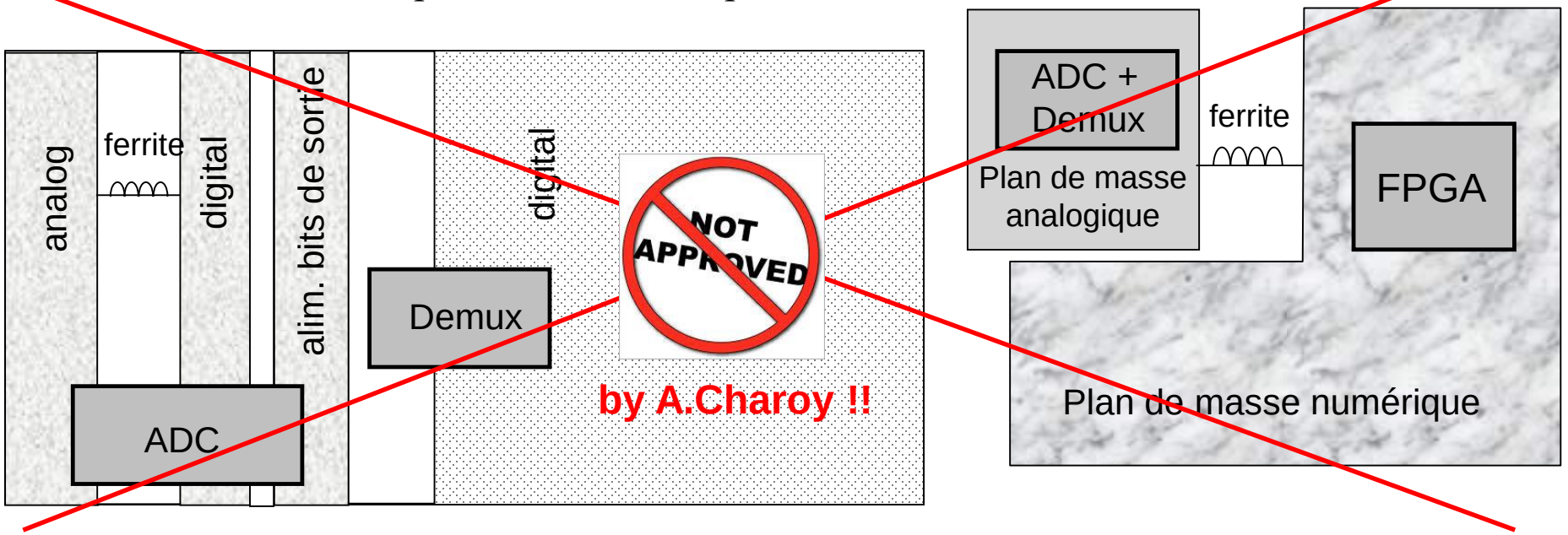
« Méfions-nous à priori des data-sheets !... »

- « Un **plan de masse** non fendu sous le convertisseur est souhaitable !
  (fente de 1cm ⇨ self ≈ 1nH) »
- « Le bruit des ADC est minimal quand AGND, DGND, REF, COM, … et capas de découplage de +Vcc et –V directement au plan 0V ! »
- « Pour permettre une conversion stable […] alimenter la partie analogique via la partie numérique. »
- « Le timing d'un convertisseur rapide est essentiel: sur un signal à 10MHz, un jitter de 10 ps génère une erreur dynamique d'une amplitude supérieure au LSB d'un ADC 12 bits. »
- « La broche d'entrée d'un échantillonneur-bloqueur injecte des charges à chaque commutation. Pour une conversion à fréquence élevée, un amplificateur rapide et stable (tel un driver vidéo par ex.) est nécessaire. »
- « Limiter les capacités des sorties numériques (ajouter des résistances série ≈ 68Ω ou un buffer « calme » pour réduire le « ground bounce »). Pour un convertisseur lent, une interface de sortie série est conseillée. »

Source: Charoix, AEMC [CHAR99] [CHAR05]

PCB pour ADC rapides

- Recommandations plan alim et masse pour l'ADC AT84AS008 de e2v

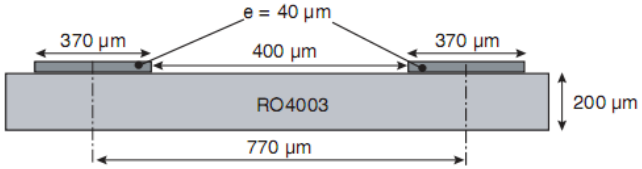


Board Layout Recommendations

It is necessary to ensure that all the lines at the input and output of the ADC are matched to within 2 mm.
As all data lines are differential, it is also necessary that each line of a differential pair is matched in length within 1 mm.

Figure 5-3 gives the layout rule used on RO4003 for differential signals.

Figure 5-3. 50Ω Matched Line on R04003 Layout (Differential Signal)



Source: App. note e2v [e2v]

Filtrage/découplage des alimentations

❑ Même soin de séparation et de découplage des alims à l'intérieur même des circuits intégrés

ADC AT84AS008

112 pins sur 148 pour alim !!

Figure 5-1. AT84AS008 Pinout of CBGA152 Package (Bottom View)

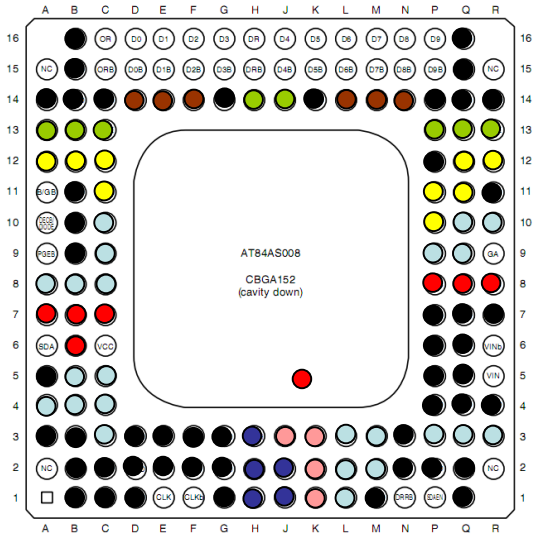
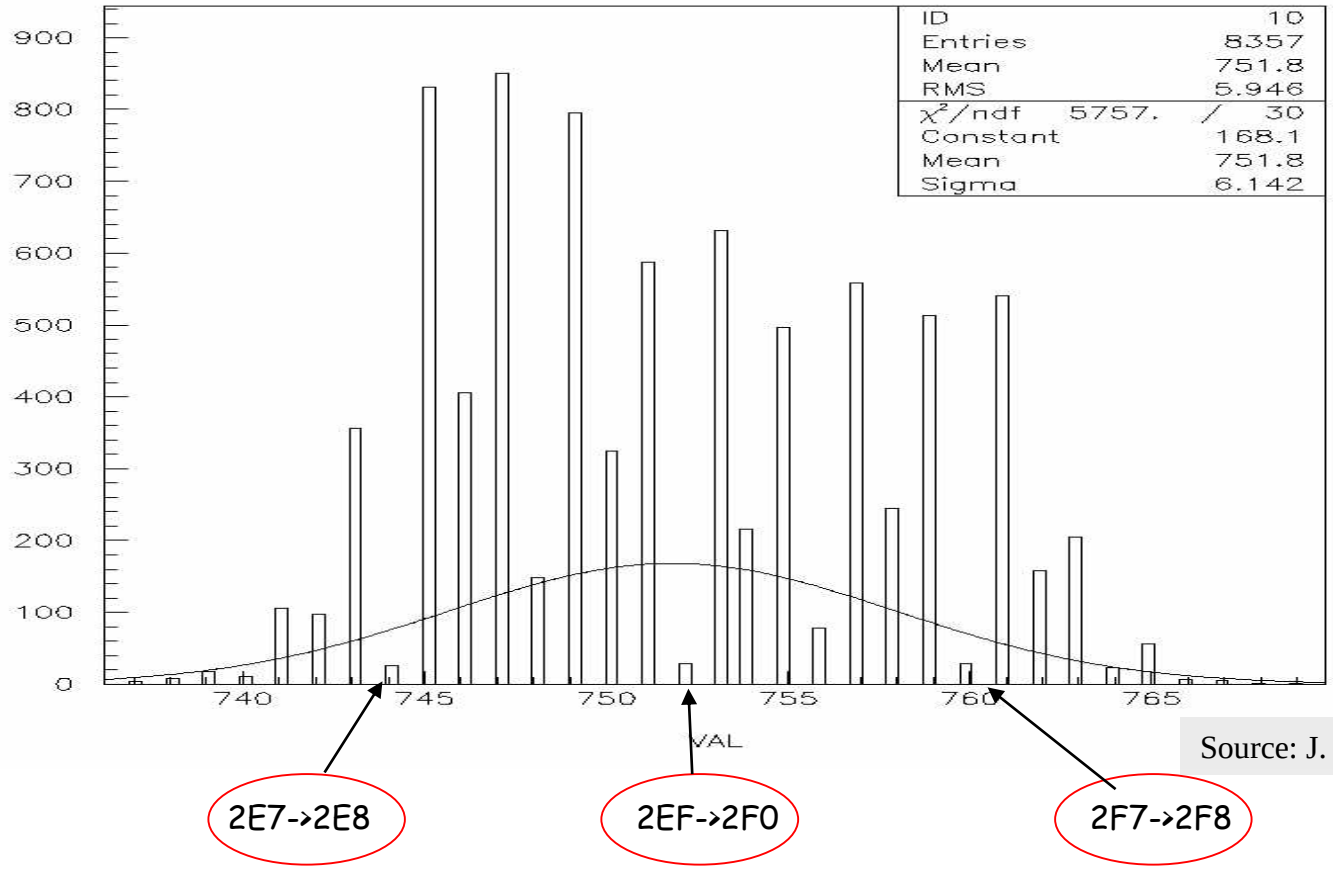


Table 5-1. AT84AS008-EB Pin Description

Symbol	Pin Number	Function
Power Supplies		
V_{CC}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	+5V analog supply
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analog ground
V_{EE}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	-5V analog supply
V_{PLUSD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
DV_{EE}	A13, B13, C13, P13, Q13, R13, H14, J14	-5V or -2.2V digital supply

Gestion des alimentations: le mauvais exemple

- ASIC: ADC à rampe
- Alim. analogique et numérique communes dans la puce
  - di/dt alim numérique ➔ dv/dt alim. analogique ➔ Codes de sorties erronés lors du changement d'états simultanés de plusieurs bits
  - Intérêt du compteur Gray (un seul changement d'état à la fois)

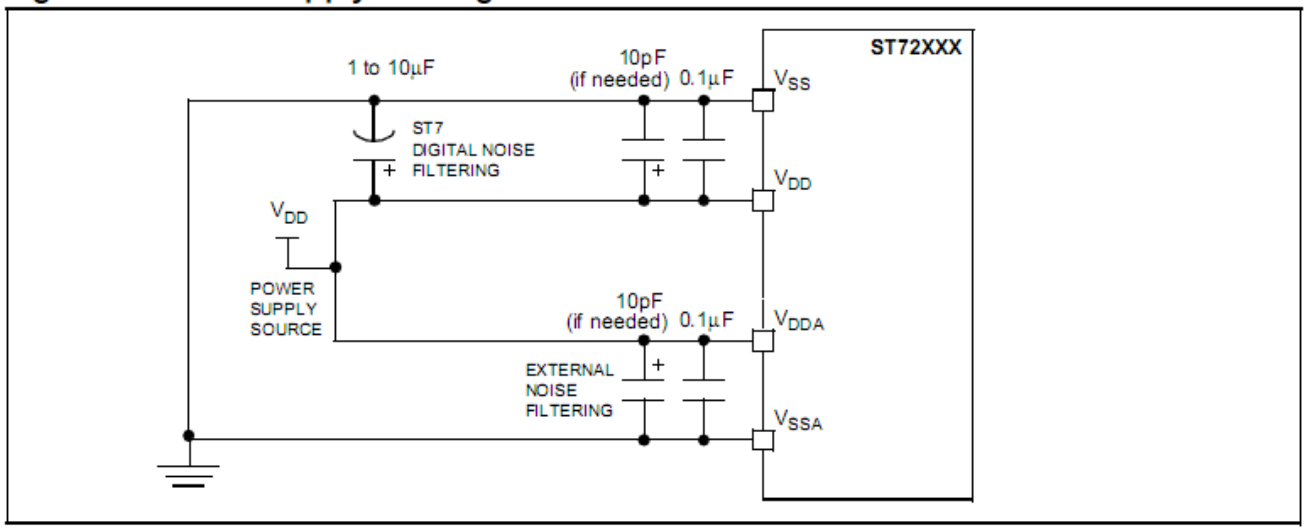


Source: J. LECOQ - LPC [LEC]

Filtrage/découplage des alimentations: rappels

- Exemple recommandations de ST Micro.

Figure 14. Power supply filtering



The capacitors allow the AC signals to pass through them. The small value capacitors filter high frequency noise and the high value capacitors filter low frequency noise. Ceramic capacitors are generally available in small values (1pf to 0.1 µf) and small voltages 16V to 50V. It is recommended to place the ceramic capacitors close to the main supply pins (V_{DD} & V_{SS} and analog supply pins (V_{DDA} & V_{SSA}). These filter the noise induced in the PCB tracks. Small capacitors can react fast to current surges and discharge quickly for fast current requirements. Tantalum capacitors can also be used along with ceramic capacitors.

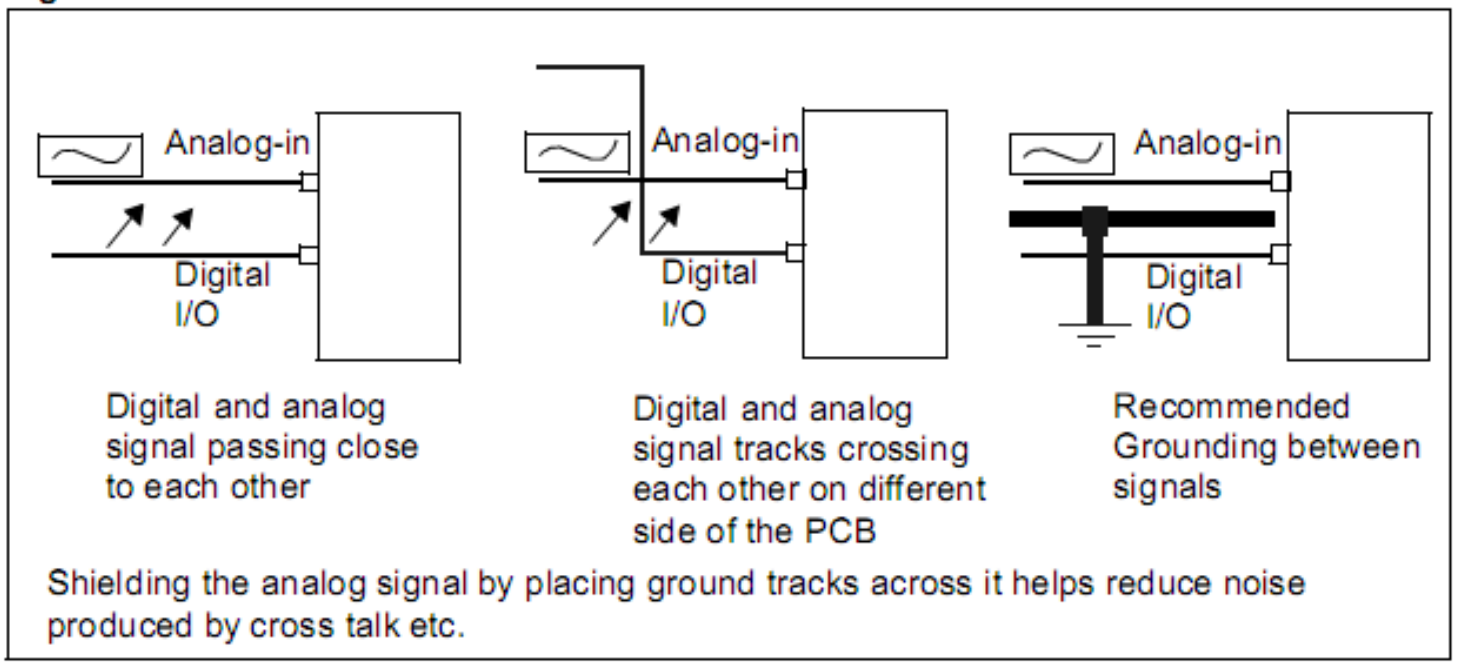
High value capacitors (10µf to 100µf) which are generally electrolytic, you can use them to filter low frequency noise. It is recommended to put them near the power source. You can also filter high frequency noise using a ferrite inductance in series with the power supply. Ferrites cause low DC loss (negligible) unless the current is high. This is because the series resistance of the wire is very low. But for high frequency, the impedance offered is high.

Source: App. note ST [AN1636]

Rappel: séparation des signaux analogiques et numériques

Analogique et numérique: une cohabitation difficile

Figure 22. Cross-talk between I/Os



Source: App. note ST [AN1636]

3. Utiliser un ADC:

⇨ l'impédance d'entrée

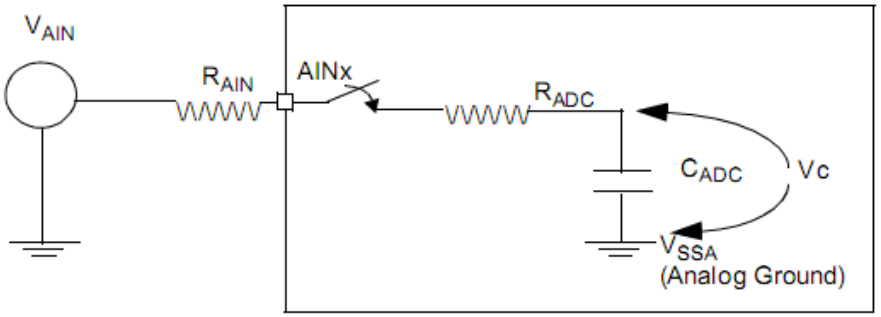
Temps de charge de la capa C_{ADC}

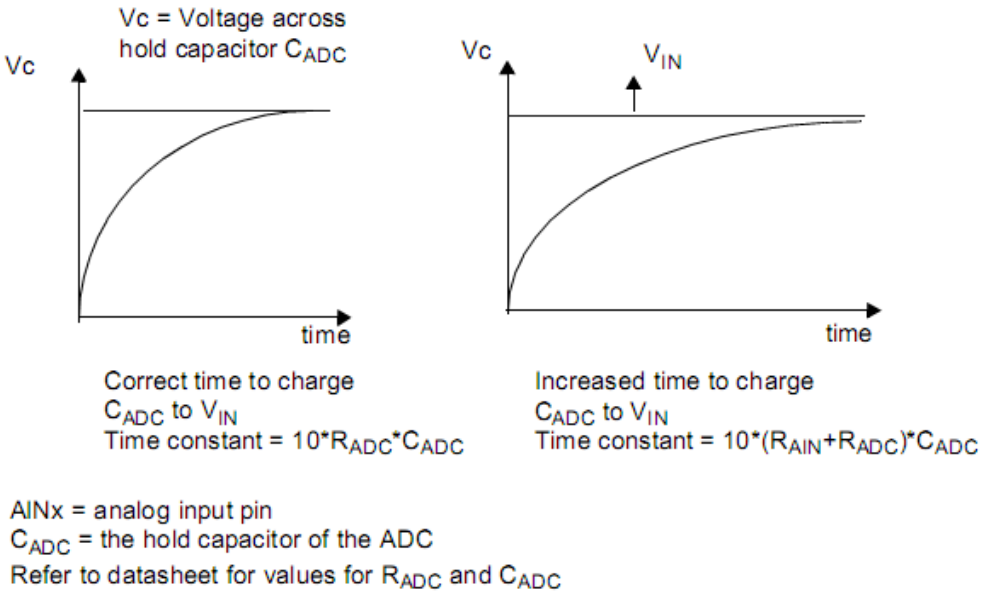
- L'impédance de sortie de la source se rajoute à l'impédance d'entrée de l'ADC:

$$\tau = (R_{ADC} + R_{AIN}) * C_{ADC}$$

- Grande R_{AIN} affecte THD

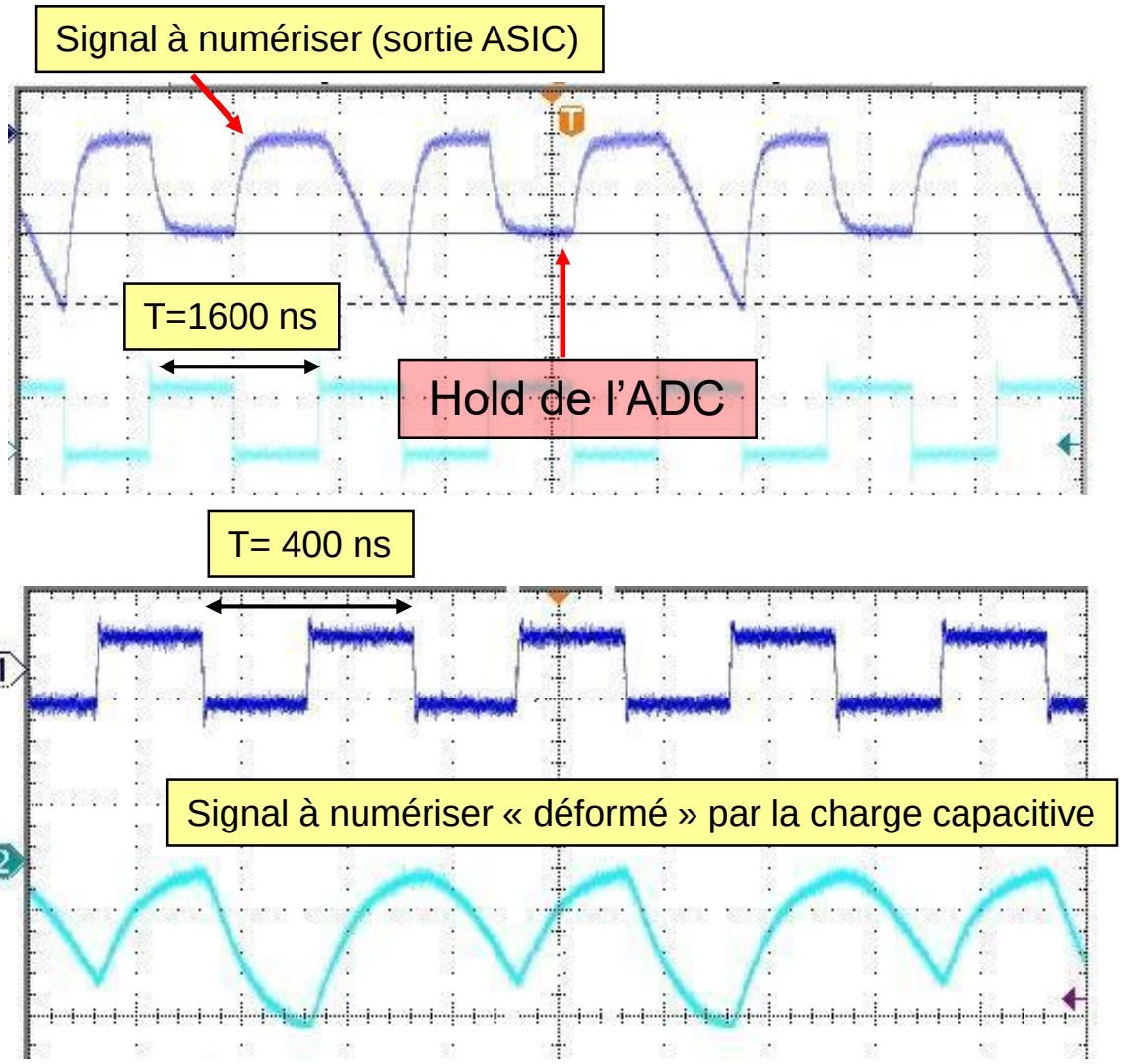
- Ex: AD7684 16 bits
  - Précision1 LSB/16 bits: 1/65536
    → précision atteinte à 11 τ
  - R_{ADC} = 600 Ω, C_{ADC} = 30 pF
  - 11 x τ = 200 ns





Source: App. note ST [AN1636]

Exemple de driver mal adapté



- Utilisation de l'ADC AD7684 pour numériser un signal délivré par un ASIC (mémoire analogique Made in LPC Clermont)
- Un driver interne à l'ASIC
- Pas de driver externe
- A la période nominale T= 400ns le signal n'a pas le temps de s'établir

Source: F.Collange (LPC Clermont)

3. Utiliser un ADC:

⇨ Les références de tension

Les références de tension

Voltage-reference impact on total harmonic distortion

Texas Instruments

Jose A. Duenas
Applications Engineer
Precision Analog
Texas Instruments

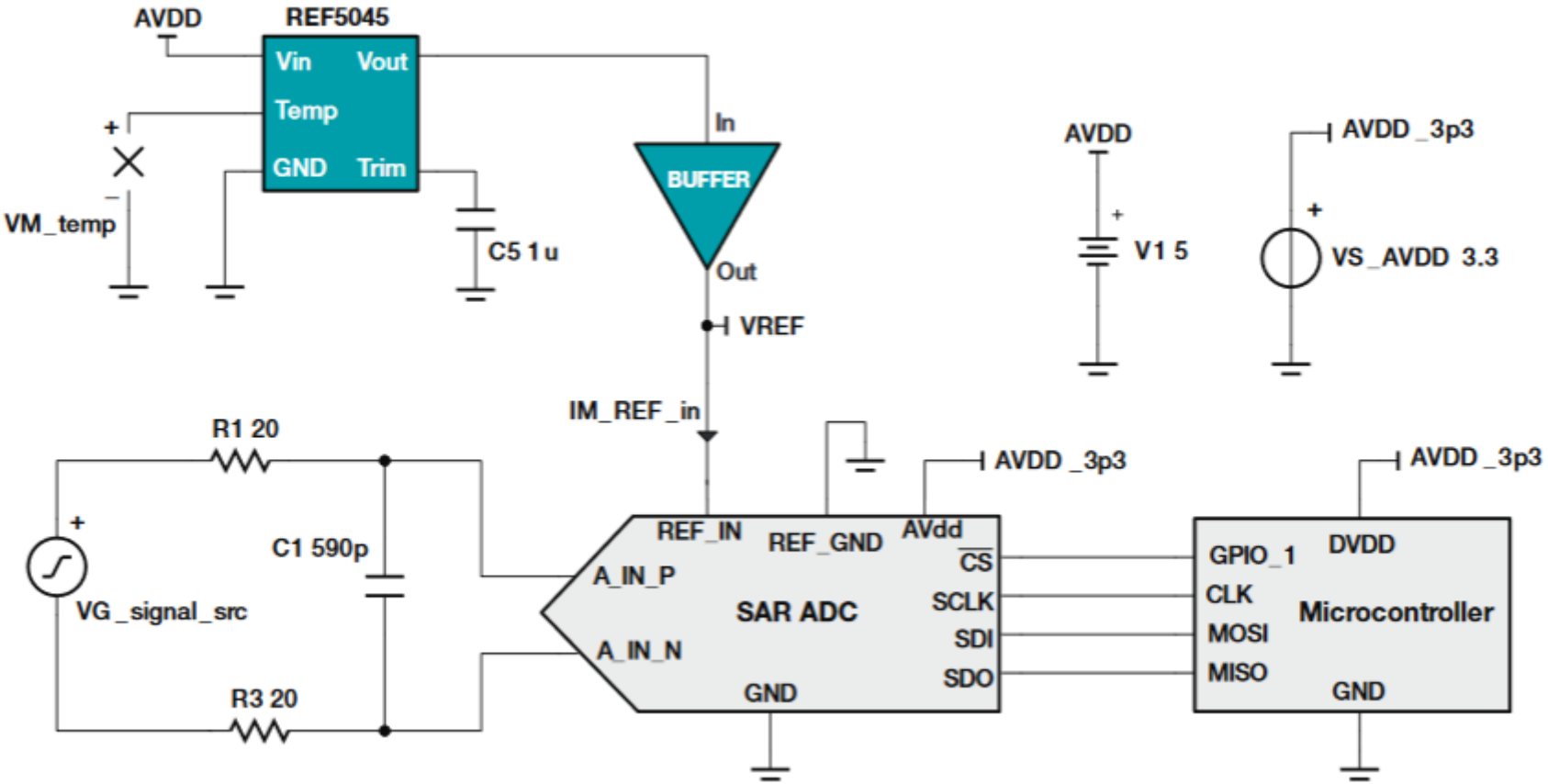
Understanding the load presented by the reference pin of SAR ADCs is key when designing data-acquisition systems with low harmonic distortion.

The internal circuitry connected to the reference pin of most successive-approximation-register analog-to-digital converters (SAR ADCs) (and some wideband delta-sigma ADCs) consists of switched-capacitor loads. During the conversion process, a switched-capacitor load imposes a current demand that can cause the external system's reference-output voltage to fluctuate in time. Consequently, the SAR ADC reference-pin voltage also fluctuates.

http://www.ti.com/lit/wp/slyy097/slyy097.pdf

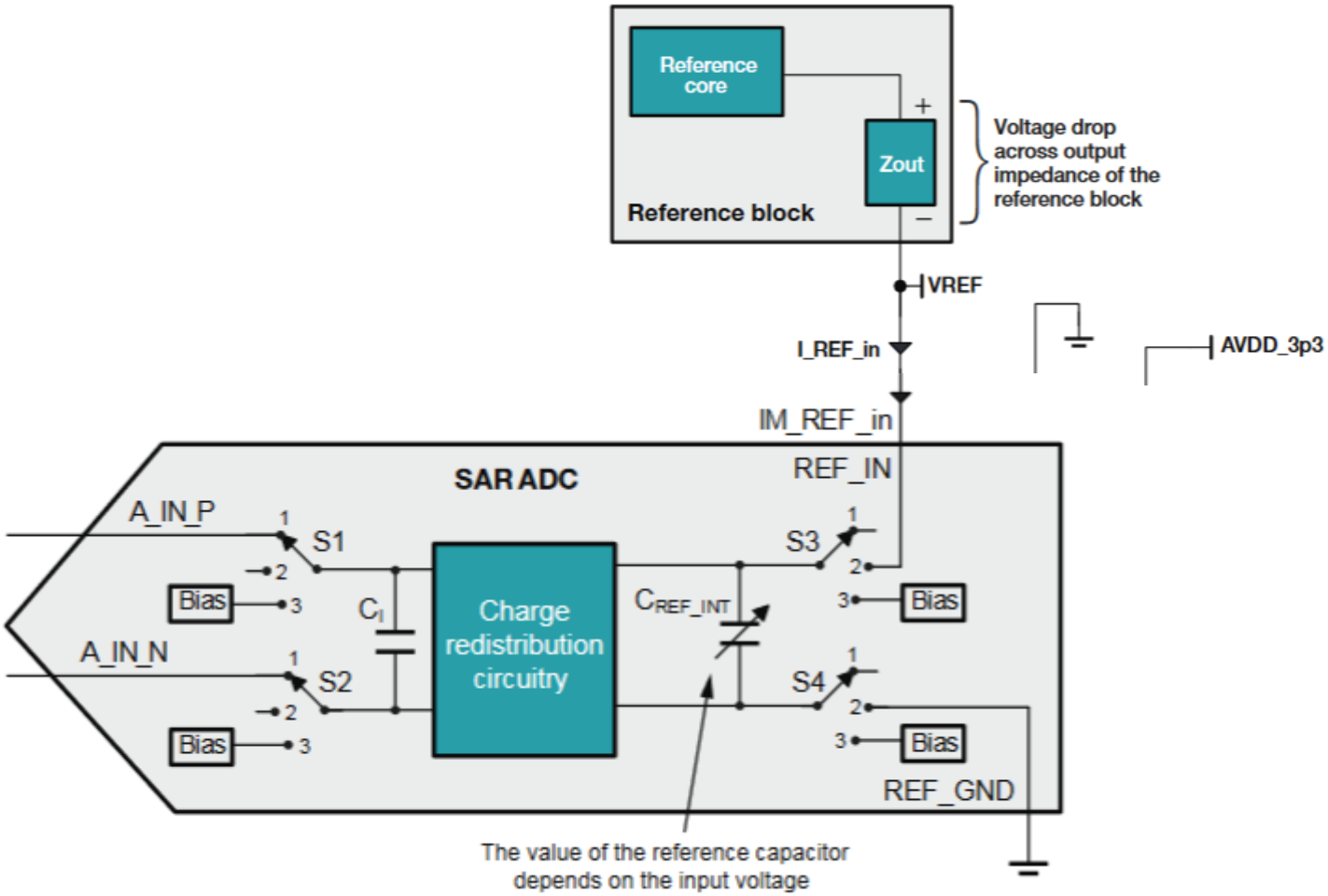
Les références de tension

Exemple de mise en œuvre d'un ADC SAR:



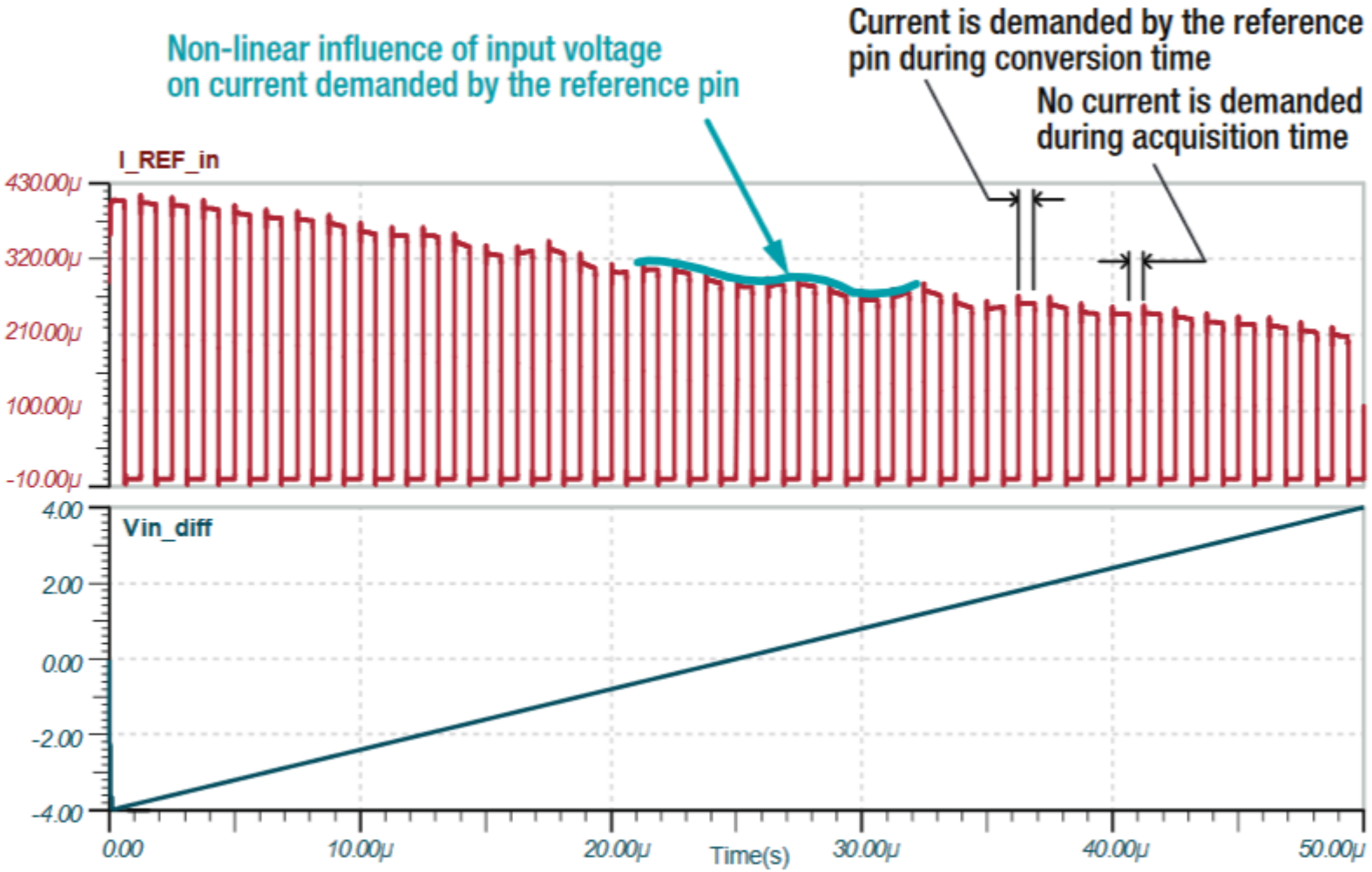
Les références de tension

- Commutation des interrupteurs S3&S4 → courants ΔI_REF_in
- Zout du bloc de référence ≠ 0 → ΔVREF



Les références de tension

- Simulation d'un modèle SPICE



Les références de tension

- Résultats sans buffer sur la référence

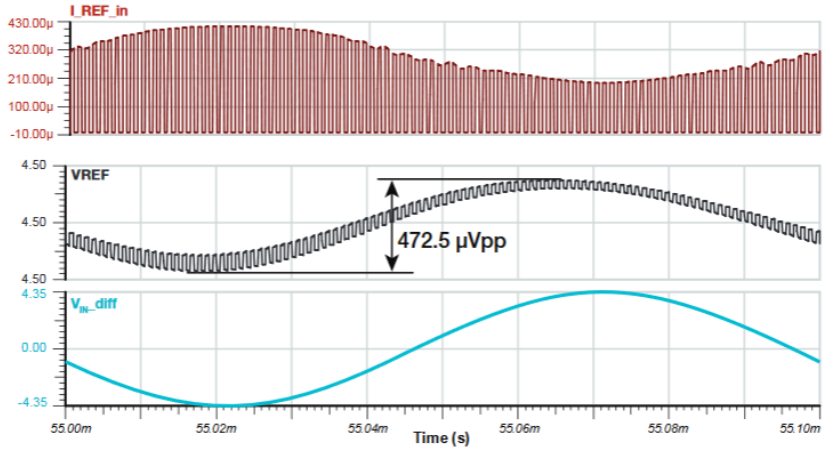
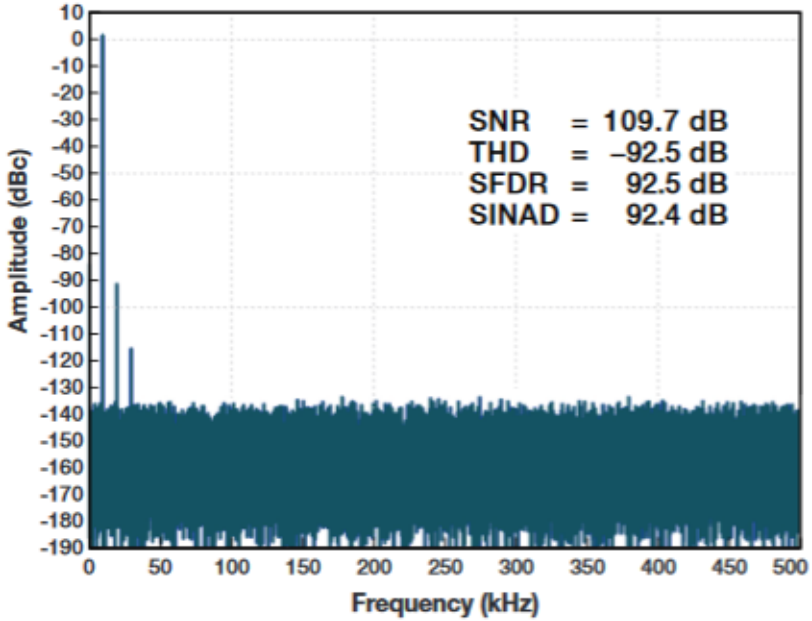


Figure 10. Simulation results for a system without a reference buffer.



→ ENOB=15 bits

Les références de tension

- Mise en œuvre d'un buffer

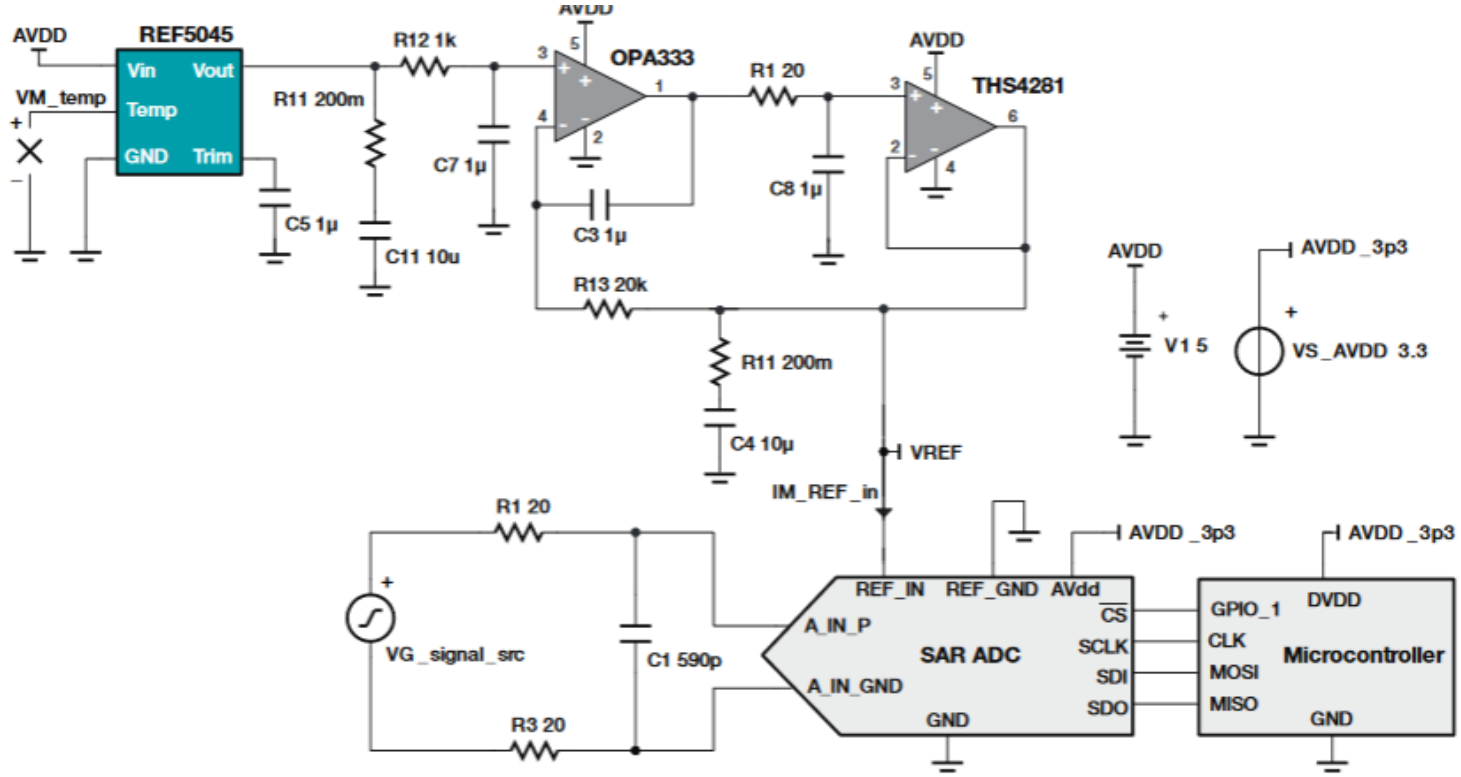


Figure 12. Schematic of a data-acquisition system with a reference buffer.

Les références de tension

Sans buffer

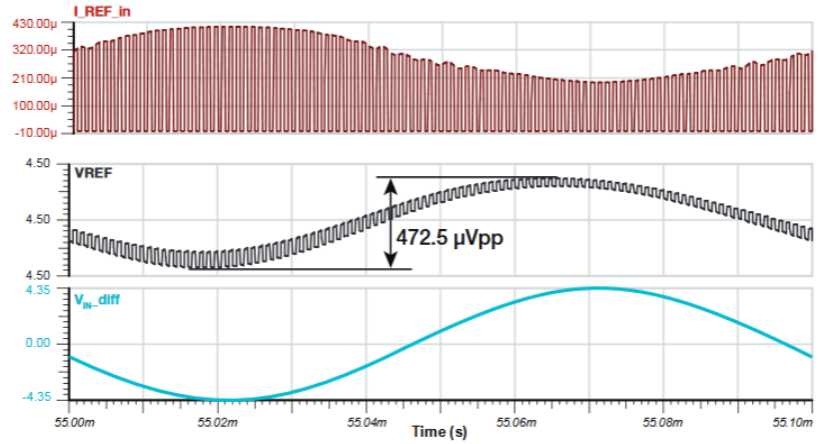


Figure 10. Simulation results for a system without a reference buffer.

Avec buffer

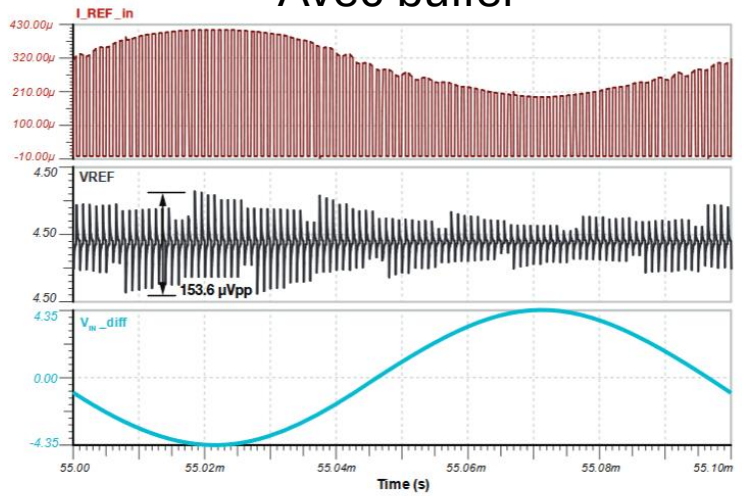
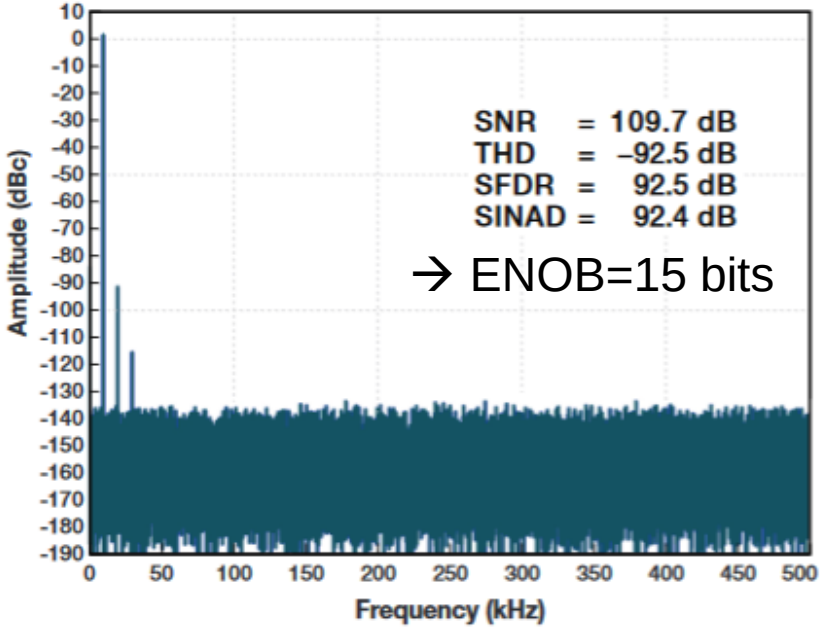
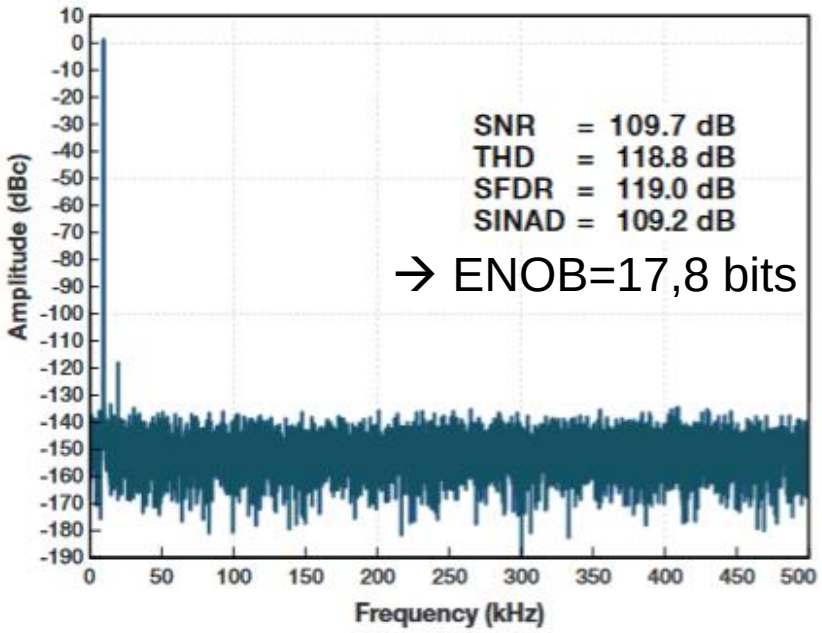


Figure 13. Simulation results for a system with a reference buffer.





Les références de tension

- Utilisation du circuit de référence REF6045

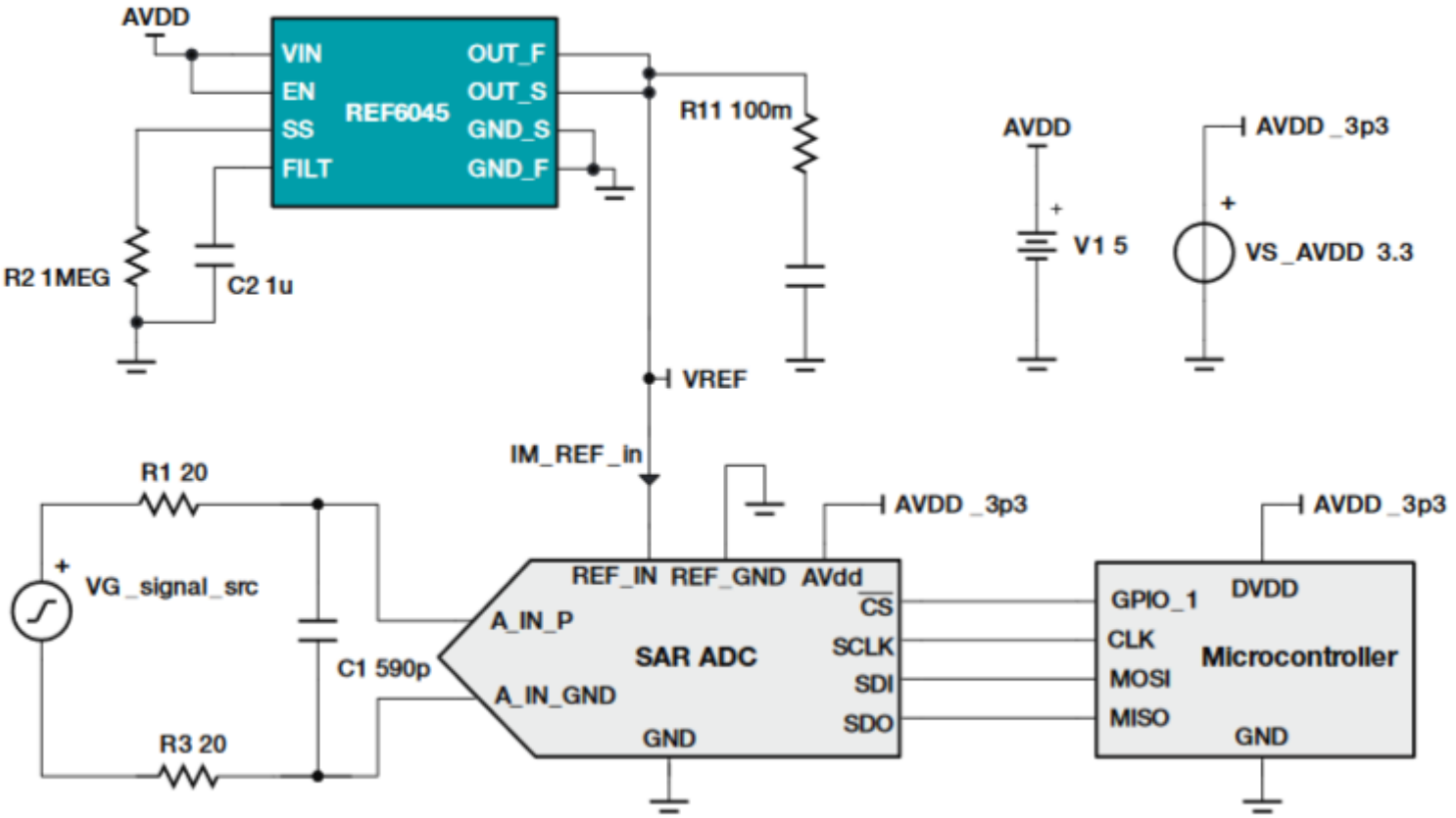


Figure 15. Schematic of a data-acquisition system with the REF6045.

Les références de tension

Avec buffer

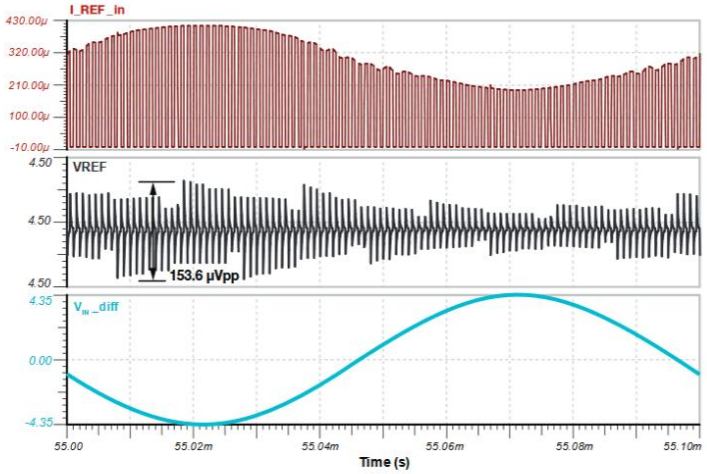
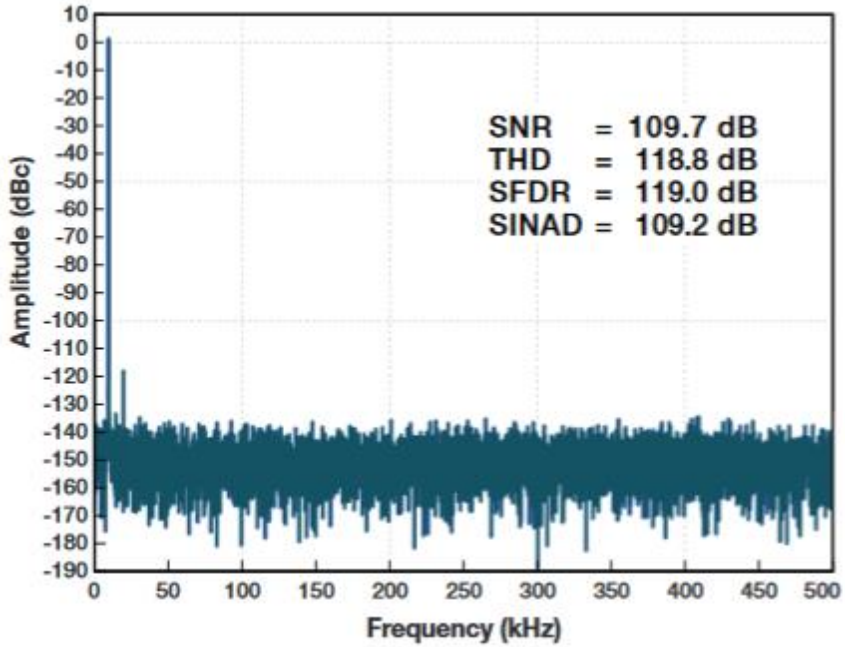


Figure 13. Simulation results for a system with a reference buffer.



Avec REF6045

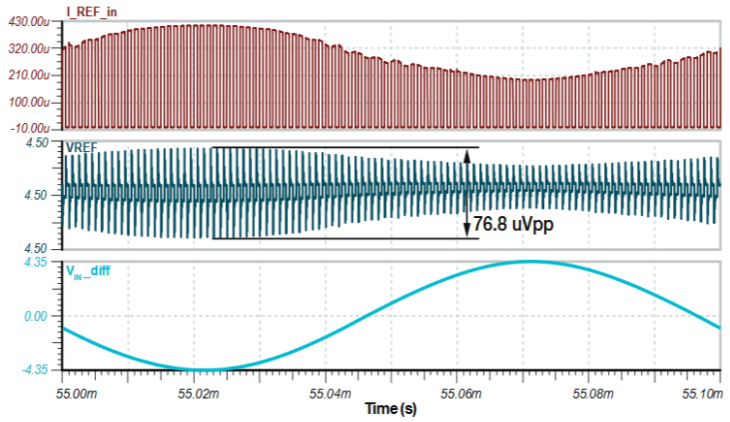


Figure 16. Simulation results for a system with the REF6045.

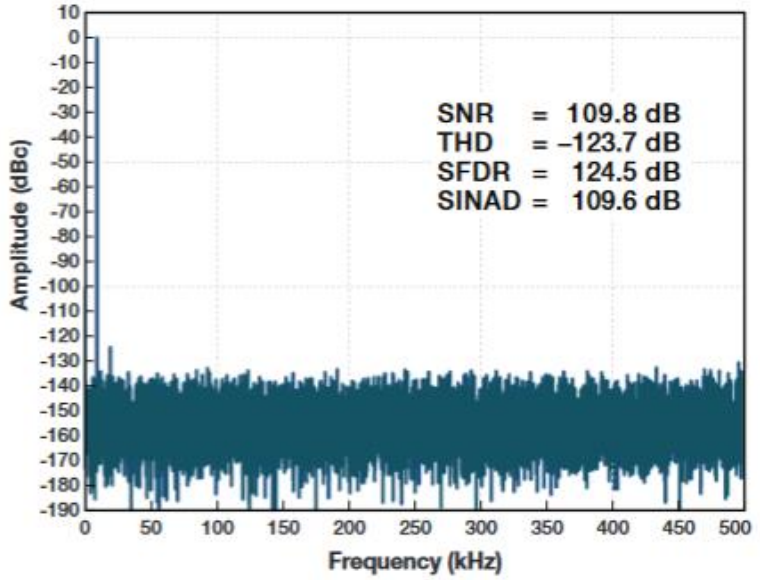
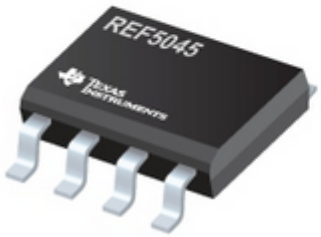


***Figure 17.** Key AC performance metrics and FFT for a system with the REF6045.*

Les références de tension

REF5045 (ACTIVE)

Low Noise, Very Low Drift, Precision Series Voltage Reference



DATASHEET

REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference datasheet (Rev. H)

View now Download

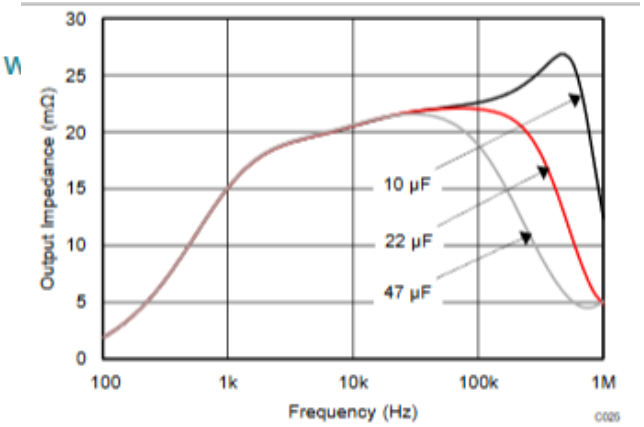
REF6045 (ACTIVE)

5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer

DATASHEET

REF60xx High-Precision Voltage Reference W

View now Download

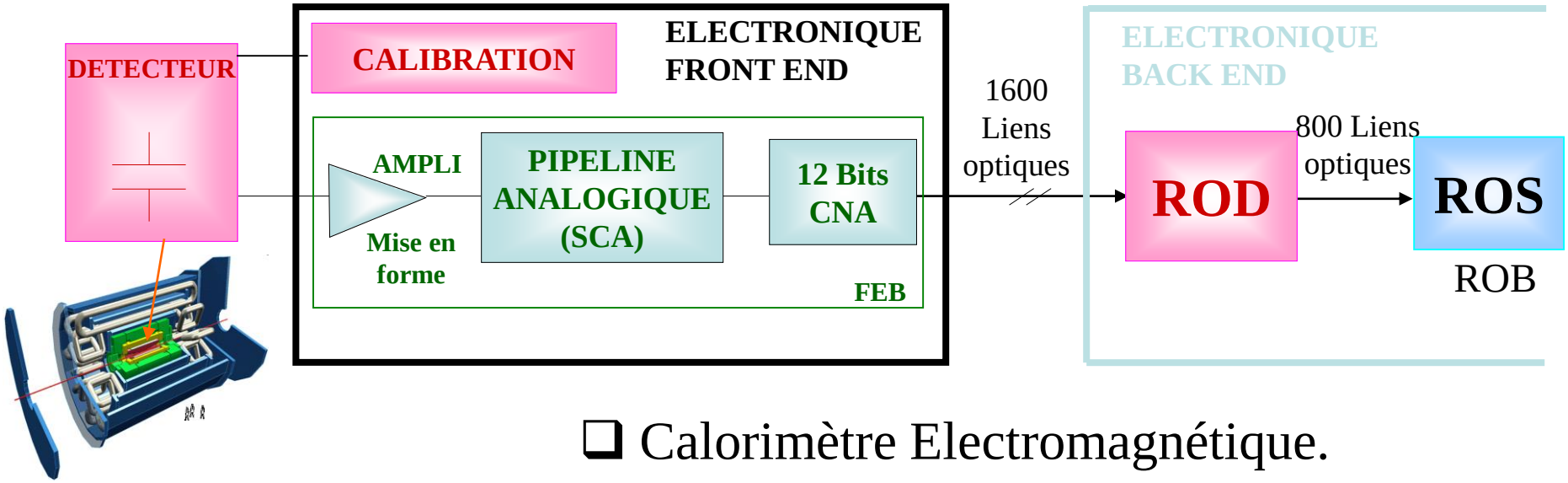


Graph obtained by design simulation

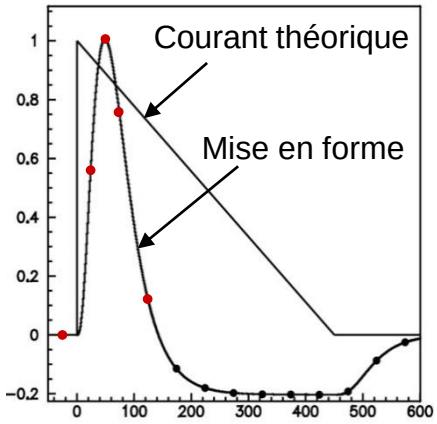
Figure 16. Output Impedance vs Frequency

4. Quelques exemples d'utilisation d'ADC @ IN2P3

FEE du calorimètre électromagnétique d'Atlas



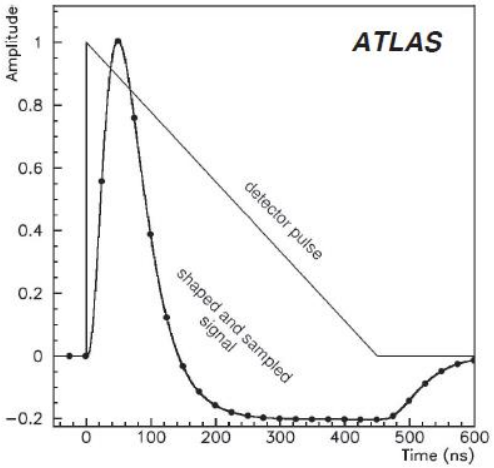
- Calorimètre Electromagnétique.
  - 200.000 Cellules
  - 1600 Modules FEB
  - 200 Modules ROD
  - 120 Modules de Calibration



Source: G.Perrot - LAPP[PER]

FEE du calorimètre électromagnétique d'Atlas

- Cartes Front-End du calorimètre à argon liquide d'Atlas (FEB)
  - ≈ 200 000 voies → 128 voies par cartes
  - dimensions: 400x500 mm^2 !!
  - 1629 cartes produites
  - Utilisation d'un ADC AD9042 par voie
  - Mesures, sous irradiation, de la dérive de:
    - ✓ la consommation en courant
    - ✓ la précision
    - ✓ du temps de conversion
    - ✓ la référence de tension interne



Source: [Atlas_Lar]

Carte FEB 128 voies

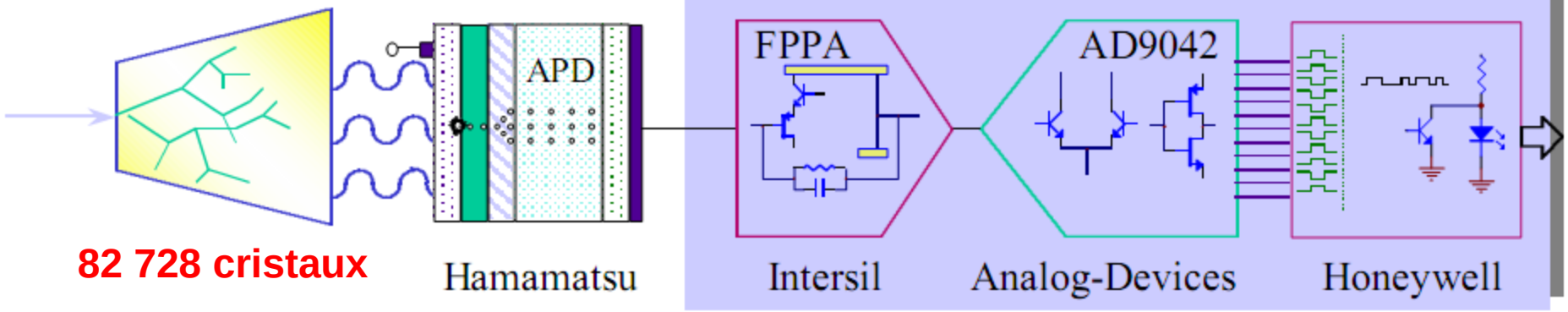
Source: T.Liu et al. [SMU]

Figure 25. The amplitude vs. time for the triangular pulse shape from the LAr calorimeter, overlaid with the bipolar-shaped and sampled pulse shape.

CMS

ELECTROMAGNETIC CALORIMETER

FRONT-END ELECTRONIC CHAIN



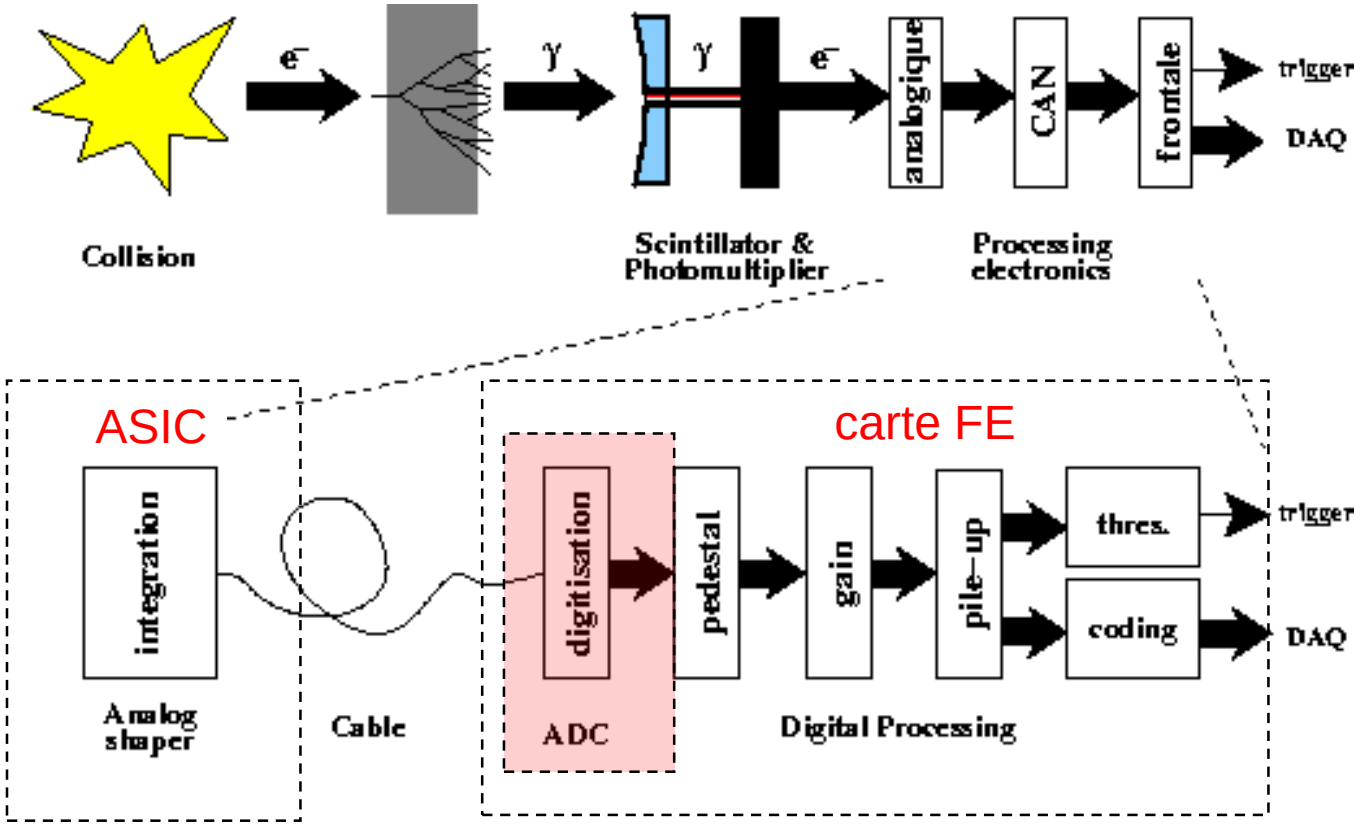
Full custom Ctrl Chip (not shown)	Type of IC	Full custom ASIC	Commercial ADC	Full custom ASIC
DMILL	Process	UHF1X	XFCB	CHFET

RAD HARD ELECTRONICS, Power dissipation: 1,2 W/channel

10^4 Gy = 1 Mrad

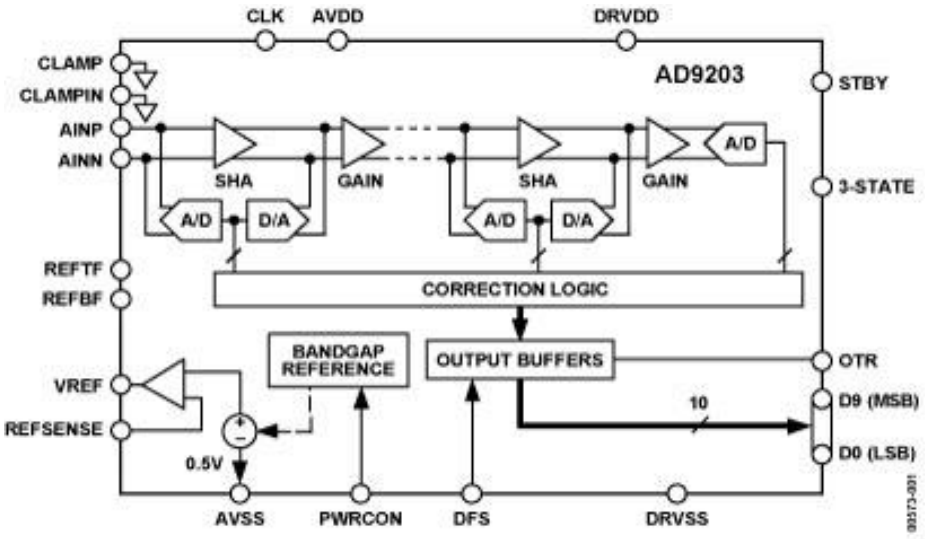
Source: P.Denes [CMS1] & P.Depasse [CMS2]

FEE du preshower de LHCb (LPC Clermont)



Source: R. CORNAT - LPC - LECC Colmar - septembre 2002

- ADC AD9203 (Analog Devices):
  - Architecture: pipeline, différentiel
  - Resolution: 10 bits sur 1V différentiel
  - Sampling rate: 40 MS/s
  - Consommation:74mW/3V



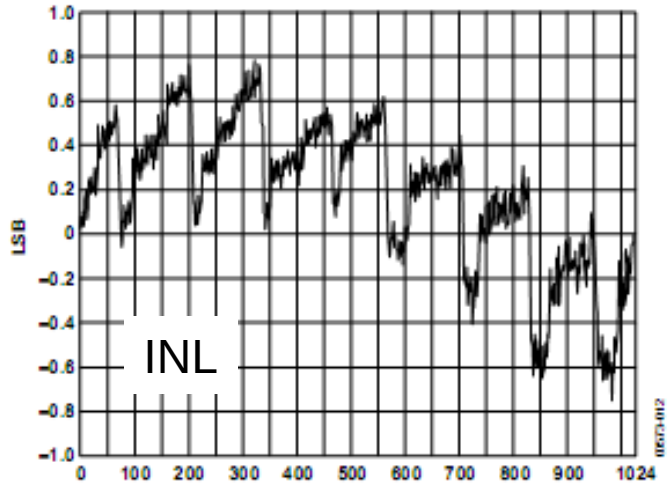


Figure 12. Typical INL Performance

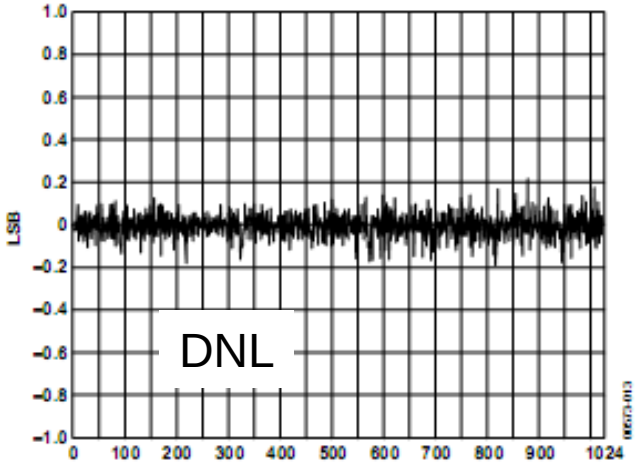
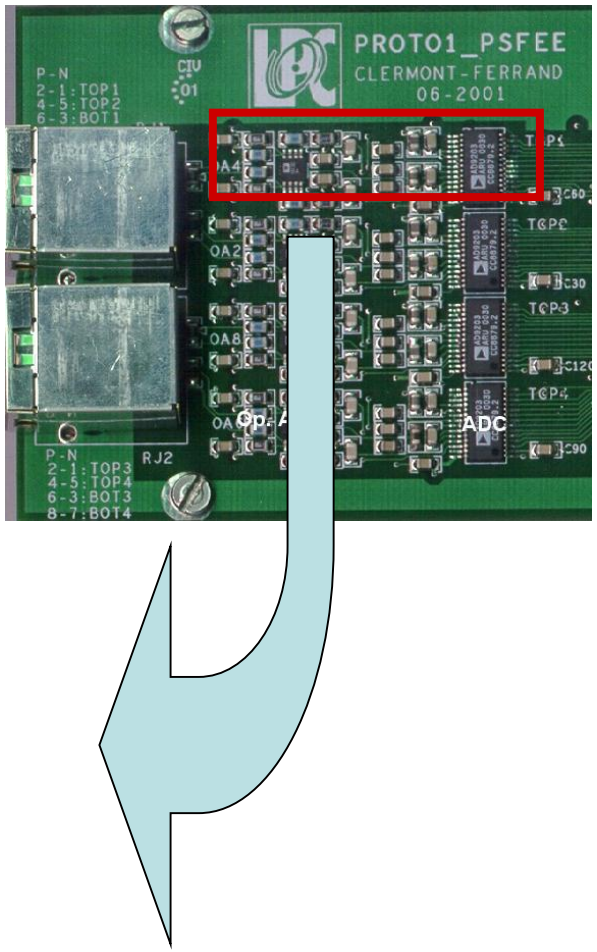


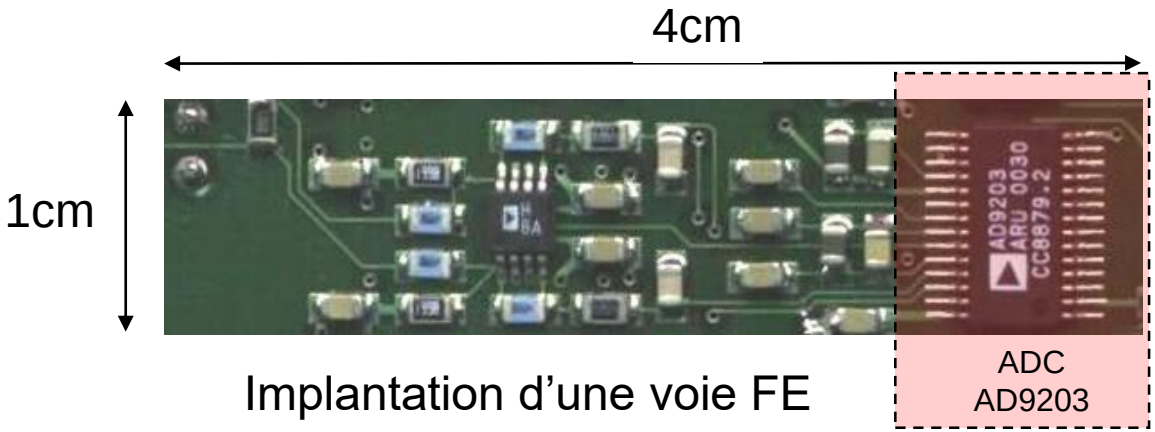
Figure 13. Typical DNL Performance

Source: Analog Devices

FEE du preshower de LHCb (LPC Clermont)

- 64 voies par carte format 9U
  - Surface max. d'une voie: 1 cm x 4 cm
- Bruit <1 LSB (1mV) grâce:
  - Plan de masse
  - Signaux analogiques différentiels
  - Horloge différentielle LVDS
  - Routage précautionneux des pistes sensibles





Implantation d'une voie FE

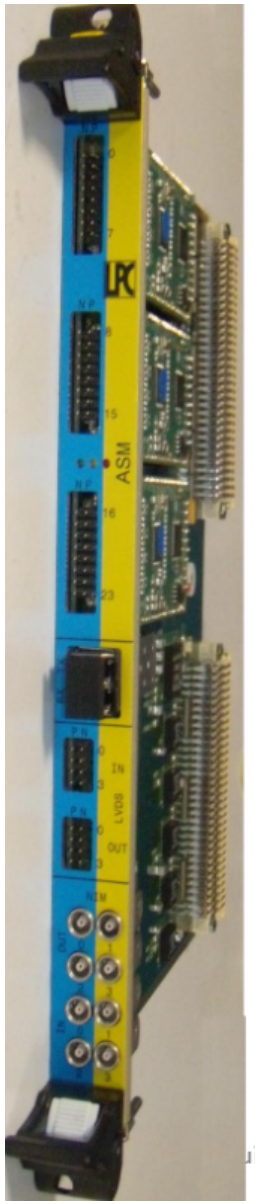
Source: R. CORNAT - LPC - LECC Colmar - septembre 2002

Aperçu @ IN2P3

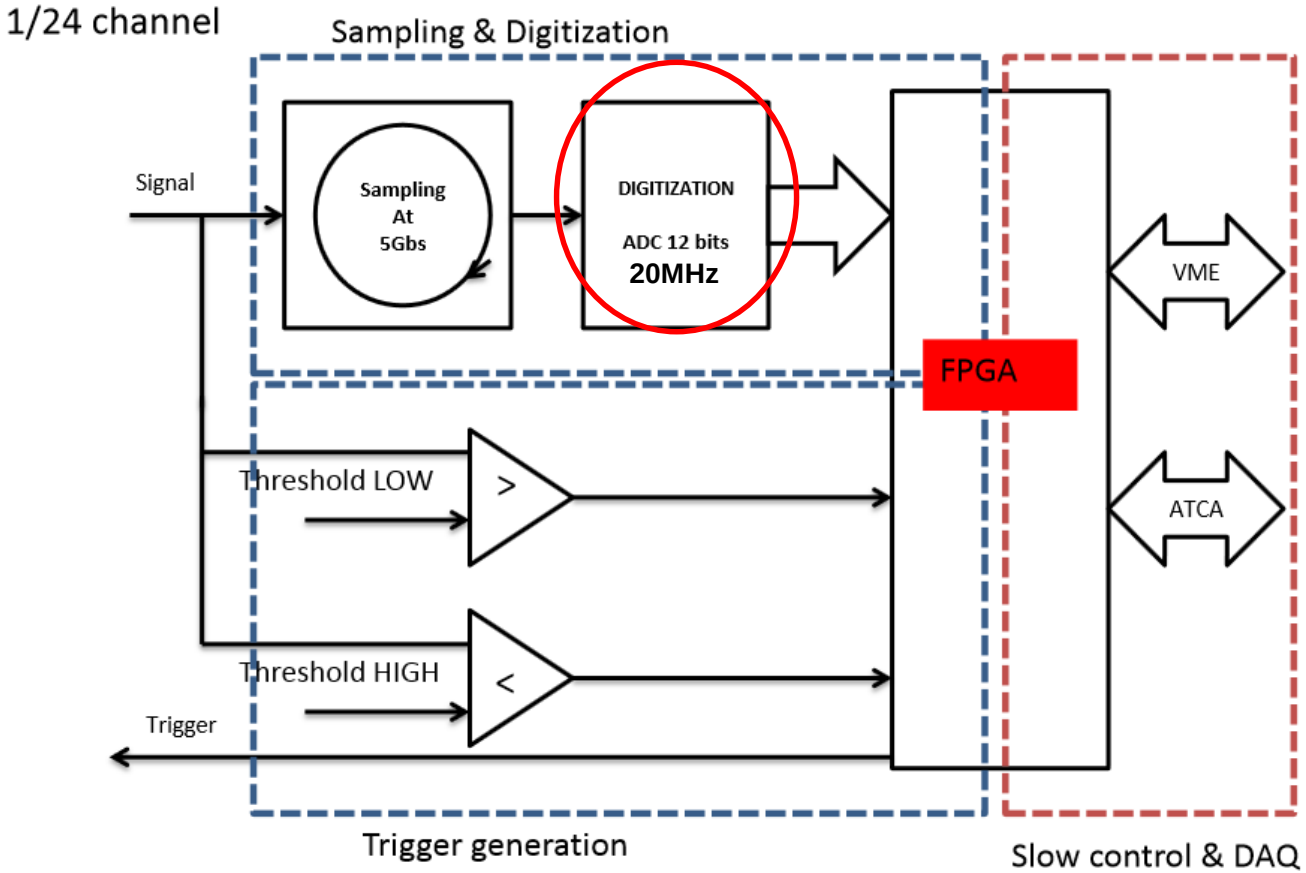
Journées VLSI - FPGA - PCB de l'IN2P3 2014
à CPP Marseille

https://indico.in2p3.fr/conferenceOtherViews.py?view=standard&confId=9825

Carte d'échantillonnage pour une application TEP en hadronthérapie



Board functional diagram



The USB_WaveCatcher board (V6)

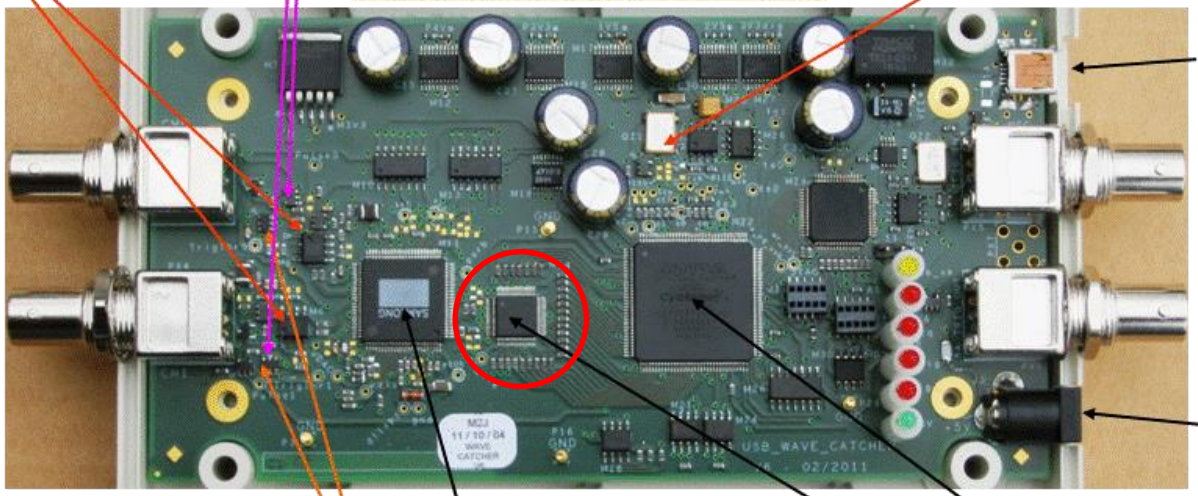
Pulsers for reflectometry applications

1.5 GHz BW amplifier.

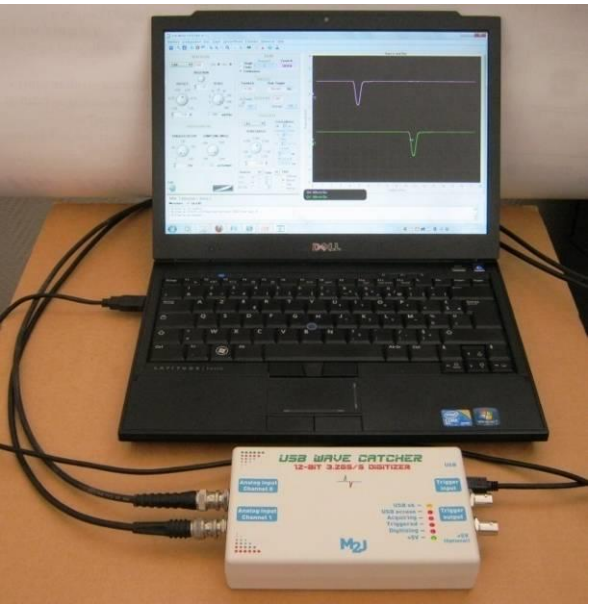
Board has to be powered by USB => power consumption ≤ 2.5W

Reference clock: 200MHz => **3.2GS/s**

2008/2010



The autonomous test bench



The historical 2-Channel module

Système d'acquisition pour caractérisation d'un imageur à multiplication électronique intra-pixel emCMOS

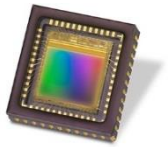
Remi Barbier, Timothée Brugière, David Chaize, Sylvain Ferriol, Cyrille Guérin, William Tromeur, Lionel Vagneron

Projet dans le cadre d'une collaboration E2V / IPNL

E2V

http://www.e2v.com

- Développement de matrices de nouveaux pixels avec multiplication électronique intra-pixel (emCMOS)

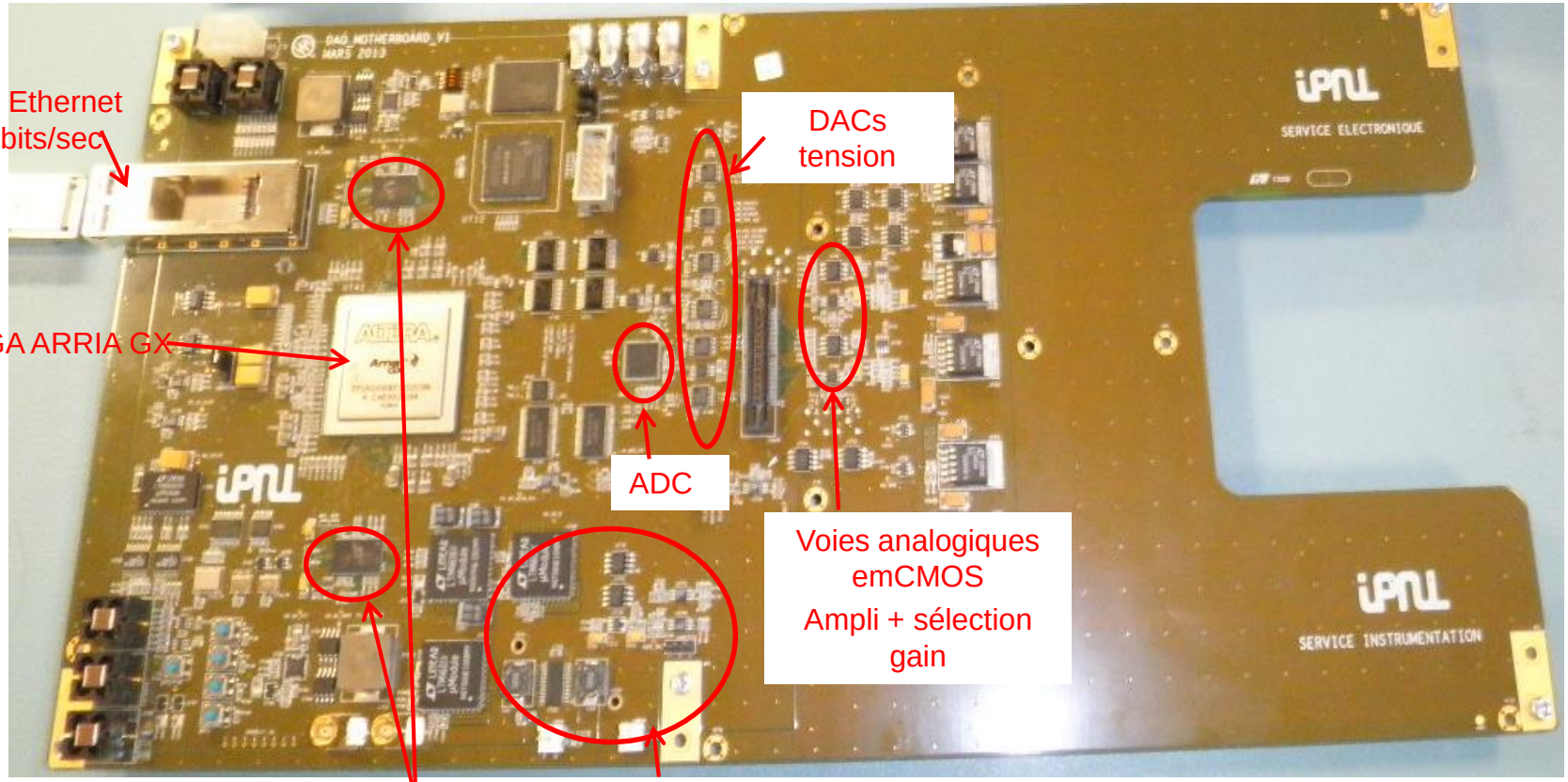


IPNL

- Conception du système d'acquisition
- Validation et caractérisation du système
- Caractérisation des matrices de nouveaux pixels sur banc optique

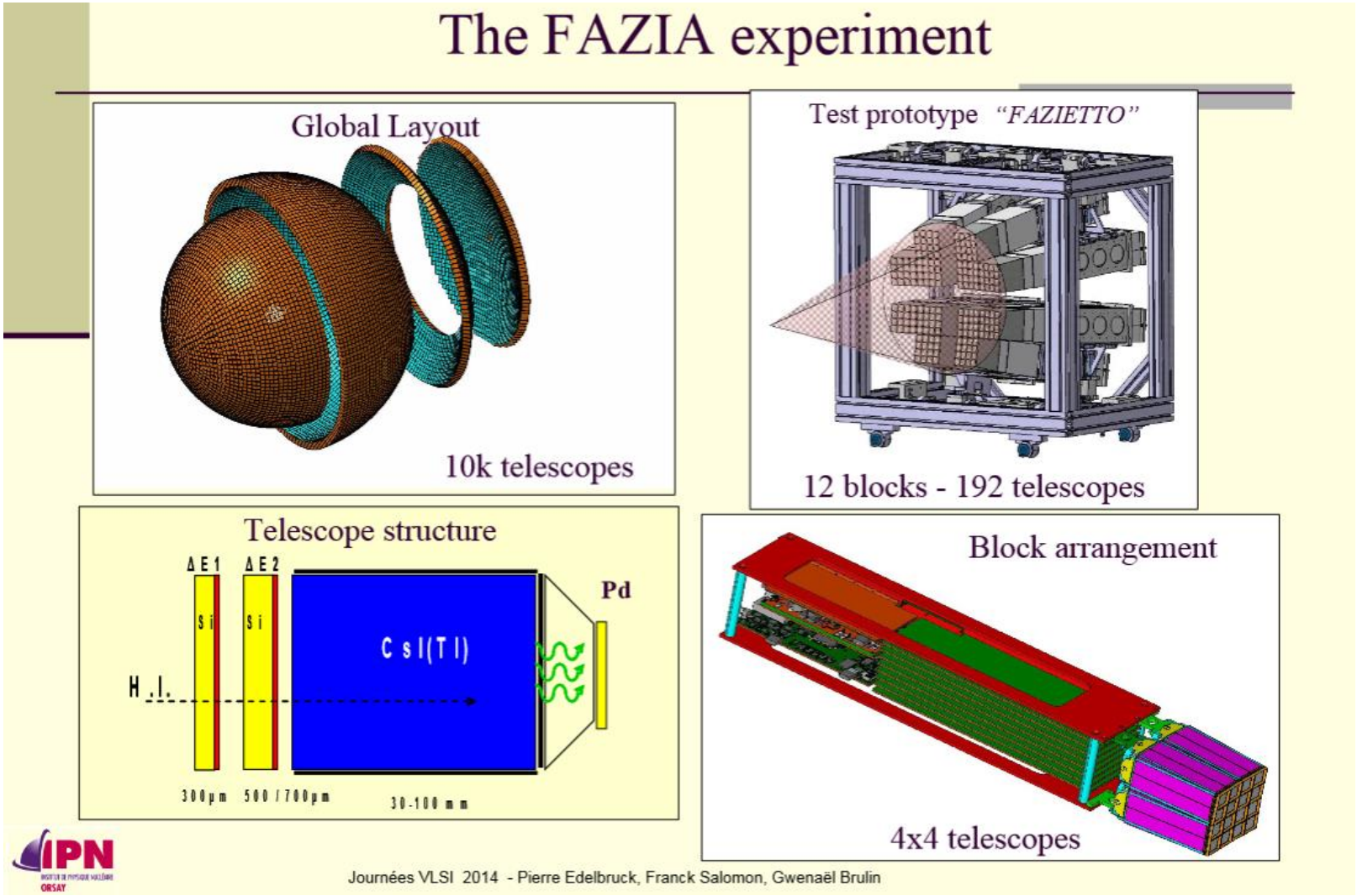
5. Présentation des cartes

➢ Carte mère

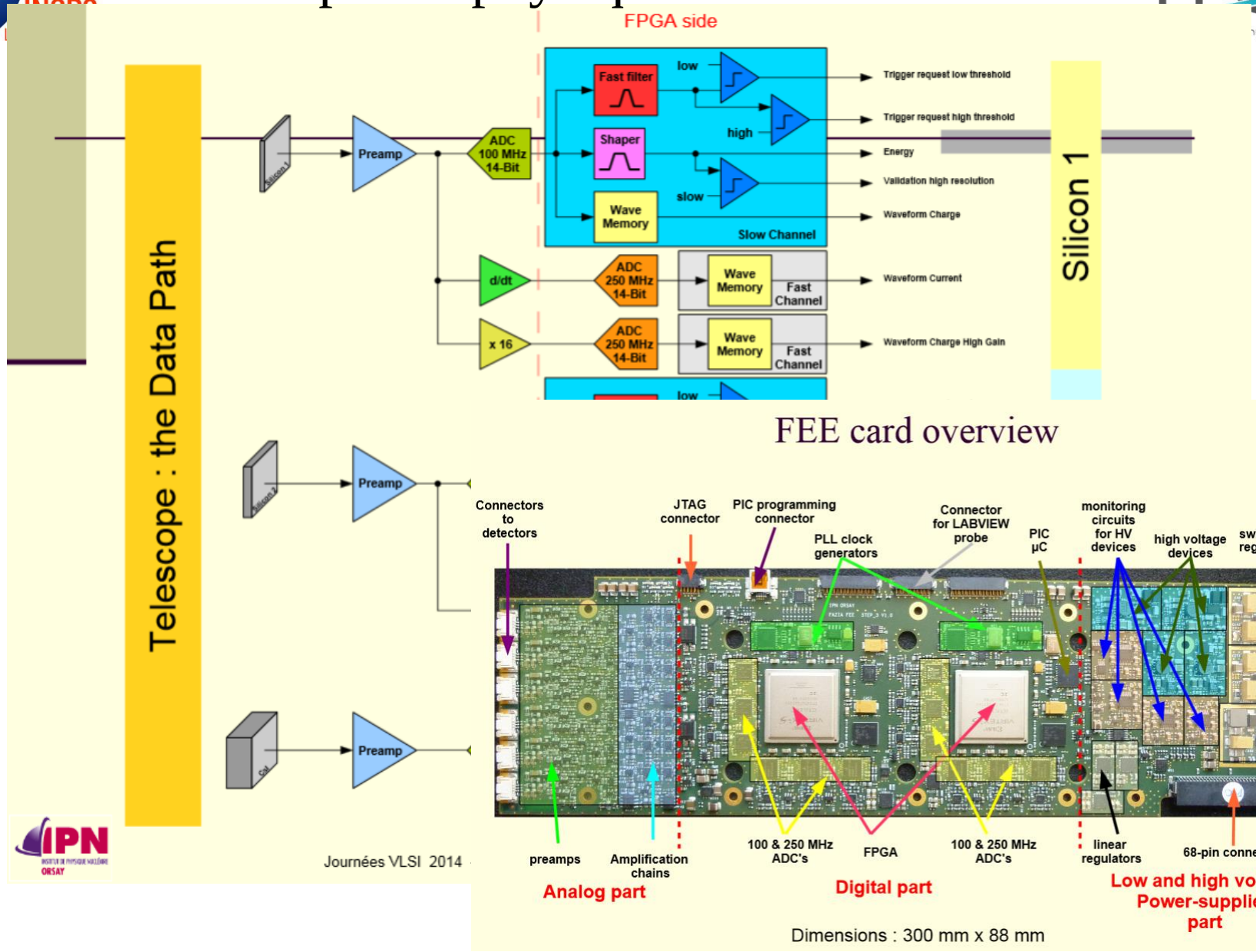


Exemple en physique nucléaire: FAZIA

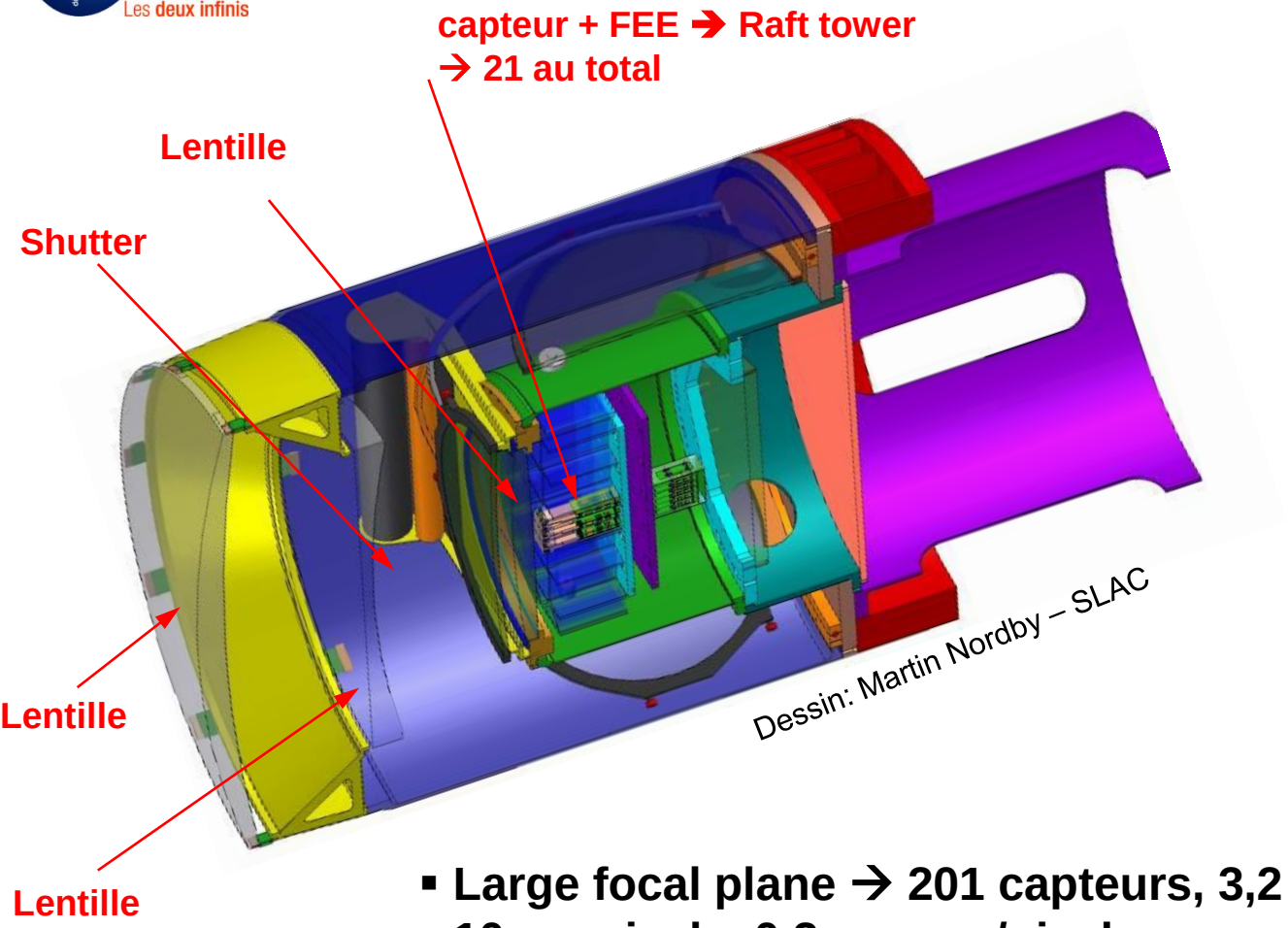
FAZIA est un multidétecteur de nouvelle génération pour les particules chargées, prévu pour servir dans le domaine des collisions d'ions lourds autour et au-dessous de l'énergie de Fermi (10-100 MeV par nucléon).



Exemple en physique nucléaire: FAZIA



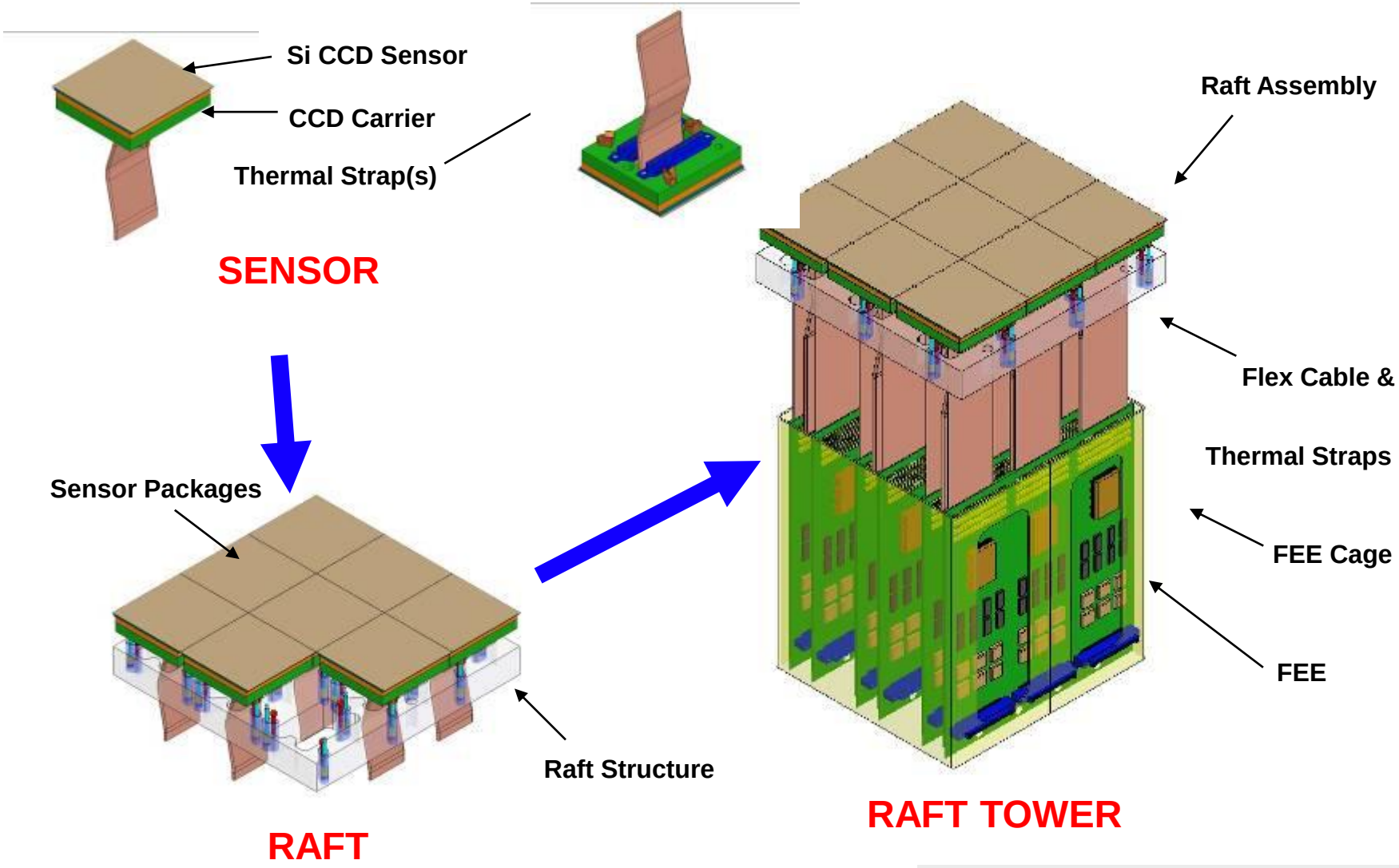
Large Synoptic Survey Telescop (LSST)



- **Large focal plane ➔ 201 capteurs, 3,2 Gpixels, 64 cm plan focal**
- **10 µm pixels, 0.2 arc-sec/pixel**
- **Chaque image: équivalent 40 lunes pleines**
- **Une image complète du ciel en 3 nuits**

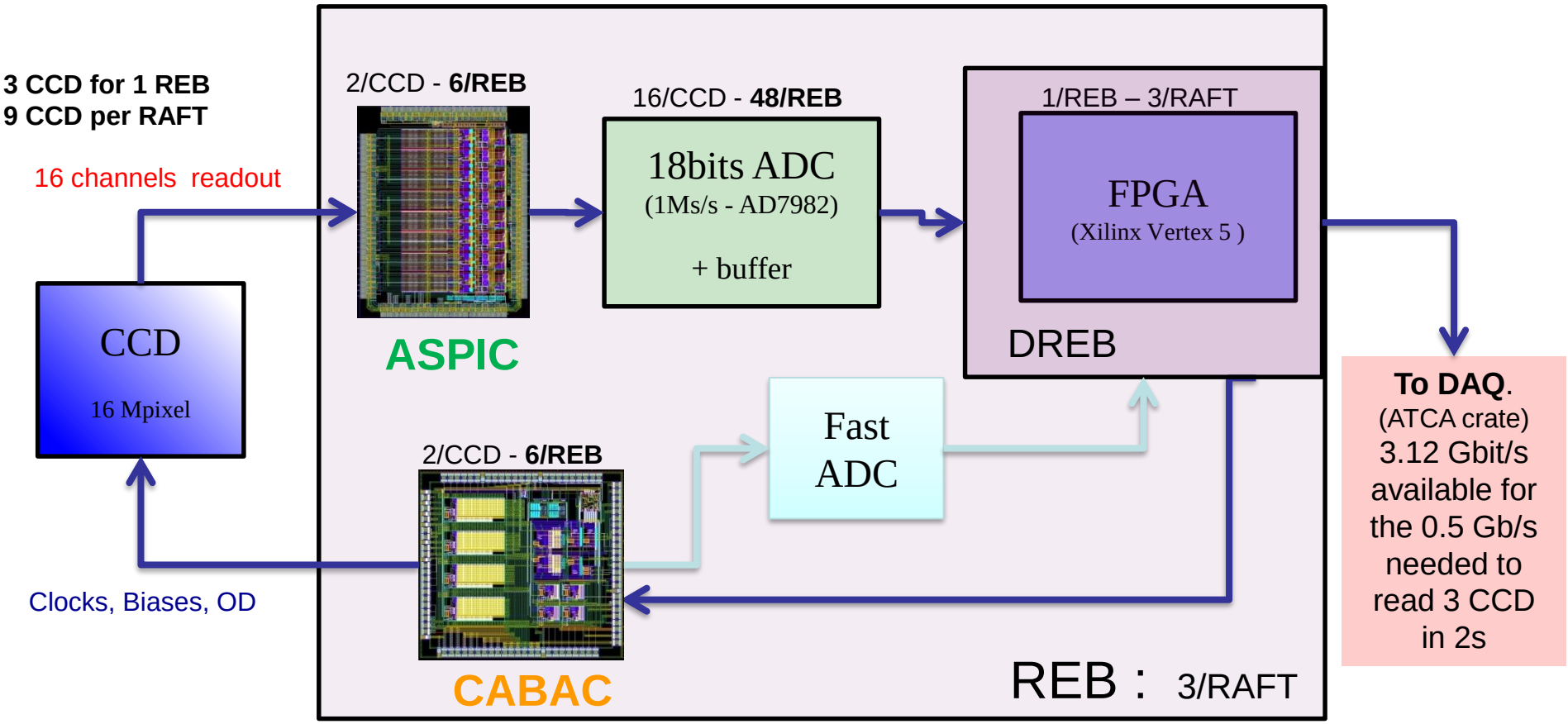
Source: K.Gilmore [LSST1] & J.Oliver [LSST2]

Large Synoptic Survey Telescop (LSST)



Source: K.Gilmore [LSST1] & J.Oliver [LSST2]

Camera Electronics : Raft Electronic Board



ASPIC a pour fonction d'amplifier les signaux analogiques provenant des 16 sorties de chaque CCD

16 sorties /CCD x 189 =

↳ **3024 voies d'électronique**

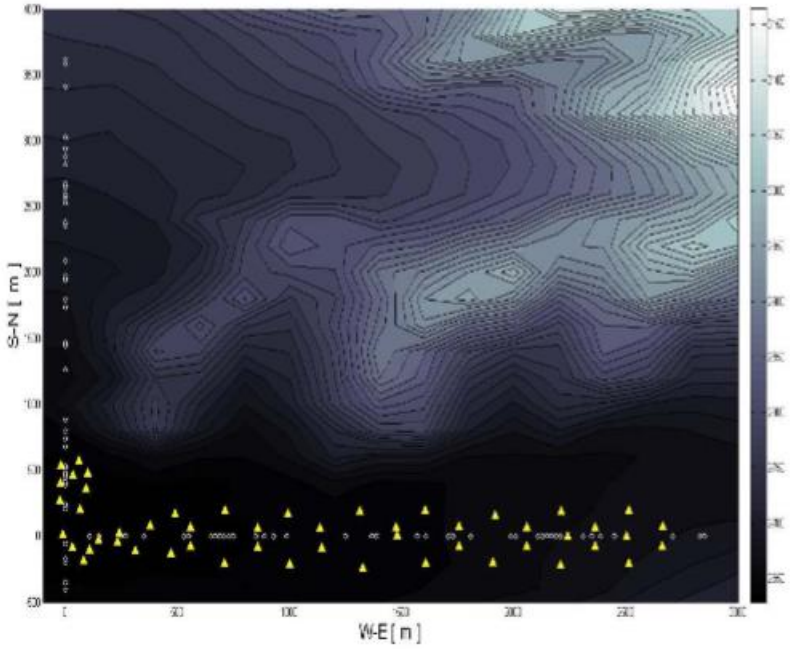
CABAC a pour fonction de fournir

- l'alimention (OD) de l'étage de sortie du CCD les polarisations : RD, OG, GD/SC
- Horloges "images" (parallel)
- Horloges "registres" (serial)

Expérience radio: TREND

INTRODUCTION TO THE TREND

- The aim of the Tianshan radio experiment for neutrino detection (TREND) is to build a large radio array to search for ultra high energy (UHE) neutrinos. The first results of TREND has already been announced (Astroparticle Physics, 2011, 34: 717-731).
  - Distribution of TREND 50 Pods



  - One pod

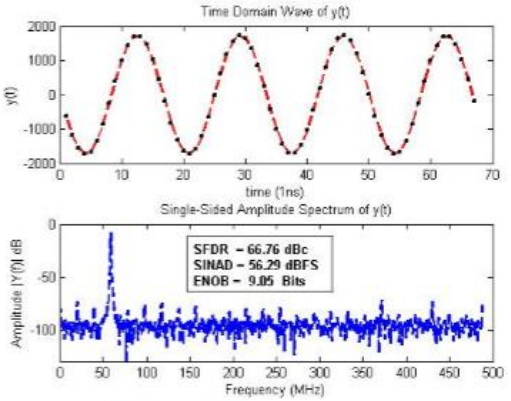
Expérience radio: TREND

THE SELF-TRIGGERING FRONT-END STATION(CONT.)

DFADC Board:

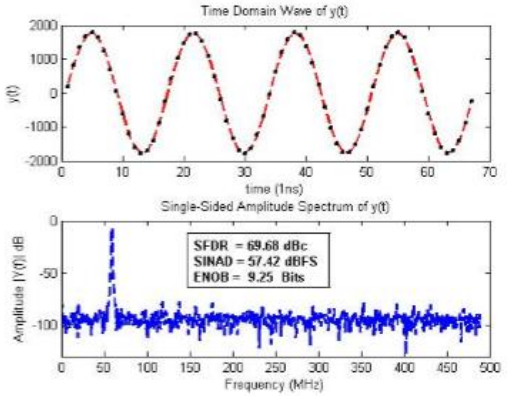
- Spartan 6 FPGA
- 12bit 1Gbps ADC(2 chns)
- 1Gb DDR2 RAM(2 Chips)
- 2 optical Link(3.125Gbps)
- USB host/peripheral Interf
- ...

ADC1



-1.3dBFS 60MHz sine signal input

ADC2



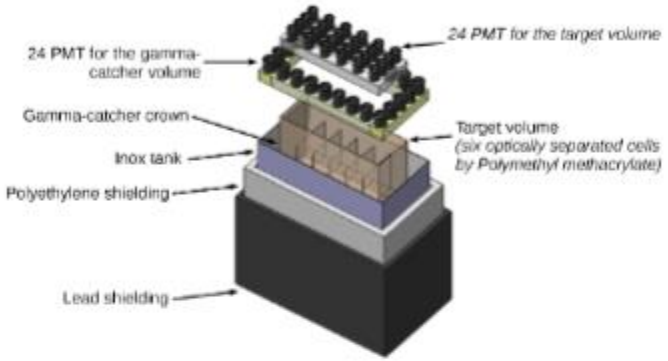
-1.3dBFS 60MHz sine signal input

Aperçu @ IN2P3

Journées VLSI - FPGA - PCB de l'IN2P3 2016
IPHC Strasbourg

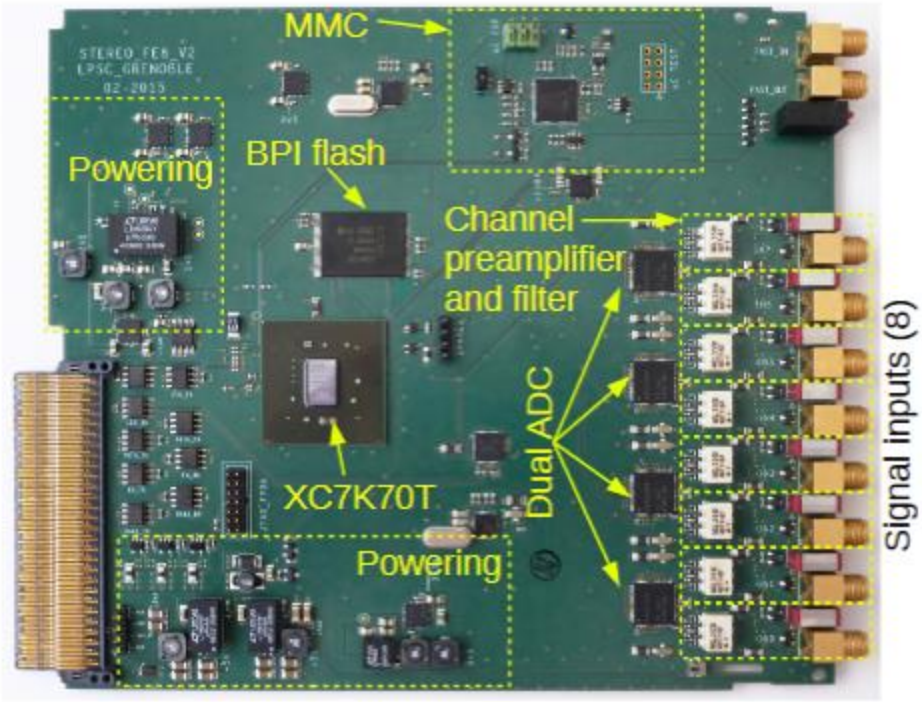
https://indico.in2p3.fr/event/12860/timetable/#20160531

General requirements



- Monitor 68 channels required in 3 classes (for triggering)
  - 24 PMT for Gamma catcher
  - 24 PMT for target (gadolinium-loaded liquid scintillator)
  - 20 PMT for muon veto (Cerenkov detector)
- Withstand a **mean** trigger rate of 1 kHz
- Have no dead-time (pile-up excepted)
- Manage various trigger schemes and conditions (coincidence and anti-coincidence)
- Process signals on board: compute Q_{tot} and Q_{tail} for *Pulse Shape discrimination (PSD)*

FE8 hardware



13 bit ADC @250 MSPS, dynamic range 1.0 V

- Main FPGA: XC7K70-2TFBG676,
- ADC: Texas Instrument ADS42LB49 (AC coupled, f_c >30 kHz)

8 Detailed Description

8.1 Overview

The ADS42LB69 and ADS42LB49 is a family of high linearity, buffered analog input, dual-channel ADCs with maximum sampling rates up to 250 MSPS employing either a quadruple data rate (QDR) or double data rate (DDR) LVDS interface. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 14 clock cycles. The output is available in LVDS logic levels in SPI-programmable QDR or DDR options.

???

- Have no dead-time (pile-up excepted)

8.2 Functional Block Diagrams

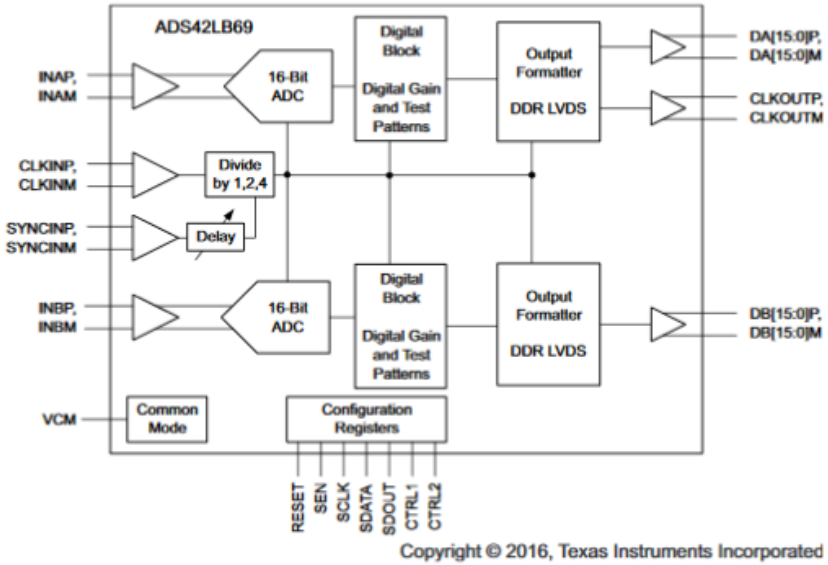


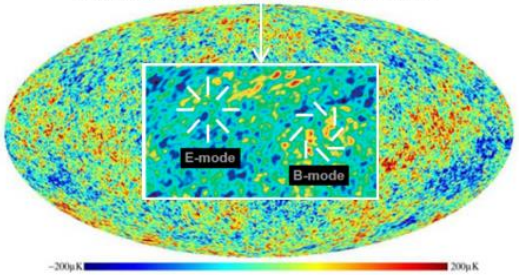
Figure 76. ADS42LB69 DDR LVDS

QUBIC (Q&U Bolometric Interferometer for Cosmology)

- Objectif scientifique:

  Polarisation des modes B du CMB (*Cosmic Microwave Background*)

E and B-mode polarization patterns



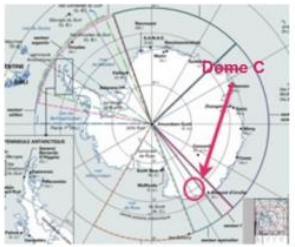
Full sky temperature anisotropies

- Collaboration internationale

APC Paris, France
IEF Orsay, France
CSNSM Orsay, France
CESR Toulouse, France
Maynooth University, Ireland
Universita di Milano-Bicocca, Italy
Universita degli studi di Milano, Italy
Universita La Sapienza, Roma, Italy
University of Manchester, UK
Richmond University, USA
Brown University, USA
University of Wisconsin, USA

- Télescope au sol :

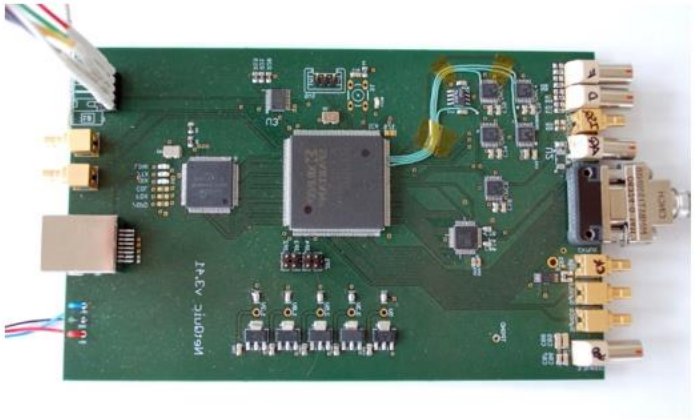
  Dôme C (Antarctique)



fabrice.voisin@apc.univ-paris7.fr – *Journées VLSI FPGA PCB et outils CAO* – 31 Mai/2 Juin 2016

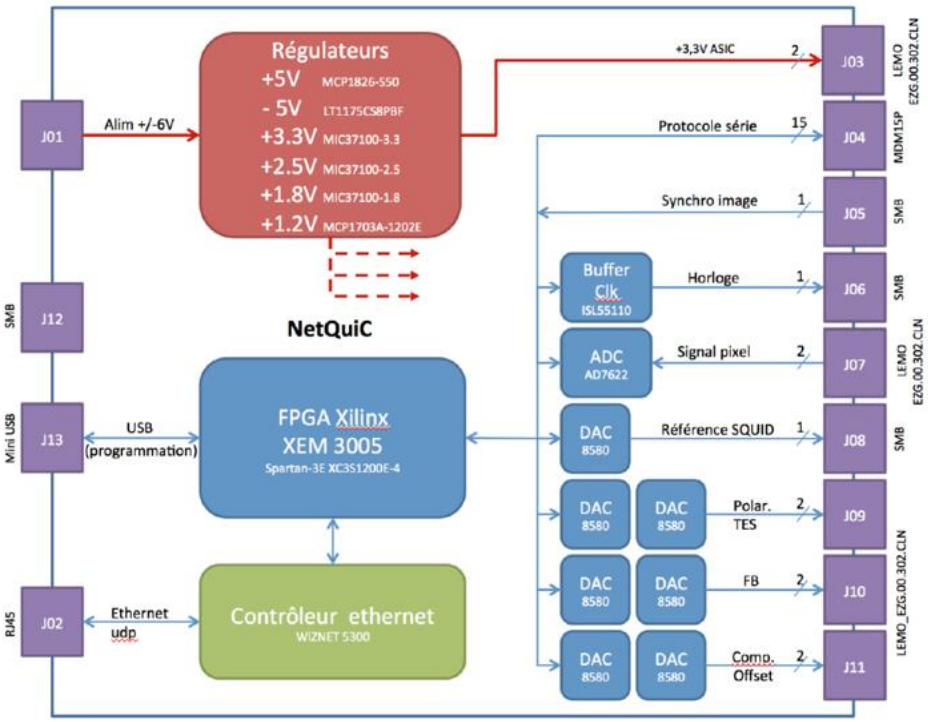
Electronique d'acquisition (300K)

Carte d'acquisition NetQuiC:



- Power supply ASIC
- Lien série ASIC
- Horloge multiplexage
- ADC/DAC
- FPGA
- …

16-Bit 2 MSPS SAR ADC

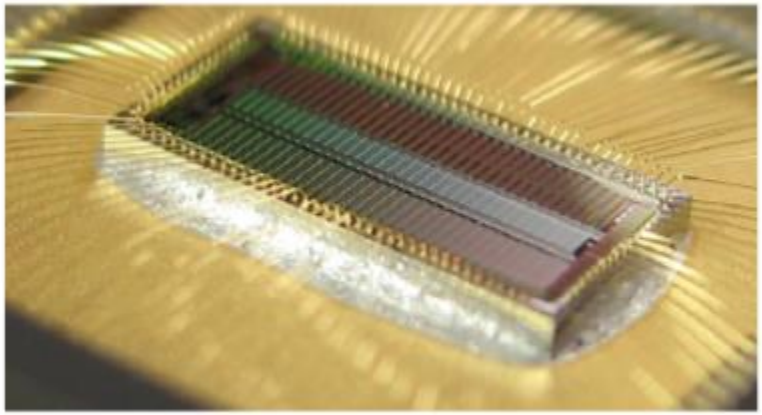


Irfu

Institut de recherche sur les lois fondamentales de l'Univers
Institute of Research into the Fundamental Laws of the Universe

OWB-1 : ADC 13-bits 32 voies pour les applications spatiales

Florent Bouyjou



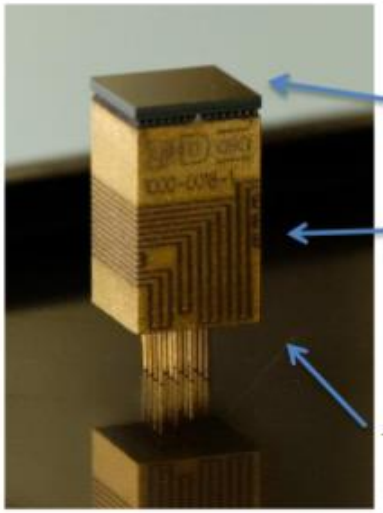
VLSI PCB FPGA–2016, Strasbourg

Contexte

Ce que nous avons fait à l'IRFU

Camera gamma Caliste :

- Densité très élevée de pixels **(600 µm)**
- Très haute résolution spectrale **(<1 keV at 60 keV)**
- Très faible consommation **(800 µW/voie)**
- Qualifiée spatiale

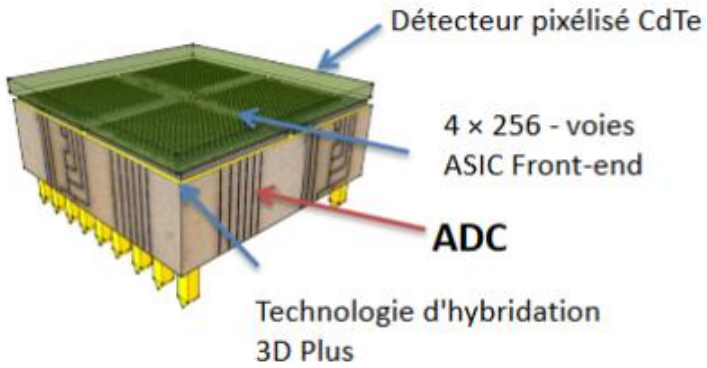


Etapes suivantes

Nouvelle micro caméra Gamma numérique :

Concevoir un ADC flexible :
Adaptés à chaque type d'architecture d'ASIC Front-end :

- Utilisable dans l'environnement spatial
- Haute résolution (typiquement 13 bits)
- Très bonnes performances en linéarité
- Faible consommation (<5mW / voie)
- Temps de conversion 1-10µs max

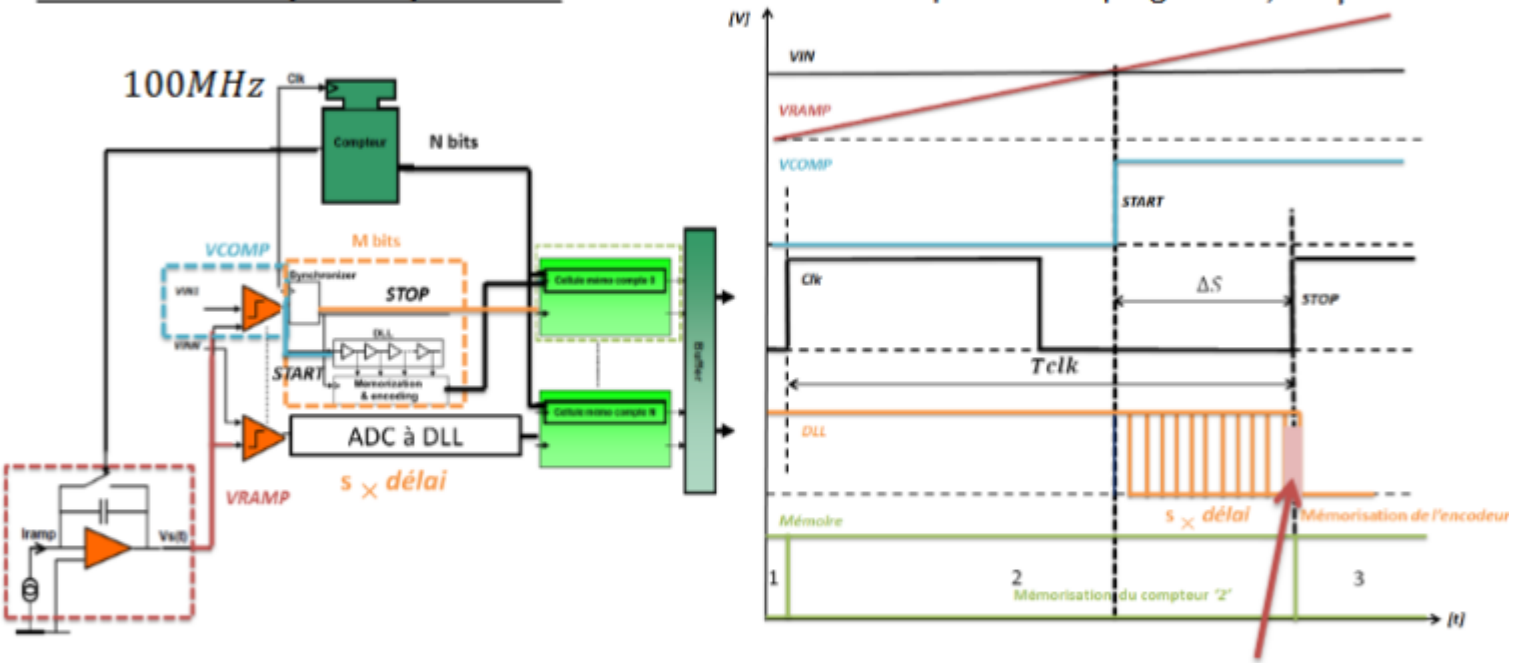


Nous avons choisi l'architecture Wilkinson

L'ADC à intégration + DLL

DLL (Delay-locked loop)

Wilkinson à simple rampe + DLL : Pour mesurer un temps sur une plage de $2,56\ \mu s$



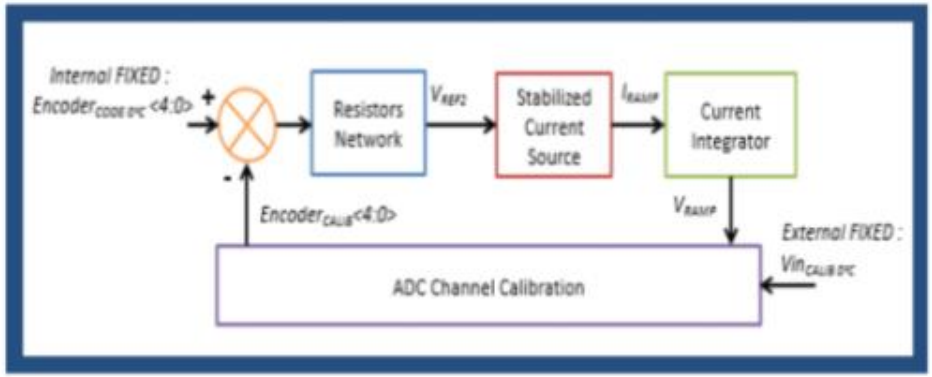
$Tconversion \times F_{DLL} = 2{,}56\ \mu s \times$ **3,2GHz** $= 8192$ soit **13 bits**

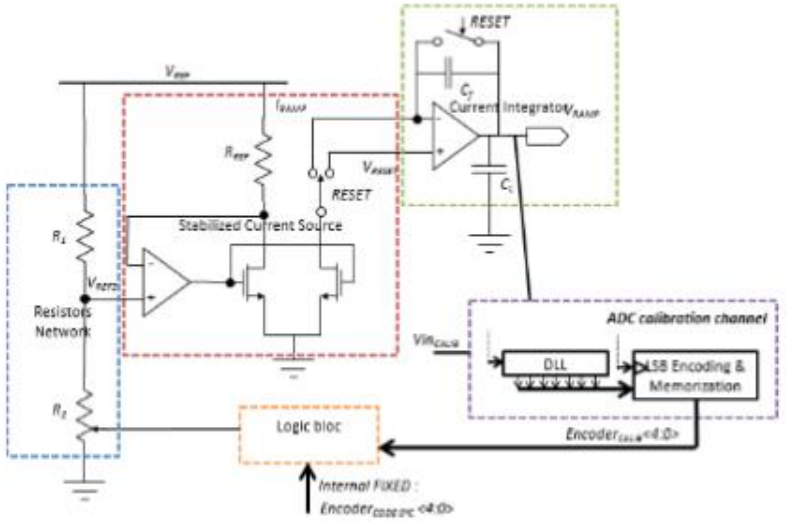
$Erreur\ \Delta t = 1/FDLL = 312{,}5\ ps$

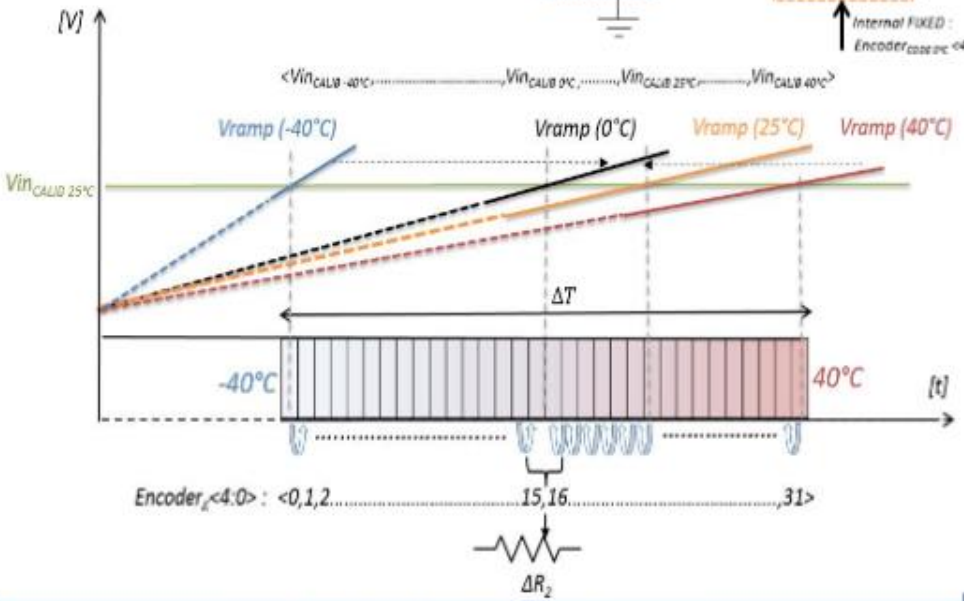
Wilkinson ➔ Wilkinson + DLL

8 bits ➔ 13 bits : 32 x plus précis !

Système d'auto-compensation en température intégré







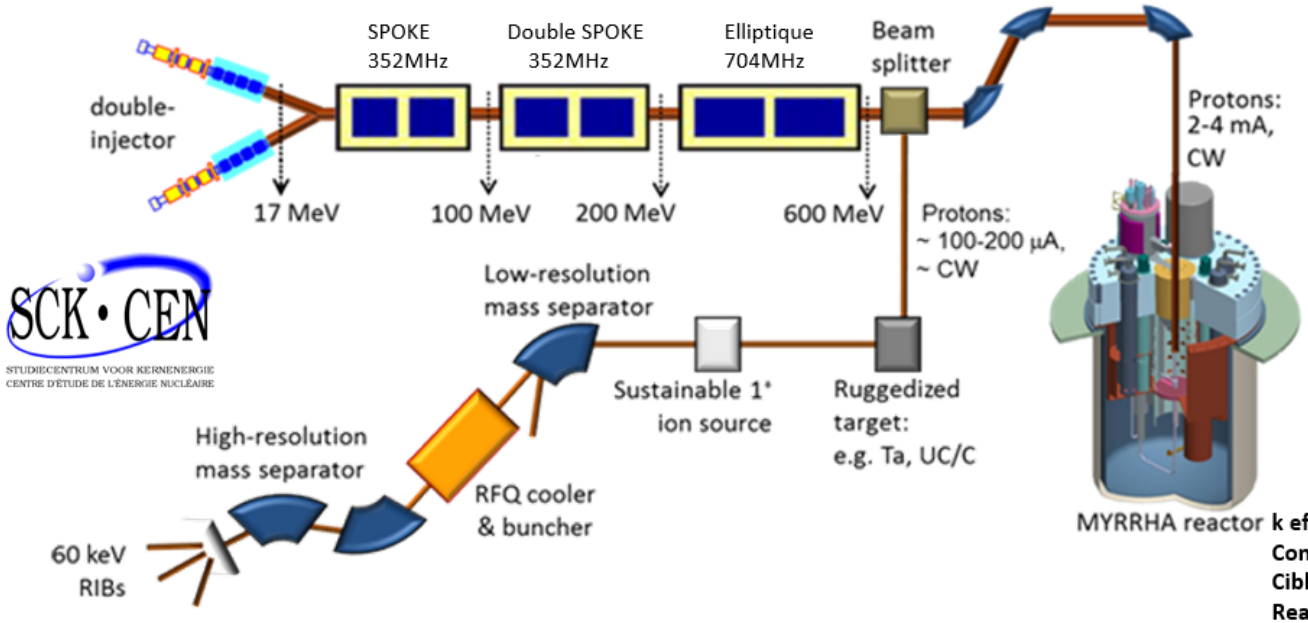
Aperçu @ IN2P3

Journées VLSI - FPGA - PCB de l'IN2P3 **2018**
LPC Clermont -Ferrand

https://indico.in2p3.fr/event/17125/timetable/#20180516

MYRRHA (ADS)

Multi-purpose hYbrid Research Reactor for High-tech Applications



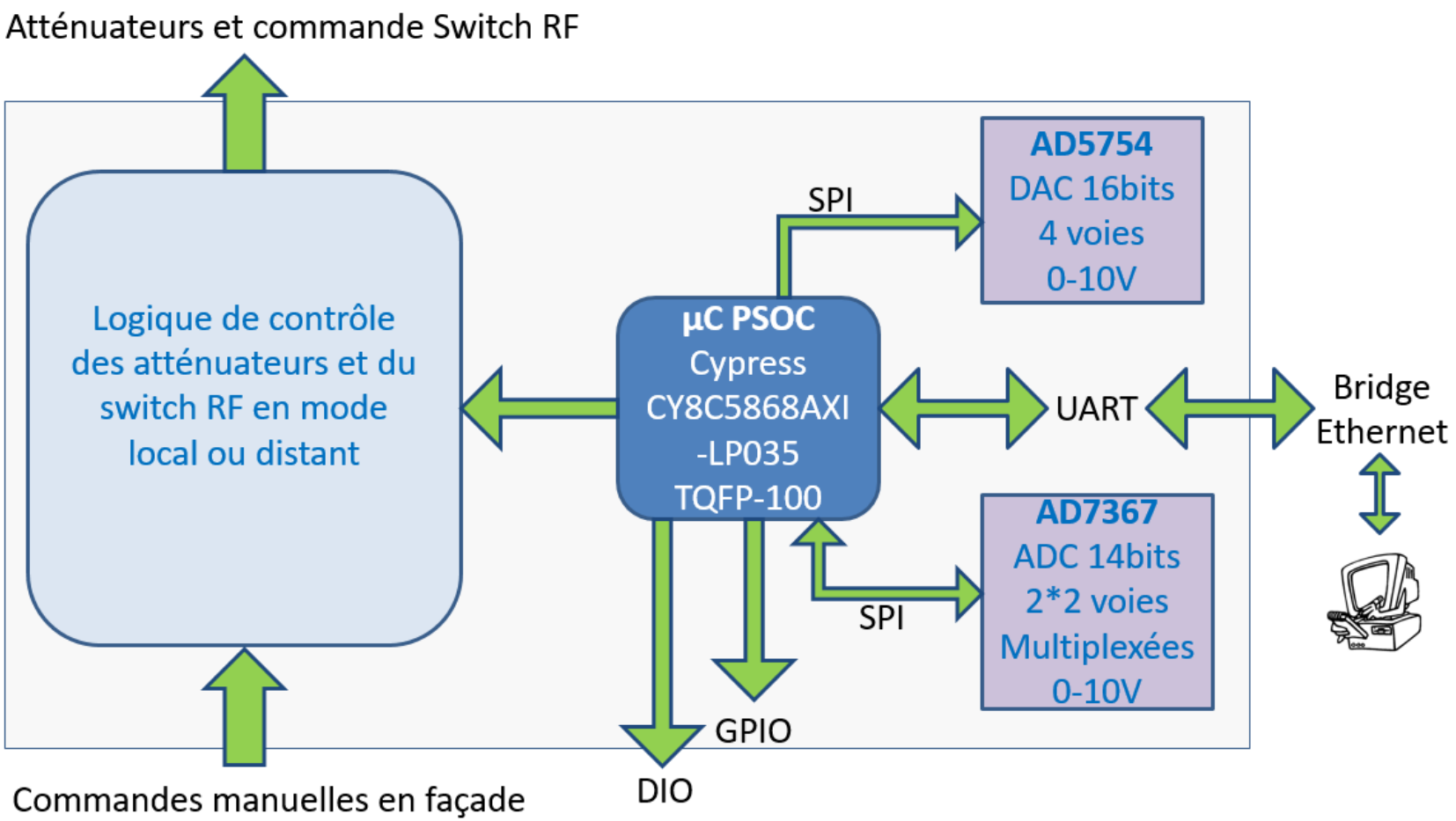
Objectifs :

- Construction d'un démonstrateur de réacteur hybride, pour la transmutation des déchets radiotoxiques, (ADS).

- Production de radio isotopes pour la médecine

- Recherche fondamentale

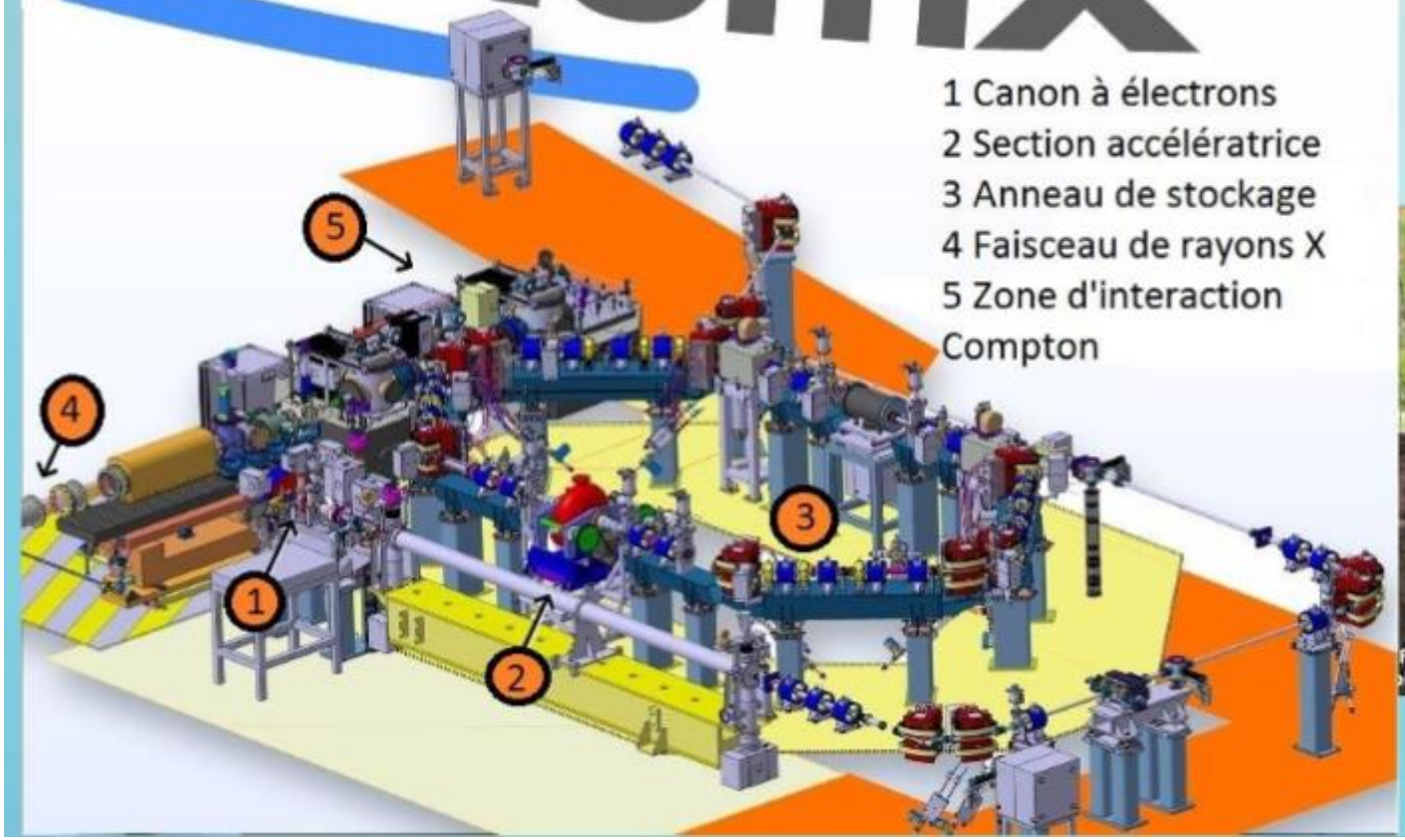
Carte µC


Atténuateurs et commande Switch RF
Logique de contrôle des atténuateurs et du switch RF en mode local ou distant
µC PSOC
Cypress
CY8C5868AXI
-LP035
TQFP-100
SPI
AD5754
DAC 16bits
4 voies
0-10V
UART
Bridge
Ethernet
SPI
AD7367
ADC 14bits
2*2 voies
Multiplexées
0-10V
GPIO
DIO
Commandes manuelles en façade

Source de rayon X compacte

ThomX

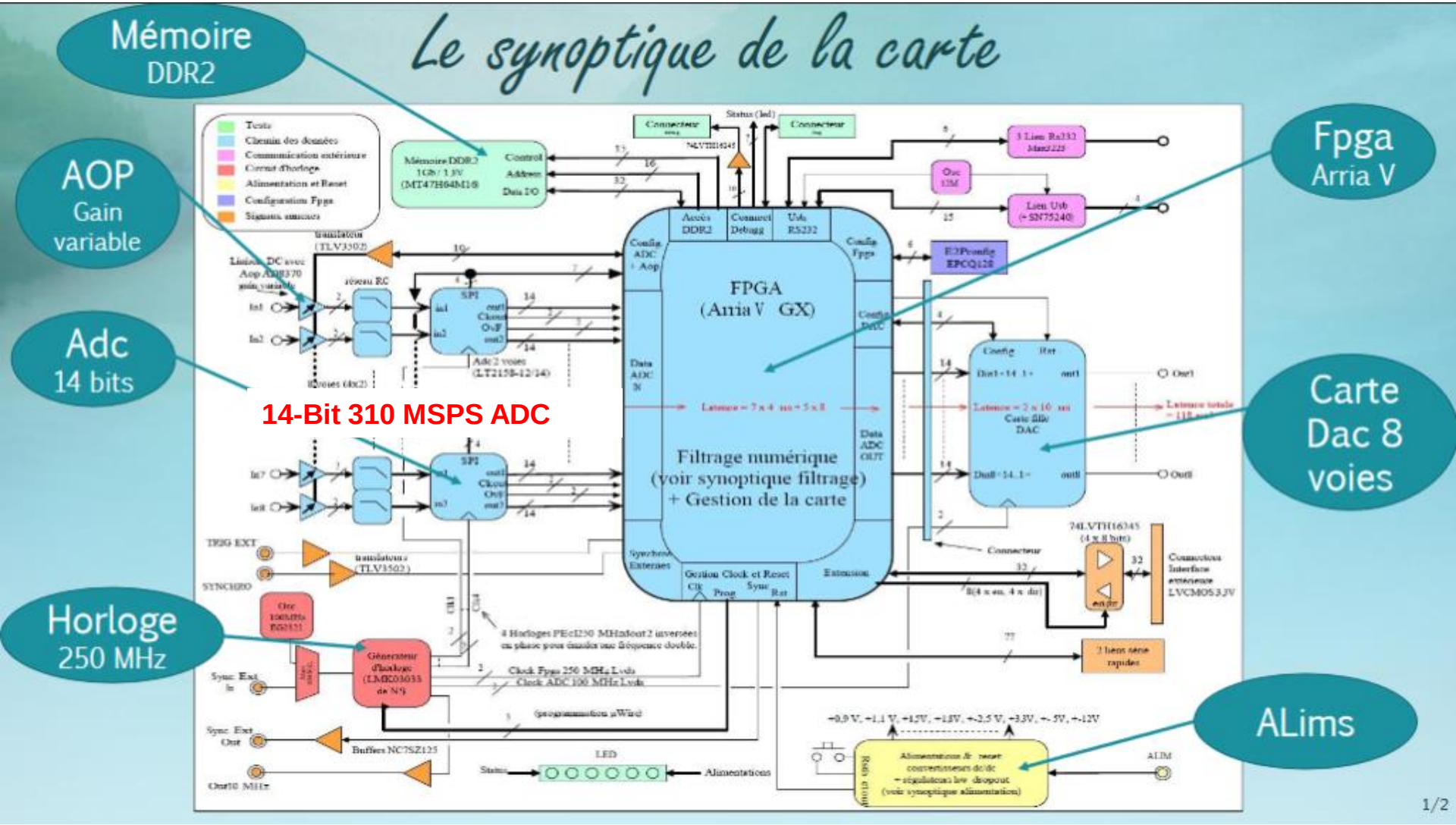
1 Canon à électrons
2 Section accélératrice
3 Anneau de stockage
4 Faisceau de rayons X
5 Zone d'interaction Compton



"ThomX", qu'est ce que c'est ?

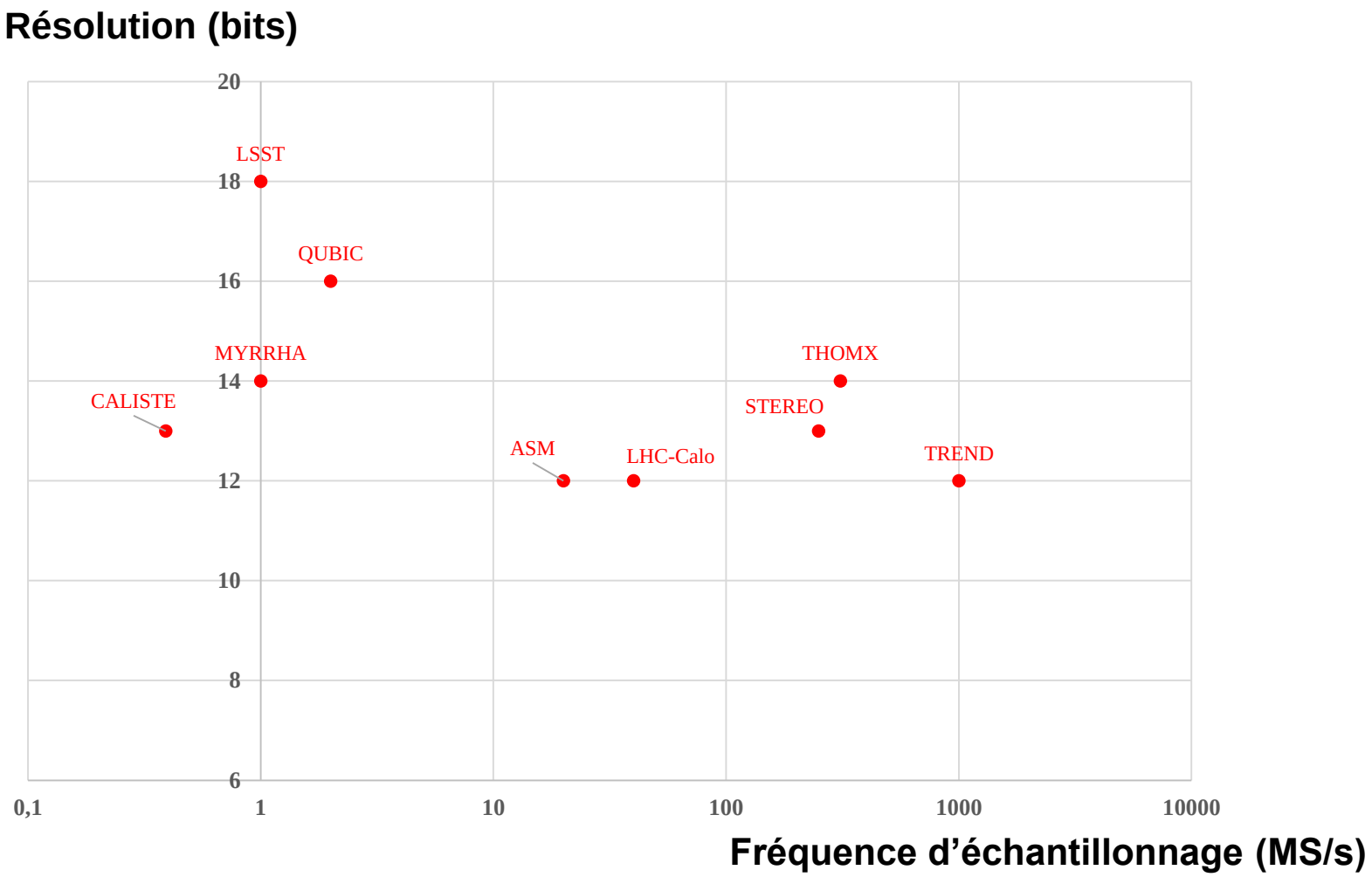
1/2

Le synoptique de la carte



1/2

Bilan ADCs @ VLSI 2014-16-18



Autres exemples à partager ??

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