Letter of Intent for LHCb Upgrade II

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Abstract

This document describes the contributions envisaged by the IN2P3 community to LHCb upgrade II. This new version of the LHCb detector will take data during the LHC Run 5 and beyond. First estimates of required funding and personnel are also provided.

1 LHCb Upgrades

The LHCb Collaboration intends to take full advantage of the flavour-physics opportunities at the High Luminosity LHC (HL-LHC) and further physics opportunities in the forward region. Therefore, the collaboration will improve its detector in two phases: LHCb Upgrade I and LHCb Upgrade II. The former is under commissioning and first data are expected in 2022. The latter would be deployed at the horizon of 2031 during Long Shutdown 4. After the submission of the Framework TDR [1] in September 2021, LHCb Upgrade II is under review by the LHCC Committee. Recommendations are expected in March 2022.

The main characteristics of the LHCb detector versions are summarised in Table 1.

	Period	Runs	$\mathcal{L}$ [cm^{-2}s^{-1}]	$\int \mathcal{L}$ [cm^{-2}s^{-1}]	Status
LHCb	2010 – 2018	Run 1 & 2	4×10^{32}	9	completed
		LHC shutdown LS2			
LHCb Upgrade I	2022 – 2030	Run 3 & 4	2×10^{33}	50	approved
		LHC shutdown LS3			
LHCb Upgrade II	2032 –	Run 5 and beyond	1.5×10^{34}	300	under approval
		LHC shutdown LS4			

Tab. 1: Characteristics of LHCb detector versions as a function of time. Upgrade of the detector takes place during the long shutdown of the LHC collider. LHCb Upgrade II is foreseen during LS3 and LS4.

In the next sections, we describe the interests of the IN2P3 community to build and exploit LHCb Upgrade II. We give more details of our intentions sketched in the Framework TDR and give first estimates for the required funding and personnel.

2 Physics motivations

The potential for flavour physics at the HL-LHC, expressed in the European Strategy statement [2], is justified by the achievements of the LHCb experiment during Run 1 and Run 2 of the LHC. In addition, the fact that new massive particles have, so far, not been discovered suggests any New Physics (NP) is likely to be beyond the mass scales directly accessible at the LHC. Consequently, precision, and thus extremely large data samples, is the key-word to clarify the situation.

The LHCb Upgrade I will greatly improve the sensitivity of many flavour studies. However, the precision on a host of measurements will still be limited by statistics, and other

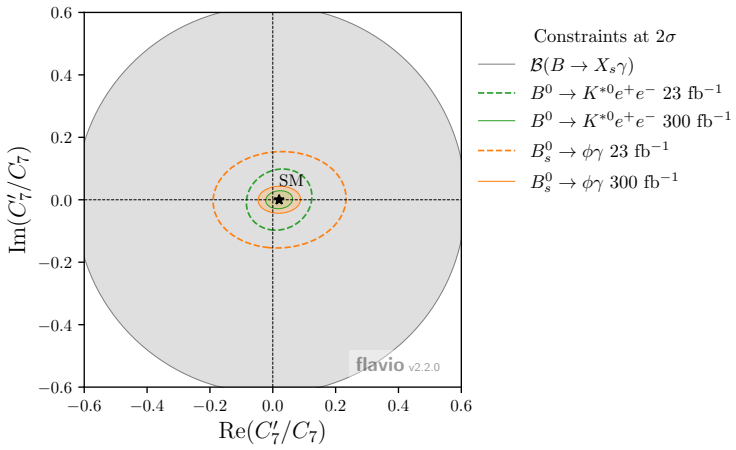

Fig. 1: Projected sensitivity with the LHCb Upgrade II detector and a total integrated luminosity of 300 fb^{-1} to the real and imaginary part of the ratio of right- and left-handed Wilson coefficients, C_7' and $C7$, obtained with the flavio software package [4]. Constraints are shown from observables that probe the polarisation of an on- or off-shell photon emitted in $b \to s\gamma$ transitions. The central values of the observables are arbitrarily set to the SM predictions [1].

observables associated with highly suppressed processes will still be poorly known. There is therefore strong motivation to build LHCb Upgrade II in order to fully realise the flavour-physics potential of the HL-LHC.

The Upgrade II flavour physics data sample will be significantly larger than that of any other planned experiment, and will lead to improvements in the precision of numerous observables without being limited by systematic uncertainties. This will allow to approximately double, with respect to the pre-HL-LHC period[1], the energy scale that is probed through precision measurements. While the main scope of LHCb Upgrade II will remain flavour physics, the flexibility of the full software trigger will allow LHCb Upgrade II to be a general purpose detector in the forward region (including electroweak, Higgs, top, heavy-ions physics, QCD and exotica searches). A detailed discussion of the physics case for LHCb Upgrade II is given in Refs. [1, 3]. As an illustration, the achievable sensitivity on the Wilson coefficient C_7 and C_7' is shown on Fig. 1.

The ambitious physics programme of this upgrade matches the science drivers *SD4* and *SD5* as well as the recommendation [2] for the intensity frontier provided by the working Group *GT01 – Physique des particules* which prepared the national prospective [5] for the period 2020 – 2030. The physics programme requires that a flexible trigger system and excellent detector performances in general are maintained. This includes the ability to have precise tracking down to low-p_T and particle identification. In addition, it is crucial to keep at the

[1] The LHCb experiment is expected to integrate 23 fb^{-1} within Run 3, at the end of the pre-HL-LHC era, and additional 300 fb^{-1} during the operation of HL-LHC.

[2] Exploit the two large-scale facilities with a wide flavour physics program, LHCb and Belle-2, which will provide further insights into the nature of the current flavor anomalies. Support the theoretical effort required to fully exploit the data, e.g., lattice calculations for flavour factories.

same level the LHCb analysis capacities for what concerns charged hadrons, electrons and photons and muons. In these different domains, the IN2P3 community can play a key role.

3 Calorimetry

The main challenge for the Electromagnetic Calorimeter (ECAL) during the phase II upgrade is to be able to cope with a multiplicity larger than the current conditions of the experiment, but keeping the same physics performances. This means keeping the same energy resolution ($\sigma(E) = 10\%\sqrt{E}$) and identification efficiency for electrons and photons. This is particularly important for the part of the LHCb physics program related to lepton universality, exotic spectroscopy or radiative rare decays measurements.

In the current design, the calorimeter is composed of scintillator-based modules whose light is readout by photo-multiplier tubes (PMTs) to measure particle energies, each of the modules being a readout channel for the front-end electronics. Two main new features will allow the ECAL to run under the phase II conditions:

- increase the detector granularity by decreasing the module sizes: a first layout proposal will lead to the increase of the number of readout channels by a factor of five;
- add the possibility to measure the arrival time of particles at the ECAL, with a resolution of about 25 ps, to distinguish particles originating from distinct primary vertices - on average 50 primary vertices per event are expected for the phase II instantaneous luminosity.

The ECAL upgrade project is composed of several activities: building the new hardware modules, replacing and improving the readout electronics chain, improving the mechanical structures and developing software. The LHCb teams at LAPP, LPC and IJCLab were involved in the front-end electronics, detector mechanics and software developments of the past calorimeter and wish to be active in the developments for its upgrade. These French teams have already actively participated to the simulation and performance studies realised for the Framework TDR [1] showing that a time resolution of about 25 ps is required to obtain the expected physics results.

3.1 Electronics

Concerning the electronics (LPC and IJCLab), the envisaged contribution consists in developing a readout chain capable of dealing with the increased number of channels and reaching the necessary time resolution.

Prototypes of modules designed for the ECAL upgrade were tested with beam and a time resolution of 15 ps was measured, for high energy electrons. The electronics chain must then have a time resolution of 20 ps so that the overall time resolution is 25 ps. The ASIC components currently available, based on time-to-digital converter (TDC) technologies, reach

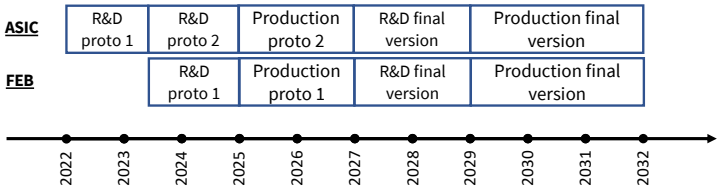

Fig. 2: Planning for the ECAL Upgrade II Front-End electronics project.

performances of about 35 ps. For the ECAL project, a technology based on analogue memories will be employed, for which an expertise has been developed at IJCLab in the past years. The main challenge of the project is to use this technology in a dedicated ASIC which will measure simultaneously the time and the energy. Such a component will also have applications beyond the LHCb ECAL Upgrade II use case.

The design and realisation of the ASIC involve teams from Barcelona, Valencia, LPC Clermont-Ferrand and IJCLab Orsay. Other members of the MICRHAU pole have also expressed interest in the project, and their possible involvement is currently under discussion. The design and realisation of the front-end boards that will host the ASIC and be the interface to the back-end readout boards is under discussion, but the LHCb effort on this aspect is currently led by IJCLab Orsay.

Several tasks are identified for the project: coordination of the entire electronics project (Barcelona and IJCLab), ASIC design (very front-end - Barcelona, analogue memories - IJCLab, digital Front-End - LPC, production - Barcelona), data processing (LPC and IJCLab), test bench (IJCLab) and Front-End board design (IJCLab).

The project can be basically split in two steps: a first step where a first ASIC prototype will be designed, installed during LS3 and tested with the ECAL during Run 4, with the current DAQ architecture. The outcome of this step will be to equip the 32 innermost modules of the ECAL which must be replaced during LS3 because of radiation damage. These modules will have an improved timing response and the experiment will benefit from being able to have a precise timing measurement for them. For this reason, the corresponding channels of these new modules (600 in total) will be equipped with the ASIC prototype and a small number of new front-end boards (10). This will allow us to test the performances of the future electronics in realistic conditions.

A second step will consist in designing a new front-end board to interface with the new infrastructure foreseen for Run 5. During this step, the ASIC prototype will be refined following observations made during data taking in Run 4 with the central modules. The overall planning is shown in Fig 2. The total number of readout channels at this stage will be of 30 000, and about 500 Front-End boards will be needed.

3.2 Mechanics

The mechanical structures of ECAL consist of two L-shape movable supporting structures on which ECAL modules are installed, and an electronics platform on the top hosting the electronics racks for the crates of the front-end boards. These structures are stabilised by a gantry and several additional beams. The cables coming from the PMTs of ECAL modules are fixed to bands and go through cylindrical holes in the storage box located under the electronic platform, which stores the extra cable length, and to the racks. The bands are fixed at the bottom on the lower support and at the top on the electronic platform.

For the Upgrade II, several modifications are foreseen to adapt these structures to the new modules and the additional front-end boards required by about five times more readout cables of these new modules. The baseline scenario is a replacement during LS3 of the innermost 32 modules surrounding the beam pipe, which have reached the limit of accumulation of radiation doses. In order to prepare for Upgrade II by taking advantage of the LS3 duration, a more ambitious proposal is the replacement of the adjacent 144 modules and the reshuffling of the remaining modules according to the occupancy map. The complete modifications of the ECAL mechanical structures are foreseen during LS3, with the constraints of installing additional modules at LS4 without the need of dismantling the electronic platform.

The mechanical service at LAPP has performed the design and studies of the mechanical and seismic resistances of the whole calorimeter structures. It proposes to take care of the mechanical modifications of the ECAL structures. The technical contributions envisaged are the modification of the side of the gantry to access the electronic platform, the enlargement of the electronic platform to host additional racks, the modification of the cable storage box, the modification of the cable holding system and the design of mechanical support and dimensioning of the seismic shock absorbers. All these modifications will require also the calculations with finite element analysis software to assess the good stability of the whole ECAL structures.

3.3 Person-power and costs

The envisaged activities in ECAL Upgrade II represent a straight continuation of the LAPP, LPC an IJCLab LHCb group involvements in Calorimetry since 1998. The ECAL Upgrade II is supported by about 16 physicists at IJCLab, LAPP and LPC. A preliminary estimate for technical person-power is shown in Table 2 as a function of time. The corresponding costs for R&D and construction, are given in Table 3 and 4.

The FTDR cost for the construction of ECAL is 34.8 MCHF. We envisage to contribute at the level 110 k€ for R&D, 1.7 M€ for construction with a technical person-power of up to 6 FTE per year. An IN2P3 R&T grant of 50 k€ has been provided to cover the R&D of the ASIC between 2022 and 2024. We also envisage having 2 PhD theses on the electronics development.

			Run 3				LS 3			Run 4			LS 4	
Project	Institutes	Staff	22	23	24	25	26	27	28	29	30	31	32	33
ECAL	IJCLab +	management	0.3	0.3	0.3	0.3	0.3	0.4	0.3	0.4	0.4	0.4	0.3	-
	LAPP +	microelectronics	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	-	-	-	-
	and LPC	electronics	0.3	2.3	2.5	1.9	0.1	1.7	1.8	1.9	0.3	0.5	0.3	-
		mechanics	0.2	0.5	1.1	1.7	1.4	0.7	0.3	-	-	-	-	-
		computing	-	0.4	0.4	0.4	0.4	-	-	-	-	-	-	-
		instrumentation	-	0.3	0.3	0.3	-	-	-	0.3	0.3	0.3	-	-
Subtotal			2.7	5.7	6.5	6.5	4.0	4.7	4.3	4.5	1.0	1.2	0.6	
UT	LPNHE +	management	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
	LLR +	electronics	0.4	1.1	2.5	2.7	2.6	2.6	2.6	2.6	2.6	2.6	1.6	1.6
	SUBATECH	mechanics	0.2	1.0	1.3	2.5	2.3	2.3	2.3	2.3	2.3	2.3	2.0	2.0
Subtotal			0.9	2.4	4.1	5.5	5.2	5.2	5.2	5.2	5.2	5.2	3.9	3.9
PCIe400	CPPM +	management	0.6	0.6	0.4	0.3	0.3	0.6	0.6	0.4	0.3	0.3		
	CENBG +	electronics	4.1	4.1	3.1	-	-	4.1	4.1	3.1	-	-	-	-
	IJCLab +	mechanics	0.5	-	-	-	-	0.5	-	-	-	-	-	-
	LAPP and	computing	-	-	-	-	-	-	-	-	-	-	-	-
	LPC Caen	quality	-	-	-	1	-	-	-	-	1	-	-	-
		instrumentation	-	-	-	2	3	-	-	-	2	3	-	-
Subtotal			6.3	6.3	4.6	3.3	3.3	6.3	6.3	4.6	3.3	3.3		
RTA	LPNHE +	management	0.75	0.25	0.25	0.75	0.75	0.75	0.75	0.25	0.25	0.25	0.25	0.75
	CPPM +	electronics	-	0.7	0.7	0.7	-	-	-	-	-	-	-	-
	LLR +	computing	1.55	1.85	1.85	1.85	1.25	1.25	1.25	1.25	1.25	1.25	1.25	
	IJCLab +													
	LAPP													
Subtotal			2.4	3.4	3.4	2.8	2.1	2.1	2.1	2.0	2.0	2.0	1.3	
Total			12.2	17.7	18.5	18.0	14.6	18.2	17.8	16.3	11.5	11.7	5.8	3.9

Tab. 2: Preliminary estimation of the required technical person-power per project and per year, for IN2P3 contributions.

R&D	Run 3				LS 3			Run 4			LS 4	
	22	23	24	25	26	27	28	29	30	31	32	33
ECAL	50		55					55				
UT	105		105									
PCIe400	47	49	13			47	49	13				
RTA	50							50				
Total	137	139	106	93	-	47	49	57	44	17	-	-

Tab. 3: Preliminary estimation of the R&D cost per project and per period, for IN2P3 contributions, in k€.

CORE	Run 3				LS 3			Run 4			LS 4	
	22	23	24	25	26	27	28	29	30	31	32	33
ECAL			75		150					1 500		
UT					60	60	60	570	670	720		
PCIe400				105	210				105	210		
RTA												
Total	-	-	75	105	345	135	60	570	775	2 430	-	-

Tab. 4: Preliminary estimation of the construction cost per project and per period, for IN2P3 contributions, in k€

4 Tracking

In LHCb Upgrades, the trajectography is performed by three detectors: the Vertex Locator (VELO), the Upstream Tracker (UT) and the Scintillating Fiber Tracker (SciFi)/Mighty Tracker (MT). The UT (SciFy/MT) is located upstream (downstream) of the magnet, respectively. UT facilitates the track matching between segments near primary vertices and downstream of the magnet. Without the UT, the rate of fake matches is unacceptably high.

The *UT Upgrade I* consists of four planes of silicon strips sensors. This system was optimised for a luminosity of 2×10^{33} cm^{-2}s^{-1}. However, it cannot cope with the data rate expected in Upgrade II, nor with a total ionisation dose above an integrated luminosity of 50 fb^{-1}. Therefore, a new UT detector is mandatory to fulfil the challenging experimental conditions of the HL-LHC expected for Run 5 and beyond.

The two relevant quantities for the future UT design are the mean and maximum hit density per bunch crossing. The former is expected to be higher in *pp* collisions, constraining the data readout scheme. The latter is larger in central PbPb collisions, constraining the detector granularity.

A possible detector layout is based on four square planes of $\sim$2.25 m^2 each. A plane consists of 12 vertical staves. Given the data taking conditions and required performances, silicon pixels are envisaged. A possible technology is Tower-Jazz 180 nm already used for ALICE-ALPIDE and MONOPIX. Each stave would have 36 modules, one module made of 4×2 CMOS chips, with a typical pixel size of 30×30 μm^2.

The UT upgrade project is composed of several activities which might be organised in five work packages: Simulations and performances in *pp* and PbPb (WP1); Chip design and characterisation (WP2); Module stave and mechanical structure (WP3); Overall mechanics, integration and services (WP4) and Detector readout (WP5).

French institutes expressed a strong interest in that project, namely LPNHE, LLR, Subatech and IRFU. In particular, IRFU and Subatech will benefit from the great experience acquired during the design and production processes of the ALICE Muon Forward Tracker in which they played together a leading role. The envisioned contributions by the French groups cover all the aspects of the detector design and construction, from chip conception to detector construction, installation and commissioning, thanks to the expertise of IRFU and Subatech in CMOS MAPS detectors and that of LPNHE and LLR in chip characterisation, detector readout and composite materials.

4.1 Simulations and performance

An important optimisation effort has already started. At LPNHE, they will study the standalone UT reconstruction in order to further explore and optimise the design of the UT upgrade. At LLR and IRFU, they simulate heavy ion events to study track matching efficiencies and detector occupancies toward the optimisation of the pixel matrix design. Some high priority studies envisioned for the near future are: the optimisation of the number and

layout of planes, the possibility to combine UT track segments with hits in the future magnet stations, the inclusion of precise timing information in the reconstruction, the optimisation of the pixel sizes and the optimisation of the readout design.

4.2 Electronics

IN2P3 groups wish to contribute to several aspects of the electronics part of the project, such as sensor characterisation (LLR) and front-end and back-end readout (Subatech, LPNHE). Those contributions would be complementary with that of IRFU, involving several engineers and technicians FTE on Silicon sensor design, and reinforce the impact and visibility of French institutions.

4.3 Mechanics

Thanks to their expertise in composite materials and the availability of the adequate tools (such as an autoclave) IN2P3 groups are in a privileged position, and wish to significantly contribute to the mechanical-structure design of the detector.

4.4 Person-power and costs

The envisaged activities in UT Upgrade II represent a continuity of IN2P3 involvements in the Muon Forward Tracking detector as well as in MAP sensors. The UT Upgrade II is supported by about 14 physicists at LLR, LPNHE and Subatech, and 6 physicists at IRFU. Preliminary estimation for technical person-power is shown in Table 2 as a function of time. Corresponding costs for R&D and construction, are given in Table 3 and 4.

The FTDR cost for the construction of UT is 8.9 MCHF. We envisage to contribute at the level of 310 k€ for R&D, 2.14 M€ for construction with technical person-power up to 5.5 FTE per year.

5 Data acquisition and real time processing

The data acquisition system for the LHCb Upgrade II will be very similar to the one used in Upgrade I. It is mainly divided into two parts. The first one is the *event-builder* and the second one is a *computer farm* which reconstructs and selects collision events interesting for physics.

Event-building is done for all LHC collisions, at 40 MHz, and will handle about 200 Tbits/s. The computer farm reconstructs all collisions in almost real time with ultimate software precision thanks to a calibration performed online also in real time. Finally, events interesting for the physics analyses are selected and stored on tape. For LHCb Upgrade I, the architecture of the computer farm is a heterogeneous one. The first step of the reconstruction is a fast

reconstruction performed by GPU cards embedded in event-builder servers, while the second step is a full reconstruction done by dedicated servers running algorithms on CPU. For the Upgrade II, both fast and full reconstruction algorithms will be executed on a farm running GPUs.

Following major contributions to the Upgrade I, the IN2P3 community has interests in the data acquisition area, namely through the development of a new generic readout board and in the RTA project. Envisaged contributions are described in the next subsections.

5.1 Data acquisition

The readout board that was developed for the Upgrade I, PCIe40, is a generic and multi-purpose board. The same hardware is used for readout, slow control and to distribute fast commands as well as the LHC clock. The different functionalities are obtained by programming different firmwares in the FPGA of the board.

The readout board interfaces the front-end electronics with the event-builder. It concatenates data, transforming the input streams which are transmitted with a custom protocol into an output stream based on a standard protocol used in the data-centre computers. For Upgrade II, the former protocol will be the lpGBT protocol at 10 Gbits/s, while the latter will be either PCIe Gen5 or Ethernet at 400 Gbit/s.

The new board designed for Upgrade II will increase the current bandwidth of the PCIe40 board by a factor 4 [6]. It can be built around a macro FPGA from the Agilex Intel family of FPGAs. A new readout board can be connected to front-end electronics with up to 48 bidirectional optical links. It is flexible since it can follow the evolution of the front-end link speed, targeting 56 Gbits/s in the future.

A first board using the PCIe Gen5 interface will be developed by using FPGAs available in 2022, allowing to reach the nominal bandwidth of 400 Gbit/s. It will be used for all new detectors added during LS3. The future generations of FPGAs will have a larger quantity of high bandwidth on-chip memory. This will allow integrating the full network functionality within the readout board on the horizon of 2030. At that time, the bandwidth might be improved by another factor of two, following evolution PCIe/Ethernet standards.

In the continuity of the PCIe40 project, CPPM aims at taking the responsibility of the new readout board development, of the design of the hardware as well as the low-level firmware of the FPGAs. LAPP aims at taking the responsibility for the firmware development of all the common parts of sub-detectors.

Contributions to the design, production and exploitation of the future readout board will keep IN2P3 at the leading edge of the development of highly versatile and powerful boards capable of handling a large bandwidth with numerous serial links and tight constraints on a time reference. It will also push our competence in programming very large FPGAs which might play a key role in future high-performance computing systems. In addition, the proposed upgraded board is generic and already found interest in the HEP community (for the future

upgrades of the Belle II and ALICE experiments), opening doors for future collaborations beyond LHCb.

5.2 Real Time Analysis

In a harsh environment with about 50 vertices and more than 2000 tracks per collision, during Upgrade II, the first-level reconstruction algorithms decode data, look for tracks with a p_{T} as low as 500 MeV/c, reconstruct vertices, identify tracks using calorimeter, muon and RICH information, and determine the ultimate track parameters by using a Kalman Fit. They also associate tracks to their vertex by using timing information. After detectors alignment and calibration, the full reconstruction will be performed in real time with an input rate between 5 and 10 MHz and an output bandwidth of 50 GB/s.

The software implementing these algorithms will be developed within a framework allowing to run the reconstruction on different platforms like CPU or GPU and with hardware coming from different vendors. A dedicated data model is used to exchange data between algorithms in such a high-performance environment.

Preparing the full reconstruction for the Upgrade II will require physicists to design algorithms handling millions of channels, dealing with timing and spatial information from various detectors. Those algorithms will have to be vectorised and to run in parallel. It also requires computing engineers to identify the best hardware (GPU, IPU, FPGA, etc.) and to use it in an optimum way. Improvements to the software lead to improved physics performance, for example by allowing the first-level tracking algorithms to reconstruct tracks with a p_{T} below 500 MeV/c, benefiting charm and strange physics.

Beyond such first-level improvements, a faster and more efficient software would enable running the full reconstruction at rates higher than the nominal 5-10 MHz, bringing LHCb very close to the ultimate goal of being able to perform the full detector reconstruction for every LHC bunch crossing.

CPPM, IJCLab, LAPP and LPNHE aim at contributing to this adventure. Contributions can be organised in four work packages: Processing in readout board (WP1); Multi-platform framework, speed-up and quality (WP2); Reconstruction algorithms for trajectography and calorimetry (WP3); Calibration tools and algorithms (WP4). A possible planning is shown in Fig. 3.

<table>
<tr><th colspan="2"></th><th>2022</th><th>2023</th><th>2024</th><th>2025</th><th>2026</th><th>2027</th><th>2028</th><th>2029</th><th>2030</th><th>2031</th><th>2032</th><th>2033</th></tr>
<tr><td>WP1</td><td>Reconstruction in readout chain</td><td colspan="4">R&D proto 1</td><td colspan="3">Production proto 1</td><td colspan="3">R&D final version</td><td>Production final version</td></tr>
<tr><td rowspan="2">WP2</td><td rowspan="2">Multi-platform framework, speed-up & quality</td><td colspan="4">Generalization Allen → Allen++</td><td colspan="3">Reco speedup & new U1a detector reco</td><td colspan="3">Speedup & U2 detector reco</td><td></td></tr>
<tr><td colspan="12">Continuous maintenance of the software and firmware repositories, dependencies, preservation of production software versions for open access purposes</td></tr>
<tr><td rowspan="2">WP3</td><td>Fast reconstruction</td><td colspan="4">Continuous improvement of Allen, R&D Allen++</td><td colspan="3" rowspan="2">Production Allen ++</td><td colspan="4" rowspan="2">Continuous improvement of Allen++</td></tr>
<tr><td>Full reconstruction</td><td colspan="4">Transfer full reco algorithms to Allen</td></tr>
<tr><td>WP4</td><td>Calibration tools and algorithms</td><td colspan="4">Continuous improvement of algorithms & methods</td><td colspan="3">Tools & algorithms proto</td><td colspan="4">Tools & algorithmsfor final version</td></tr>
</table>

Fig. 3: Planning for the RTA Upgrade II project.

Contributing to such developments will keep IN2P3 at the leading edge of trigger-less architecture in which event building, reconstruction and selection are performed almost in real time. At the output of the chain, events can be directly analysed. This matches the recommendations[3] provided by the working group *GT09 – Calcul, algorithmes et données* which prepared the national prospective [5] for the period 2020 – 2030. This project is also a good opportunity to learn and experience state-of-the-art high-performance computing, including machine learning techniques. It opens the possibility to collaborate with other CNRS laboratories outside IN2P3, as well as institutes associated with universities near IN2P3 laboratories which are involved in computing.

5.3 Person-power and costs

The envisaged activities in data acquisition and real time computing represent a straight continuation of our involvements in LHCb Upgrade I. The RTA Upgrade II is supported by about 6 physicists at CPPM, IJCLab, LAPP and LPNHE. A preliminary estimate for technical person-power is shown in Table 2 as a function of time. The corresponding costs for R&D and construction are given in Table 3 and 4.

The FTDR cost for all readout boards is around 7 MCHF. It will be mostly covered by sub-detectors. We envisage to contribute at the level of 220 k€ for R&D and of 650 k€ for construction, with a technical person-power of up to 6 FTE per year. An IN2P3 R&T grant of 110 k€ has been provided to cover the first step of the R&D between 2022 and 2024.

The FTDR cost for RTA is 17.4 MCHF. We envisage to contribute at the level of 100 k€ for R&D and with a technical person-power up to 3 FTE per year. The construction cost will be covered by all institutes of LHCb through the Common Fund.

6 R&D Cooling with microchannels

The vertex detector of LHCb is operated in vacuum and requires active cooling at very low temperature to mitigate the effect of the radiation damage on the silicon sensors. Substrates with microchannels etched into silicon were chosen for the VELO Upgrade I, showing high cooling performance for a moderate material budget.

The bonding of plates has been one of the most critical step of the manufacturing process, leading to a relatively high production cost of the microchannels radiator. A R&D has started in CPPM, exploring alternative bonding processes that would drastically cut down the production cost. Two processes have been investigated : anodic bonding with an intermediate thin layer of glass and thermo-compression with intermediate layers of gold. According to the first results, both techniques would allow reaching the pressure resistance required for the

[3] Make use of and extend expertise in Real Time Analysis. This allows enhancing the scientific throughput of experiments, in particular when facing limited storage resources. This requires using in production advanced algorithms (in particular in Machine Learning) on GPU/FPGA. Make use and extend IN2P3 expertise on ML/DL in real-time applications on innovative infrastructures.

VELO cooling system.

To finalise this proof of concept, the R&D is now focusing on the development of a connector bonding process. The very encouraging results that have been obtained so far give very good prospects for these techniques to be used to develop a low cost microchannels-based cooling system for the upgraded VELO and the CPPM is eager to move forward to the realisation of a demonstrator.

7 Computing

At the output of the full reconstruction, data are split into 3 streams: FULL, TURBO and TURCAL. The information to store can range from only the objects involved in a trigger decision only through to the full event and even some raw data banks. A special case is represented by the calibration TURCAL stream, where raw data banks of events selected for detector alignment and calibration are persisted. The TURBO stream is then ready to be used directly in physics analysis. The TURCAL and FULL streams are further filtered and slimmed offline before storing them on disk, in order to mitigate the disk storage requirements.

The computing work is dominated by simulation production. It has been observed, so far, that the number of produced events scales with the integrated luminosity. Events are produced using either a detailed Geant4-based simulation, or a palette of faster simulation options, ranging from techniques, where the same underlying event is reused, but new signal decays are generated and simulated in detail every time, to fully parametric simulations.

Estimation of the computing resources for the Run 5 and 6 is based on the computing model of the LHCb Upgrade I. A scale factor 5 is applied on the yearly integrated luminosity as well as on the number of events to be simulated. Other parameters are kept unchanged. Main parameters of the model for Upgrade II are summarised in Table 5.

Model assumptions	
	Upgrade II
Peak L ($cm^{-2}s^{-1}$)	1.5×10^{34}
Yearly integrated luminosity (fb^{-1})	50
Logical bandwidth to tape (GB/s)	50
Logical bandwidth to disk (GB/s)	17.5
Running time (s)	5×10^6
Fraction Full / Turbo / TurCal (%)	26 / 68 / 6
Ratio Turbo/Full event size	16.7%
Ratio full/fast/param. MC	40:40:20
CPU work per event full/fast/param. MC (HS06.s)	1200 / 400 / 20
Number of simulated events	$4.8 \times 10^9/fb^{-1}$/year
Data replicas on tape	2 (1 for derived data)
Data replicas on disk	2 (Turbo); 3 (Full, TurCal)
MC replicas on tape	1 (MDST)
MC replicas on disk	0.3 (MDST, 30% of the total dataset)

Tab. 5: Summary of the computing model parameters and main assumptions, for LHCb Upgrade II.

The Figure 4 compare the required tape as a function of time with what can be acquired

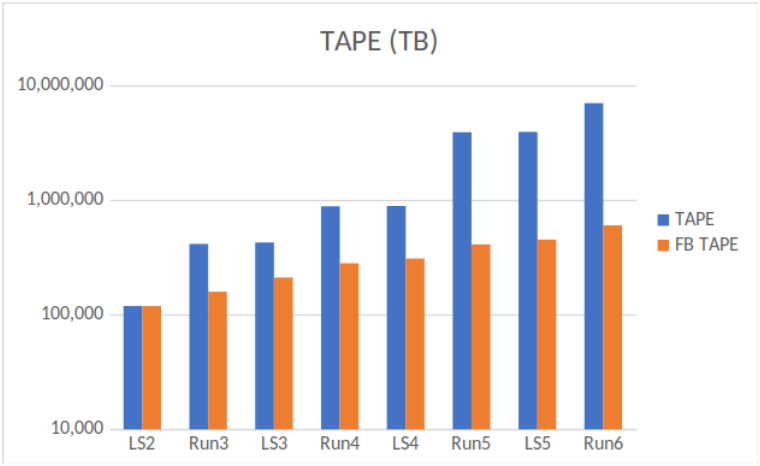

Fig. 4: the evolution of the tape as a function of time. In blue what is needed and in orange what can be acquired in a flat budget Scenario. In this estimation the data of the Run 3 are collected during 3 years [2022 – 2024] and the duration of LS3 is 2.5 years.

with a flat budget. It shows that a flat-budget approach is not working any more. The same pattern is also observed for CPU and disk.

Mitigation strategies are under study by the HEP community and by the LHCb Collaboration. They concern the simulation, the storage and the data management. LHCb will carefully follow the developments, in common with the other experiments and in coordination with WLCG and the HEP Software Foundation, with the obvious benefits of an entire community working in close contact. In order to sustain the R&D required to meet the challenge of efficiently exploiting modern CPU architectures, considerable investment in software engineers is required.

8 Conclusions

LHCb is a general purpose detector in the forward region. The physics programme includes a comprehensive range of flavour physics measurements, spectroscopy studies, QCD and electroweak physics, heavy ion and fixed target opportunities and long-lived particle searches. It is unique and shall take data in the coming two decades. It is also well recognised by the international community.

Contributing to the LHCb Upgrade II is an opportunity to reveal and identify physics beyond the standard model, to push our competences towards the state-of-the-art calorimetry, tracking, data acquisition and real-time processing. It will also prepare the next generation of engineers and physicists to design, build and manage future big experiments.

The total investments for IN2P3 are at the level of 688 k€ for R&D, 4 500 k€ for construction and with technical person-power of 166 FTE. These preliminary estimates do not include a safety margin related to exchange rate, inflation or evolution of the fair share within the

collaboration. They can also evolve to follow improvements in detector design. Our technical contributions might be assisted by fixed-term contracts for engineers, funding for technical PhD students and possibly by project assistants.

IN2P3 will participate with common funds to the cost of the common electronics, general infrastructure and data centre facilities (13 500 kCHF). Common funds will be also used to cover the cost of the RTA processing farm (17 400 kCHF) and of the Online system (8 850 kCHF), with the institutes contributing to the development of the architecture and custom components of these projects (*e.g.* the readout board for the Online project).

Discussions will be held with the Resource Review Board (RRB), leading to an addendum to the LHCb Memorandum of Understanding (MoU) covering the sub-detector construction and common fund. This MoU is anticipated in 2025, in parallel to the presentation of sub-detector TDRs to the LHCC, and in time to start detector construction at the beginning of 2026.

Despite many difficulties related to funding, evolution of technical staff and the increase of the average age of the LHCb France members, we are eager to strongly contribute to this major evolution.

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Links for LHCb upgrades :

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Intérêts technologiques de LHCb Upgrade II pour les laboratoires et pour l'IN2P3

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Abstract

Cette note éclaire brièvement en quoi les contributions envisagées à la construction du futur détecteur LHCb Upgrade II permettront de faire évoluer nos savoir-faire et nos compétences tant au niveau des laboratoires que de l'institut. Développements stratégiques pour rester à la pointe et pour préparer les futures générations d'ingénieurs et de physiciens aux expériences à venir.

1 Calorimétrie

Le projet calorimétrie LHCb ECAL2 consiste à mesurer le temps d'arrivée des particules dans le détecteur avec une grande précision, de l'ordre de 20 ps conjointement avec une mesure en énergie pour réaliser les objectifs de physique pour ce calorimètre. Les modules envisagés pour construire le calorimètre ont une résolution en temps intrinsèque de 15 ps environ. Pour avoir une précision en temps totale de 20 ps (RMS), la chaîne d'électronique devra avoir aussi une résolution de l'ordre de 15 ps, en ayant une mesure précise de l'énergie sur 12 bits.

La mesure en temps sera réalisée dans un ASIC dédié, qui fonctionnera en parallèle d'un ASIC mesurant la charge (énergie) et qui sera développé conjointement avec Barcelone et Valence en Espagne. Avoir deux ASICs séparés permettra de réutiliser pour d'autres applications ou d'autres détecteurs l'ASIC dédié à la mesure de temps. Les solutions actuelles développées pour la physique des particules, basées sur des circuits TDC permettent d'avoir des résolutions de 35 ps, mais sont limitées par la sensibilité aux dispersions d'amplitude du signal.

La solution que nous proposons est basée sur le principe d'échantillonnage du signal à haute fréquence (quelques GS/s) dans une mémoire analogique, de sa numérisation puis de l'application d'un algorithme d'extraction du temps à partir des valeurs des échantillons. Elle est notamment utilisée par l'ASIC SAMPIC développé par IJCLab et l'IRFU, qui offre une résolution de 3 ps RMS. Les équipes de IJCLab sont un des leaders mondiaux dans ce domaine. L'émergence des besoins de mesure en temps des grandes expériences comme celles du LHC est une opportunité à saisir pour l'IN2P3 pour faire bénéficier de cette expertise la communauté de physique des particules. La gamme d'énergie sur laquelle nous souhaitons faire une mesure de temps se situe entre 100 MeV et 5 GeV soit un rapport 50. L'architecture à base de mémoire analogique est un système pertinent pour répondre à ce point du cahier des charges particulièrement exigeant. La résolution de 15 ps sur cette dynamique est un véritable défi, en particulier pour le faire à la fréquence de 40 MHz du LHC. Les évolutions nécessaires par rapport à l'architecture de l'ASIC SAMPIC, en particulier celles concernant le temps mort et le taux de comptage moyen, constituent un défi technologique majeur.

Ce design complexe nécessitera la réalisation d'un circuit mixte avec une importante partie numérique. La technologie envisagée pour le développement est la technologie TSMC CMOS 65 nm, nouvelle pour la majorité des microélectroniciens de l'IN2P3.

La méthodologie de conception utilisée devrait être *Digital on Top* comme conseillé par les experts de cette technologie au CERN. Cette méthodologie est aujourd'hui encore mal maîtrisée par la communauté IN2P3 et ce projet qui sera réalisé en collaboration entre plusieurs

groupes microélectroniques de l'IN2P3 (IJCLab, LPC Clermont, IP2I-MICRHAU) permettra ainsi d'acquérir et de diffuser un savoir-faire crucial pour la suite dans le domaine. Cet ASIC permettra de faire une mesure de temps sur les plusieurs milliers de voies de mesure du calorimètre.

La prise en charge des bancs de tests sera faite par IJCLab et le LPC Clermont. De plus, la fédération MI2I (Microélectronique des 2 Infinis) soutient ce développement d'ASIC fédérateur pour les microélectroniciens de l'Institut et permettra de mieux travailler ensemble sur les techniques de mesure du temps à haute résolution. Au-delà de la réalisation de ce composant, l'architecture complète du système ainsi que la carte Front-End seront aussi à concevoir pour pouvoir y intégrer et réaliser les traitements numériques nécessaires pour transmettre les données du calorimètre à la ferme de calcul de LHCb.

2 Trajectographie

Les capteurs monolithiques CMOS à pixels actifs (MAPS) sont des détecteurs semi-conducteurs ayant la particularité d'intégrer à la fois la partie sensible et l'électronique de lecture sur un même substrat de silicium homogène.

LLR : Le groupe électronique du LLR possède, à ce jour, une grande expertise dans la caractérisation et l'étude de performances de capteurs tels que les SiPM, PMT ou wafer de silicium, ainsi que des ASICs de lecture de ces capteurs : SPIROC, SKYROC, HGROC, PEPITAS, etc. Pour ces éléments de front-end, le LLR a la capacité de mettre en oeuvre et instrumenter les électroniques de tests associées, permettant l'ensemble de ces qualifications. Le groupe n'a jusqu'ici aucune expérience dans le test de capteurs MAPS.

La participation à l'upgrade UT de LHCb offrira la possibilité d'élargir le domaine de compétence et d'expertise du groupe. Cela fera du LLR un des acteurs incontournables pour ce savoir au sein de l'IN2P3 et reconnu sur le plan international.

LPNHE : Le LPNHE dispose d'une expertise solide dans le développement de firmwares notamment pour les cartes PCIe40 du projet SciFi, qu'il sera intéressant de maintenir et développer pour la programmation des cartes back-end de l'Upgrade II. Il sera, par exemple, judicieux pour le laboratoire et l'institut d'explorer et de mettre en pratique des technologies de conception haut niveau (HLS).

Les équipes techniques du LPNHE ont par ailleurs acquis une expertise en développement de banc de tests instrumentaux et en caractérisation de détecteurs (par exemple : CTA, DAMIC, LSST). Aussi, une participation dans cette thématique est une option intéressante à explorer dans le but de maintenir ces compétences.

SUBATECH :

1. **Structure mécanique et thermique :** Le service mécanique de SUBATECH a pris en charge la conception de structures mécaniques et thermiques pour la construction de détecteurs de l'expérience ALICE comme EmCAL et MFT. Travailler sur la conception du mur de détection de l'UT de LHCb utiliserait parfaitement cette compétence. S'il fallait refroidir de manière importante les détecteurs MAPS, l'utilisation de micro-canaux ou de liquide cryogénique serait nécéssaire. La conception et la réalisation d'un tel système de refroidissement constituerait une montée en compétence pour le laboratoire.

2. **Intégration et services :** SUBATECH a montré ses compétences en matière d'intégration mécanique et de services (puissance et refroidissement) lors de son implication sur les détecteurs EmCAL et MFT avec un haut niveau d'intégration mécanique et électronique, pris en charge en interne. Cette expérience sur les détecteurs MAPS amincis est immédiatement utilisable sur l'UT de LHCb et si elle ne débouche pas directement sur une montée en compétence, SUBATECH pourrait prendre en charge une partie importante des opérations de construction.

3. **Readout et banc de test :** L'utilisation de capteurs en silicium de type MAPS nécessite une électronique de lecture capable de gérer un flux de données important et incluant une logique permettant leur contrôle et leur configuration. Ce premier niveau d'électronique de lecture repose sur l'emploi de cartes à base de FPGA qui nécessite des compétences de programmation présentes à SUBATECH et que le laboratoire souhaite maintenir et renforcer. Travailler sur ce premier code de lecture prolongerait l'expérience acquise sur l'électronique de lecture du MID d'ALICE tout en augmentant le savoir-faire lié à une plus haute vitesse d'acquisition. Cette étape pourrait permettre de participer à la réalisation d'un banc de test pour la caractérisation des capteurs MAPS, activité dans laquelle l'équipe du MFT s'était déjà impliquée.

4. **Filtrage et reconstruction :** SUBATECH a crée un pôle pour la modélisation numérique et le développement logiciel en support direct pour le spectromètre à muons d'ALICE. Les défis sur la réduction nécessaire du flux de données de l'UT de LHCb au plus tôt dans la chaîne d'acquisition permettront de s'impliquer sur cette activité afin de poursuivre la montée en compétences des membres du pôle.

CPPM : Le refroidissement des détecteurs à pixels à l'aide de micro-canaux gravés dans un substrat en silicium est une technique innovante en plein essor à même de répondre aux besoins croissants des détecteurs de nouvelle génération. La production de ces micro-radiateurs est cependant complexe et coûteuse. Le CPPM a démarré une R&D sur de nouveaux procédés de fabrication permettant d'abaisser les coûts de production.

Ainsi, alors que le collage des plaques en silicium est une étape particulièrement critique et coûteuse de la chaîne de fabrication, le CPPM en partenariat avec le laboratoire Femto-ST (CNRS-Besançon) met au point un procédé de collage innovant basé sur la thermo-compression avec des couches minces intermédiaires. Cette R&D permet au CPPM de développer une expertise dans les procédés de fabrication des micro-canaux ainsi que des capacités de tests.

Ce savoir-faire s'inscrit dans la continuité des savoir-faire présents au CPPM, déjà engagé dans la fabrication de détecteurs en silicium ainsi que dans la conception de systèmes

de refroidissement. Utiliser les techniques innovantes développées au CPPM au service d'un projet d'envergure comme le détecteur de vertex prévu pour l'Upgrade II de l'expérience LHCb, permettra au CPPM d'asseoir une compétence certaine dans le domaine du refroidissement micro-fluidique complémentaire à celle développée dans d'autres laboratoire de l'IN2P3 (LAPP, LPNHE).

3 Acquisition à très haut débit

L'augmentation de la luminosité instantanée introduit des phénomènes de saturation dans les *triggers hardwares* de LHCb. Une façon élégante de traiter ce problème est de transférer les données de toutes les collisions vers une ferme de serveurs où celles-ci sont reconstruites, puis sélectionnées en temps réel. L'architecture de la ferme est hétérogène (CPU, GPU) et la reconstruction est effectuée en une seule fois avec les précisions ultimes.

Cette architecture logicielle est très flexible et permet d'implémenter des algorithmes de sélection optimaux. Un élément clé de ce type d'architecture est l'électronique qui interface les sous détecteurs afin d'assembler les données d'une collision. Dans l'Upgrade I de LHCb, la première étape est assurée par la carte au format PCI Express développée au CPPM : la carte PCIe40. Cette carte est suffisamment générique pour avoir été réutilisée avec un rôle similaire dans les expériences Alice, Belle II et mu3e.

La luminosité envisagée pour l'upgrade II requiert une augmentation des performances d'un facteur ~ 10 par rapport à la carte PCIe40, ce qui n'est pas encore atteignable avec la technologie actuelle. Il est proposé d'atteindre cet objectif en deux phases.

A l'horizon 2026 (LS3), une augmentation de la bande passante d'un facteur 4 peut être obtenue en utilisant les FPGA Agilex d'Intel qui seront disponibles en 2022. La carte PCIe400 est en cours d'étude par un groupe élargi de laboratoires incluant le CPPM, le CENBG, l'IJCLab, le LAPP et le LPC Caen. Elle pourra acquérir un volume de données de 400 Gbits/s et les pousser vers la mémoire des serveurs par accès direct à travers un bus PCIe à 400 Gbits/s. La puissance de calcul du FPGA utilisé sera également augmentée d'un facteur 12, notamment en augmentant la fréquence de la logique à 640 MHz. Les algorithmes bénéficieront aussi d'une mémoire intégrée de 32 Go, ouvrant la voie à l'implantation d'algorithmes neuronaux ou bien permettant l'implémentation d'une interface 400 Gigabit Ethernet (GbE) pour laquelle une importante capacité de bufferisation est nécessaire.
A cette époque, les données des détecteurs arriveront sur des liens sériels LpGBT à 10 Gbit/s, développés au CERN. La carte PCIe400 sera équipée de 40 liaisons sérielles bidirectionnelles ayant chacune une bande passante maximale de 28 Gbit/s dans chaque direction. Cette montée en bande passante permettra d'acquérir la maîtrise des liaisons sérielles à très haut débit et de s'adapter aux développements des liens sériels étudiés au CERN, partenaire de la carte PCIe400.

À l'horizon 2030 (LS4), une seconde version, la carte PCIe800 multipliera les performances par un facteur deux. Elle intégrera aussi une interface réseau ou les données acquises transiteront cette fois par un Ethernet 800 Gbits/s, ce qui simplifie beaucoup l'*event builder*.

Par ailleurs, ce type de carte est capable de distribuer des horloges très précises aux front-ends. La carte actuelle l'effectue avec une précision d'environ 100 ps. L'upgrade II requière une précision encore plus grande, de l'ordre de 15 ps ou moins, une caractéristique déjà en cours d'étude pour la carte PCIe400.

Les augmentations de vitesse et de puissance de calcul précitées constituent de réels défis technologiques. Il s'agit de multiplier en quelques années les débits sériels par un facteur entre 10 et 20. Rappelons que la carte PCIe40, fonctionnait à 5 Gbits/s par lien, même si elle était conçue pour tourner à 10. La nouvelle carte PCIe400 devra gérer des vitesses de 112 Gbits/s par lien au niveau de l'interface 400 GbE. Cela impose une maîtrise très fine des phénomènes d'intégrité du signal. Également en termes de refroidissement, les technologies employées requièrent l'injection de courants compris entre 100 et 150 Ampères dans le coeur du FPGA. Il va sans dire que le refroidissement est également un point critique. La maîtrise de l'ensemble de ces techniques positionnera l'IN2P3 dans un cercle très restreint de développeurs, ce qui pourra donner un avantage prépondérant lors des prises de responsabilité au sein des expériences.

L'élargissement de l'équipe de développeurs mentionné précédemment souligne l'intérêt des différents laboratoires pour ces techniques d'acquisition très innovantes. Il permettra par ailleurs de diffuser un savoir-faire bien rôdé en matière d'acquisition à haute vitesse, de suivi de production, de développement de logiciels de traitement et de contrôle qui ont été élaborés avec succès dans le cadre de la carte PCIe40.

Enfin par sa généricité, la carte PCIe400 est susceptible de répondre aux besoins de nombreuses expériences, que ce soit dans le domaine de la physique des particules, mais aussi celui de l'astroparticule ou des applications médicales.

4 Calcul parallèle temps réel

Le système actuel de calcul en temps réel de LHCb utilise 200 cartes GPU et presque 4 000 serveurs CPU pour traiter 32 térabits de données par seconde, avec une consommation de $\sim$1 MW. En revanche, le futur détecteur LHCb Upgrade II posera le défi de traiter $\sim$200 térabits de données par seconde, en réduisant leur volume par un facteur $\sim$ 1 000. Malgré les avancées technologiques industrielles attendues au niveau des prix, performance et consommation énergétique de calcul, redimensionner le système actuel ne suffira pas.

Pour relever ce défi, il faudra maîtriser les technologies de calcul parallèle de façon optimale, ce qui permettra de débloquer toute leur capacité. De plus, il faudra probablement adopter une architecture de calcul hybride. En effet, une seule architecture ne sera pas optimale pour tous les besoins, car les différentes étapes de traitement des données impliquent des algorithmes et des logiques assez différents. Il s'agit donc de mettre en place un travail pionnier, cohérent et synergique d'une équipe mixte de chercheur.e.s et d'ingénieur.e.s pour :

1. Évaluer les différentes technologies de calcul parallèle qui sont en train d'être développées, pour comprendre leurs points forts et faibles et leur utilisation optimale.

2. Développer des moyens efficaces de transfert des données et de répartition du calcul entre des architectures différentes, mais également des algorithmes capables d'optimiser le coût et la consommation énergétique du système global.

3. Concevoir et mettre en place des algorithmes nativement parallèles pour les étapes individuelles du système (par exemple la trajectographie, la reconstruction du calorimètre, la sélection des événements).

4. Développer les outils de maintenance et gestion qualité de ce système de calcul complexe et hybride, capables d'assurer la qualité et la fiabilité des données traitées.

La communauté LHCb France a bien préparé le terrain pour mener ce projet innovant, vers lequel elle souhaite pousser ses ambitions. D'abord, elle a été protagoniste de l'organisation dans le cadre d'un projet de la communauté de calcul en temps réel de LHCb. Ensuite, elle a proposé, fait accepter, et mis en œuvre le nouveau traitement des données basé sur des cartes GPU. Pour cela, elle a développé avec des partenaires internationaux Allen, un système de reconstruction et sélection des évènements en temps réel sur GPU qui est versatile, évolutif et suffisamment générique pour pouvoir potentiellement être utilisé par d'autres expériences. Ce travail a été accompli en fusionnant les compétences des plusieurs laboratoires de l'IN2P3 (CPPM, IJCLab, LAPP, LPNHE) en termes d'algorithmes de reconstruction des détecteurs, de conception de systèmes de déclenchement et d'intégration dans les systèmes d'acquisition des données. L'intégration des ingénieur.e.s de calcul dans nos équipes s'est révélé importante, et est une des lignes d'actions qu'il faudra intensifier pour le futur. Des efforts sont aussi en cours pour participer au développement de logiciels capables de débloquer et utiliser la puissance totale des nouveaux centres de calcul scientifique Exascale.

Les compétences acquises par ces équipes permettront non seulement de relever le défi posé par le traitement des données du futur détecteur LHCb Upgrade II, mais aussi de consolider et développer une communauté IN2P3 de chercheur.e.s et ingénieur.e.s avec l'expertise nécessaire pour faire face aux défis du calcul scientifique dans l'avenir, qui concerneront non seulement le domaine de la physique aux accélérateurs mais la physique des deux infinis en général.

Plans for LHCb Calorimeter LS3 Consolidation

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Abstract

This document describes the evolutions of the project LHCb ECAL2 presented initially in the Letter of Intend [1] written by the French LHCb groups for the LHCb Upgrade II. The changes involve mainly the consolidation work which is planned for the LHC Long Shutdown 3 (LS3) scheduled for $2026-2028$. The French LHCb teams are involved in the electronics and the mechanics for the ECAL.

1 Introduction

The goal of the Phase II Upgrade for the LHCb Electromagnetic calorimeter (ECAL) is to replace the entire ECAL with new modules. In order to work under the large pile-up conditions expected for that upgrade, it is mandatory to add to the ECAL the possibility to measure the time of arrival of the particles with a precision better than 20 ps. This will allow to distinguish particles coming from different interactions in the same bunch-bunch collisons. New modules are being designed to fullfill this requirement, together with the associated readout electronics, project in which the Clermont-Ferrand and Orsay LHCb teams are involved.

The 32 innermost modules (closest to the beam, corresponding to 300 channels) of the current ECAL will be completely inefficient because of irradiation damage at the end of Run 3 (2022–2025). They must be then replaced during LS3 (2026–2028). The strategy is to replace these modules by the new modules designed for the Upgrade Phase II, planned for installation in LS4 (2033–2034), in a wider area than only this central part. The plan is then to replace 176 modules close to the beam. This corresponds to 3500 channels. The existing modules in the outer areas of the current ECAL will be kept and rearranged in a rhomboid shape. The geometry of the detector foreseen for LS3 is shown in Fig. 1. The new modules correspond to the red and orange areas, the current existing modules correspond to the green and blue areas. As a comparision, the current ECAL contains 6000 channels and the detector foreseen for the Phase II LS4 upgrade will contain 30000 channels (because modules will also be split longitudinally for that upgrade, doubling the effective number of channels).

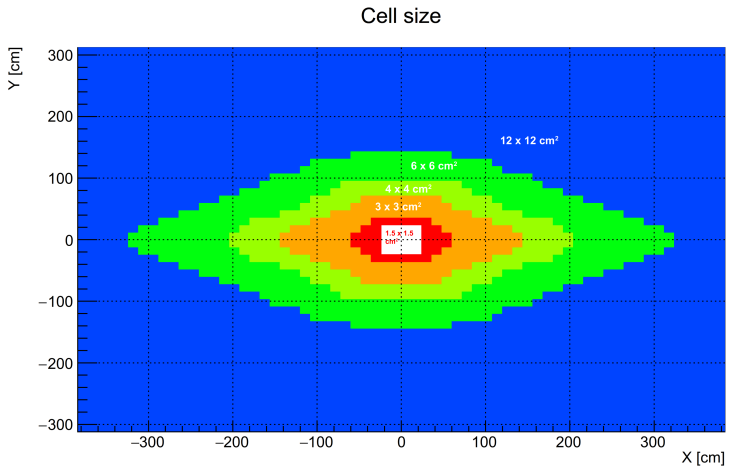

Fig. 1: Layout for ECAL in LS3

The projects in which French LHCb teams are involved for the LS3 consolidation phase are the Front-End electronics (Clermont-Ferrand and Orsay) and the mechanics (Annecy). The work for the mechanics was planned already to happen during LS3 for the entire upgrade of the ECAL and is described in Ref. [1].

2 Timing ASIC

The new modules that will be installed during LS3 will also provide precise timing measurement, even if not strictly mandatory because the running conditions during Run 4 (2029–2032) will be the same as the current conditions where timing is not implemented. However, the LS3 consolidation provides a perfect setup to test in real conditions the precise time measurement that will be necessary for Run 5 (2035–2038). The goal is to have a Front-End electronics capable of measuring this time with $<$20 ps resolution and to equip the new inner modules with it.

To achieve this goal, the French LHCb teams started to develop an ASIC to measure the time, called SPIDER, since the beginning of 2022. This activity is funded by an IN2P3 R&T project of 50k EUR for the period 2022–2024. In parallel, another ASIC is being developed by the Barcelona LHCb group to measure the energy. This energy ASIC is mandatory to readout the new modules and is an evolution of the current ASIC that was already developed by the same group.

Since beginning of 2022, a group was put in place for the development of SPIDER, lead by Philippe Vallerand (IJCLab Orsay) and Samuel Manen (LPC Clermont-Ferrand). Electronics engineers from 4 IN2P3 laboratories take now part to the development in the framework of the IN2P3 R&T for a total of 5.7 FTE: IJCLab Orsay (1.3 FTE: Philippe Vallerand, Dominique Breton, Christophe Sylvia), LPC Clermont-Ferrand (2.8 FTE: Samuel Manen, Nicolas Arveuf, Richard Vanadaele, Guillaume Blanchard, Baptiste Joly), LPC Caen (0.8 FTE: Ludovic Alvado, Laurent Leterrier), IP2I Lyon (0.8 FTE: Edouard Bechetoille, Hervé Mathez). Test beams in 2022 at DESY and at the CERN-SPS, with the modules under development for the LS3 consolidation, validated the principle of the ASIC, based on waveform sampling in analog memories, and demonstrated that a resolution of the entire detection chain of less than 20 ps can be achieved.

The planning of the ASIC design and production is as follows:

1. 2022–2023: design and production of a first prototype
2. 2024: test of first prototype
3. 2024–2025: design and production of a second prototype
4. 2026–2027: production of ASIC to use for LS3 ECAL consolidation

All teams will participate a priori to the R&T project until 2024 while the IJCLab and LPC Clermont-Ferrand teams will continue the development at the end of the R&T project until completion. If potential improvements are found during the Run 4 operation, they will be included in the final version of the ASIC that will equip the entire detector for Upgrade Phase II.

Concerning the budget, the production of the first prototype and the preparation of the test bench are covered by the IN2P3 R&T project (50 kEUR). A budget of 35 kEUR is needed for the production of the second prototype. In order to equip the 3500 channels during LS3, 500 chips are needed, for a total cost estimated to 50 kEUR for the production of them.

3 Front-End electronics

The design of a new Front-End board is mandatory to readout the new channels that will be installed during LS3. The function of the Front-End board is to host the two ASICs (energy and time), to process the information from these ASICs in a FPGA to compute the energy

and time of the particles in the ECAL, to format them and then send them to the back-end electronics for online and offline software processing. The back-end boards will be a new version of the PCIe40 board currently used to readout all LHCb detectors. It is being designed at CPPM Marseille and other IN2P3 laboratories for LS3, through the IN2P3 R&T project PCIe400.

This new Front-End board will be similar to the ones designed for the current calorimeter (first version built for Runs 1 and 2 and the upgraded version built for Run 3) which were designed by the French LHCb groups (ICLab Orsay, LPC Clermont-Ferrand and LAPP Annecy for the first version, IJCLab Orsay for the second version). The IJCLab electronics department and LHCb team intend to lead the development of the new Front-End board in order to maintain the strong involvement of the team since the beginning of LHCb in that project. It will also allow to keep the leadership on the Calorimeter electronics within the collaboration.

The project started at the end of 2022 and is lead by Christophe Beigbeder. The person-power resources needed will be provided by IJCLab Orsay: for the duration of the project, 1 FTE for the design of the board and for the organisation of the project (Christophe Beigbeder, Jihane Maalmi) and 1 FTE for the DAQ software for the tests of the board; for specific periods, 1 FTE for the CAO of the board during the prototyping phase, 1 FTE for the board cabling of the prototypes, 1 FTE for the installation and the cabling in the experimental area during LS3. Since it is a long term project, the recruitement of a ingénieur de recherche with broad competencies in electronics will be necessary in order to design the final versions of the boards for LS4. Possible collaborations with other groups, in France or in other countries will be also investigated.

The planning of the Front-End board design and production is as follows:

1. 2023: design
2. 2024: first simple prototype to test with the first ASIC prototypes and simplified DAQ
3. 2025–2026: prototypes to test the interface with the new backend boards
4. 2027: production of the 110 boards
5. 2028: tests of the production, installation at CERN and commissioning

The boards produced will handle 32 channels per board. For the LS4 upgrade, to equip the entire detector, a new version of the board will be designed to handle 64 channels per board and to be interfaced with the final version of the backend board (PCIe400).

For the LS3 consolidation, 110 Front-End boards, 10 control boards and 10 readout boards will be needed. The corresponding cost, including spares and the design and prototyping phase is estimated to be 500 kEUR.

4 Conclusions

The radiation dose accumulated by the innermost modules of the LHCb Electromagnetic calorimeter imposes to replace them during the Long Shutdown 3 of the LHC. This is the occasion to replace them with new modules designed for the LHCb Upgrade Phase II in advance. New Front-End boards will have to be designed and built to read them out. Since these new modules will have good time measurement performances, it provides also the perfect possibility to test a new ASIC designed to measure the time in the ECAL already during Run 4.

References

[1] N. Allemandou *et al.*, Letter of Intent for LHCb Upgrade II (2022).