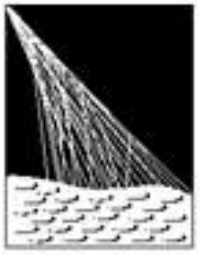


WP1- Technical Design Report 2015

R. Assiro, P. Creti, G. Marsella

Outline

- Specific requirements
- Design concept and solution selected
- Prototype test board design
- Test report and results on prototype
- Design Status

Specific requirements

The wp1 is in charge to design the analog PMTs processing signal. The new specific requirements are:

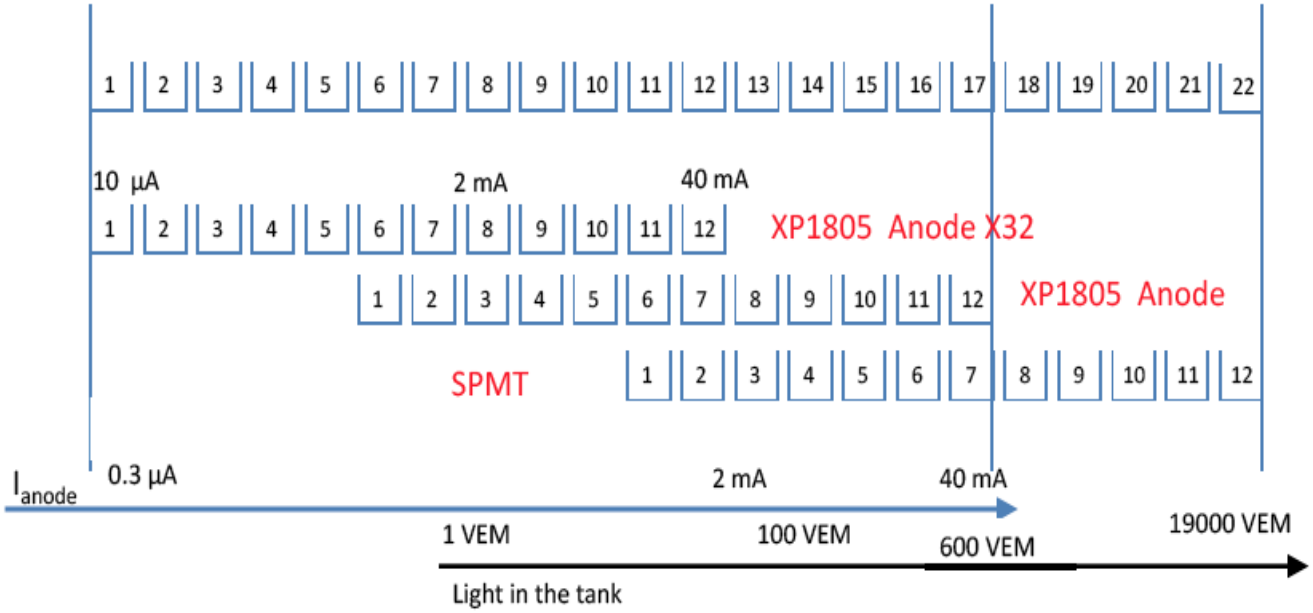
- 5x2 differential channels, low noise (0.5 LSB < 250 μV), 12 bit, and 120 MHz ADC converter
- Power < 0.5 Watt/channel
- 10 Low pass Filter (Bandwidth < 60 MHz)
- 3x2 channels to read the PMT anode signal and splitted in high (30 dB) and low (0 dB) gain + 4 single channels with possible different gain (1 Small PMT, 3 ASCII)
- Analog signal dynamic range: from 100 mV to -1900 mV (5% of dynamic reserved for the undershoot)
- 1 ms recovering time

Specific requirements

In the following scheme, the dynamic range of the new electronic is shown:

The dynamic range scheme will allow moving the trigger threshold two bits higher and increasing the current dynamic range by a factor of 32.

The gain of the PMTs will be kept the same as before, 3 10^5. The muon peak will be in channel 200. An additional small PMT (SPMT) will be used to extend the dynamic range.



The selected commercial ADC

ANALOG DEVICES

12-Bit, 125/105 MSPS, 1.8 V Dual Analog-to-Digital Converter

AD9628

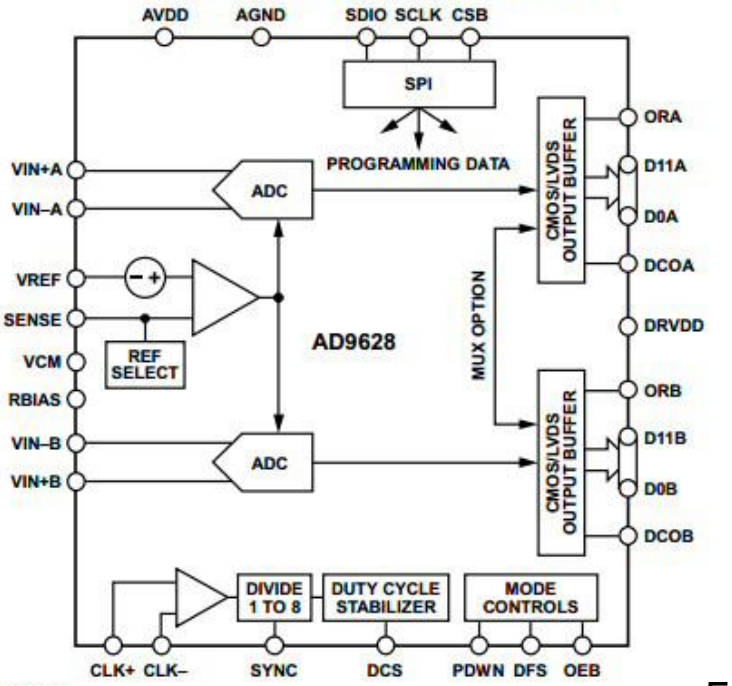
FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or LVDS outputs
- SNR = 71.2 dBFS @ 70 MHz
- SFDR = 93 dBc @ 70 MHz
- Low power: 74 mW/channel ADC core @ 125 MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.25 LSB
- Serial port control options
  - Offset binary, Gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Integer 1-to-8 input clock divider
  - Data output multiplex option
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock out with programmable clock and data alignment

APPLICATIONS

Communications

FUNCTIONAL BLOCK DIAGRAM

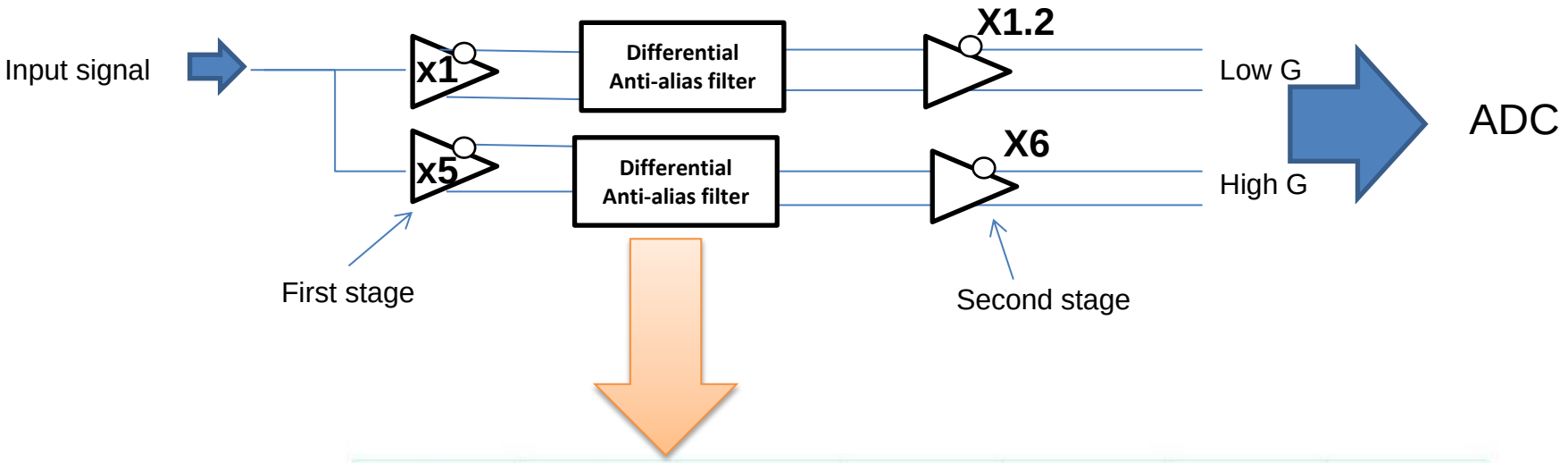


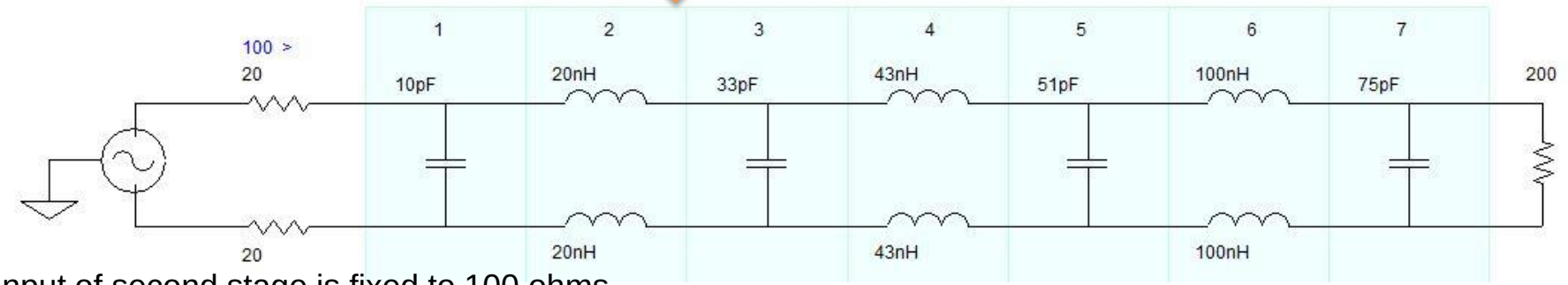
NOTES
1. PIN NAMES ARE FOR THE CMOS PIN CONFIGURATION ONLY; SEE FIGURE 7 FOR LVDS PIN NAMES.

Figure 1.

Design concept and solution selected

To obtain the requested performances various possibilities have been investigated. The idea is to split the PMTs anode signal in two channels: a 0 dB and a 30 dB channels. Filters for each channel will be implemented instead of a single filter for each anode to avoid to amplify the noise produced by the filters. The final adopted solution is the following:

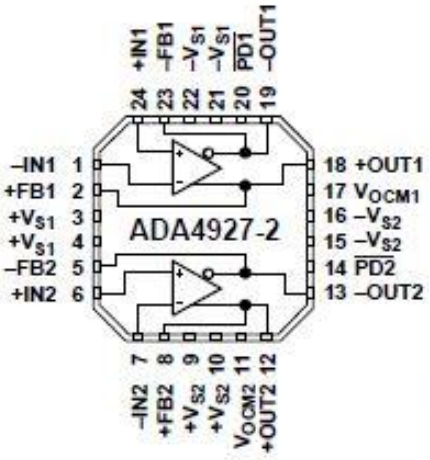




Input of second stage is fixed to 100 ohms
The filter is calculed by elsie 2.72 program with 20 ohm input impedance
The maximum filter attenuation (in low frequency) is -2dB

Design concept and solution selected

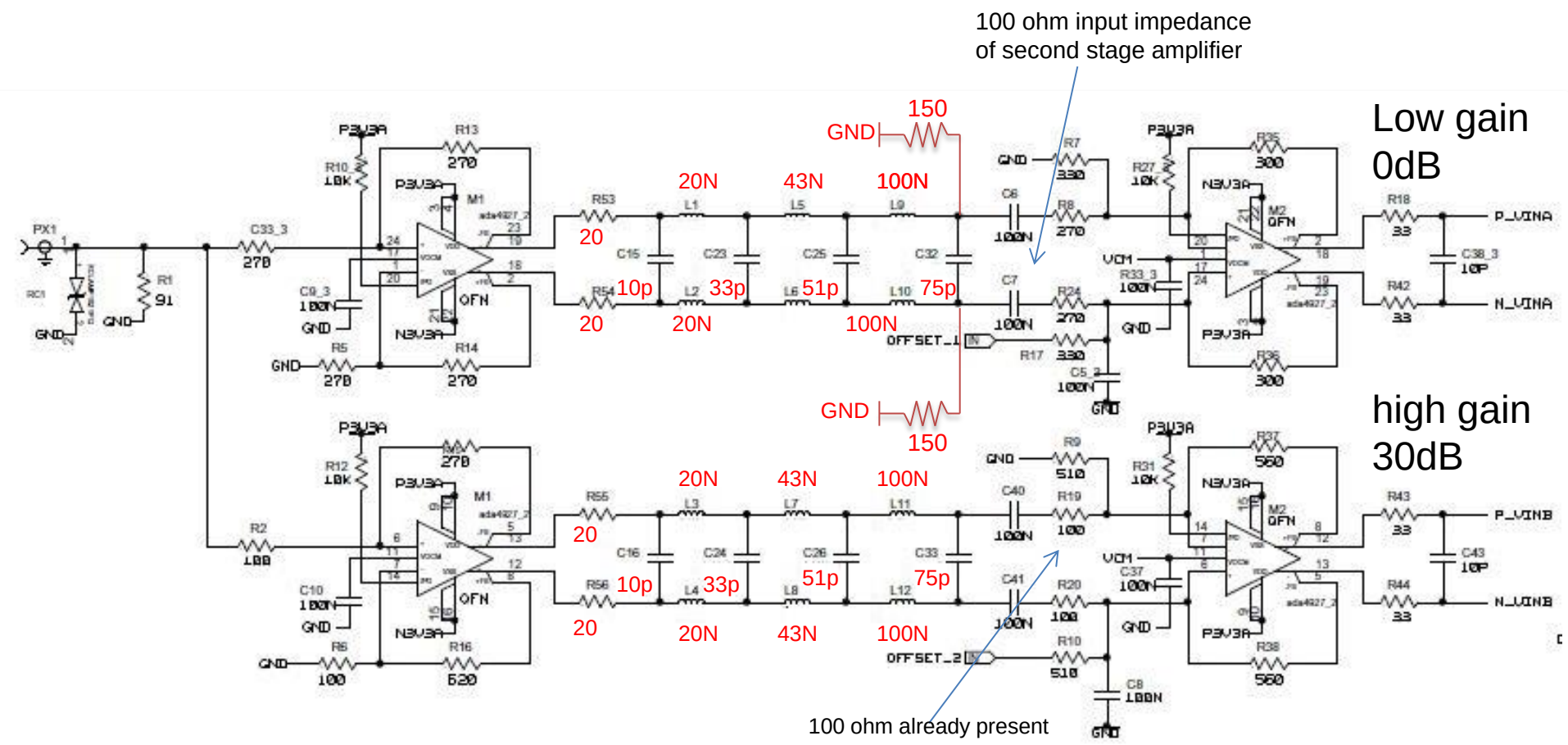
- Type 1 Input: The signal from the anode of the PMTs are splitted and amplified, by 0dB the low-gain channel and by 5dB the high-gain channel and made differential. This has been done using dual channel ADA4927 Operational Amplifier (OA). Then a 5 pole passive Low-band pass filter is implemented using inductances and capacitors. Finally the last amplification stage is implemented using the same ADA4927 OA obtaining a 0 dB and a 6 dB gain on low-gain and high-gain channel respectively. At that stage are also implemented the V_{CM}, the common mode voltage reference, and the offset generator to make the ADC working in the correct dynamic range (form 100 mV to -1900mV)
- Type 2 Input: The same solutions are adopted with the last 4 channels but with the possibility to split a single input on two channels or using two separated channels with the amplification tunable by the choice of the feedback resistors in both solutions. One of this will be used for the "Small PMT" and the other 3 for ASCII.

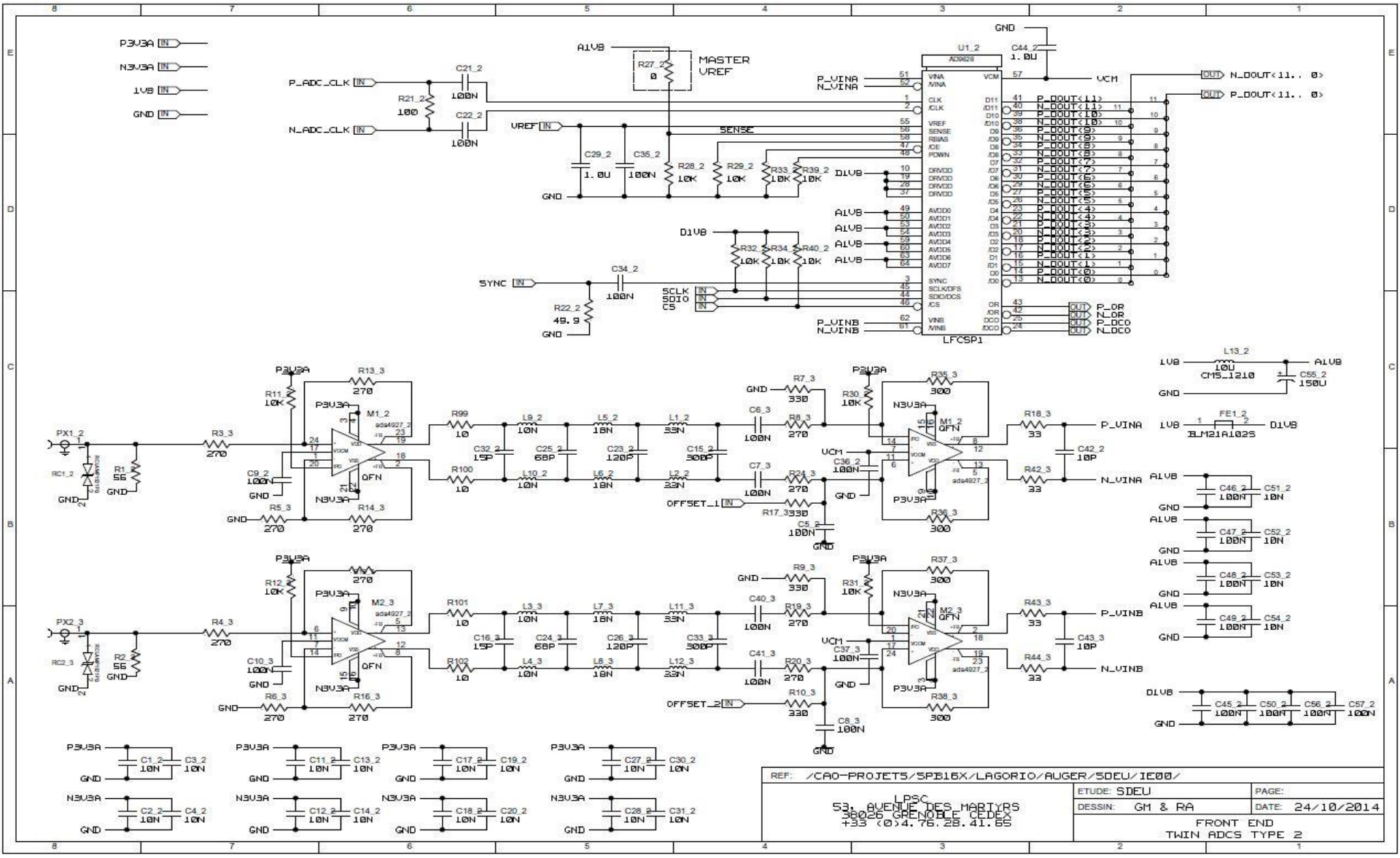


ADA4927-2 is the final Analog Device microchip chosen.
four stages, two microchips

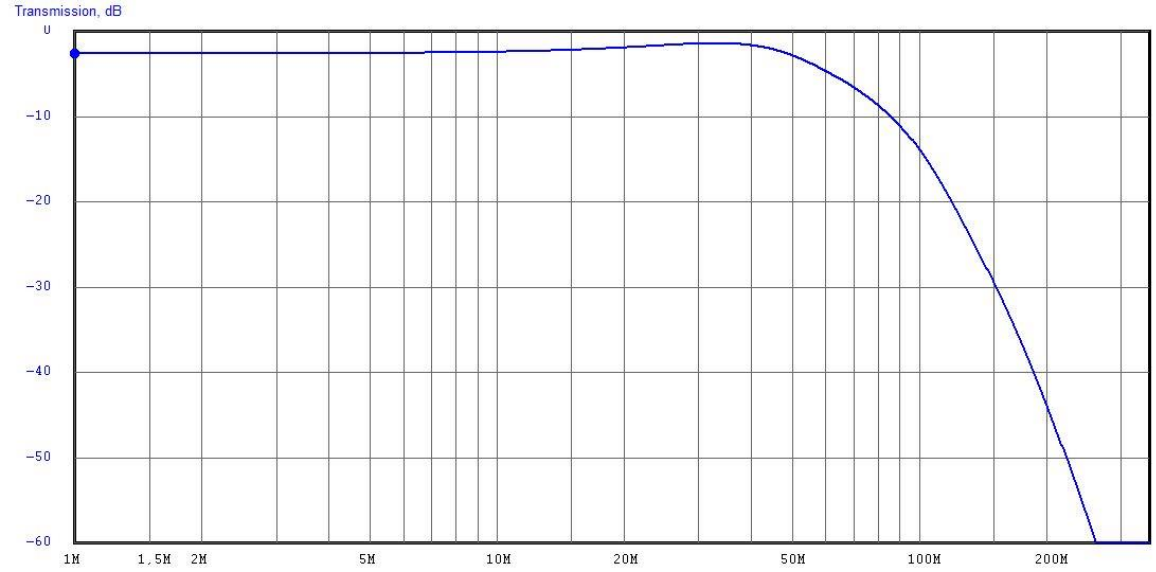
Features
Extremely low harmonic distorsion
Very Low noise 1.4nV /$\sqrt{\text{Hz}}$
Bandwith -3dB 2.3GHz
Differential line drivers

Type 1 input detail



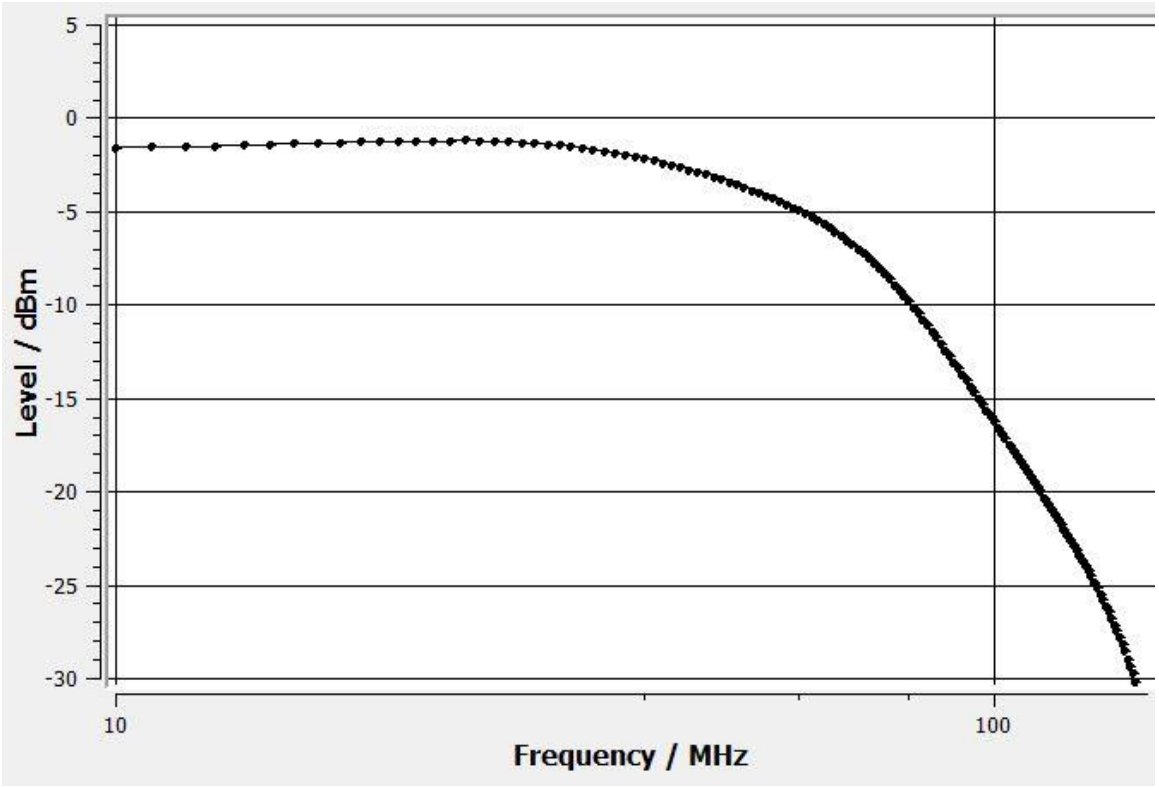


The offset can be supplied by a single generator and distributed on a common line to each ADC channel input. Due to the importance of the stability of those values, the possibility of activating dedicated offset generators for each channel has been implemented by mean of Zero resistors.

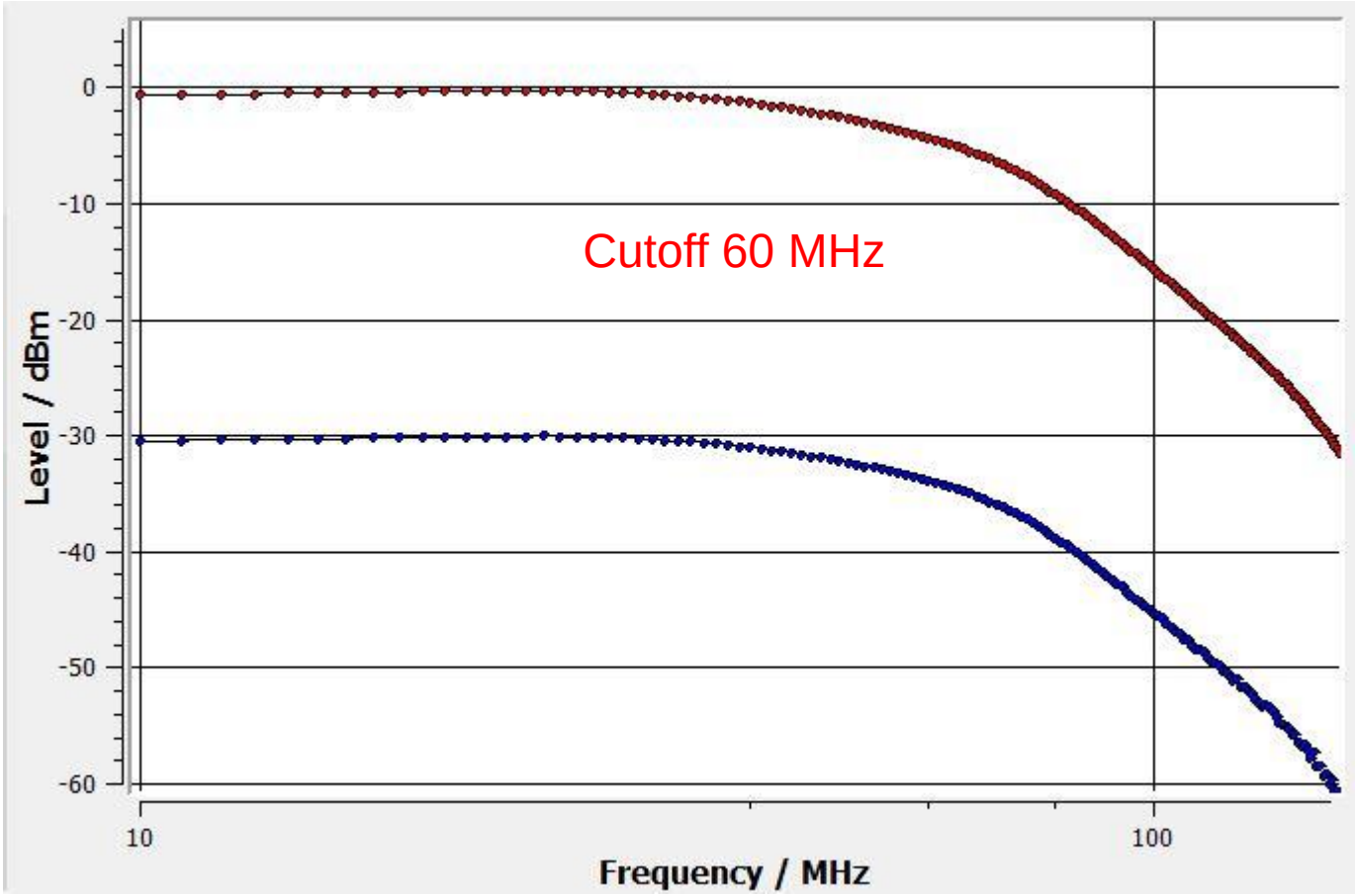


Filter simulated

Filter tested



Output of twin channels (high gain and low gain) on sweep of frequency(input signal -30dBm)

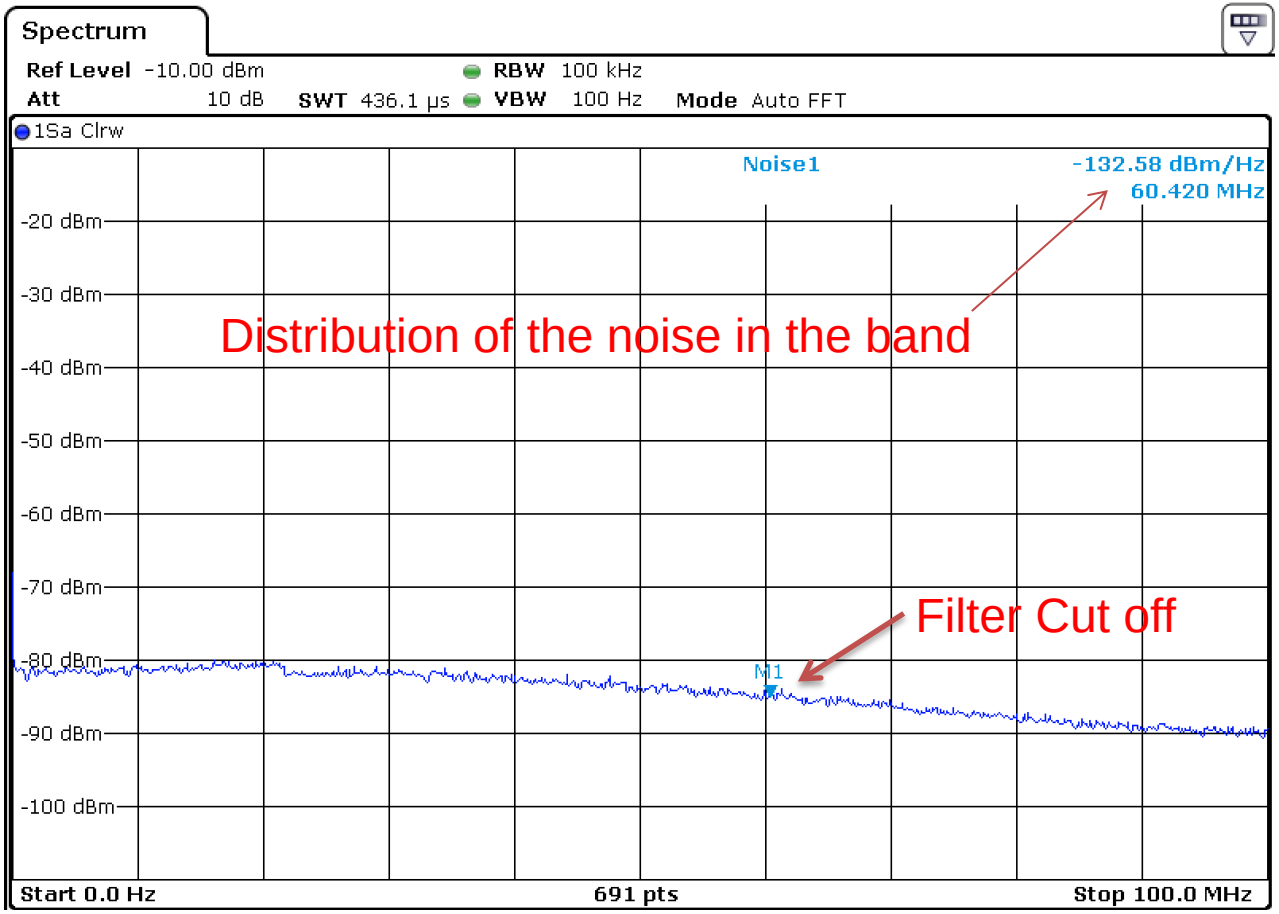


Noise and Power measurements

High gain channel Noise level =

-132 + 10*log 60000000 = -54 dBm

NOISE LEVEL = 446uV RMS



Work Package	Functions	Devices	Maximum current (mA) / power supply (V) / Devices: FPGA 1	FPGA 1,2	FPGA 1,8	FPGA 3,3	Slow C 3,3	Analog 3,3	Analog -3,3	GPS 5	USB 5	Radio 12	PMT 12	Max Power / Devices (mW)	Nb.	Powers	Powers / WP
WP1	Front-End	Anti aliasing filter (TBD)						0	0					0	3	0,00	4216,38
		Low-gain path filter proposal						2,8	2,8					18,48	3	55,44	
		High-gain path filter proposal						2,8	2,8					18,48	3	55,44	
		Differential amplifier (2xADA4927-2)						82	82					541,2	5	2706,00	
		12 bits ADC 120MS/s (Twin AD9628) proposal			155,5									279,9	5	1399,50	

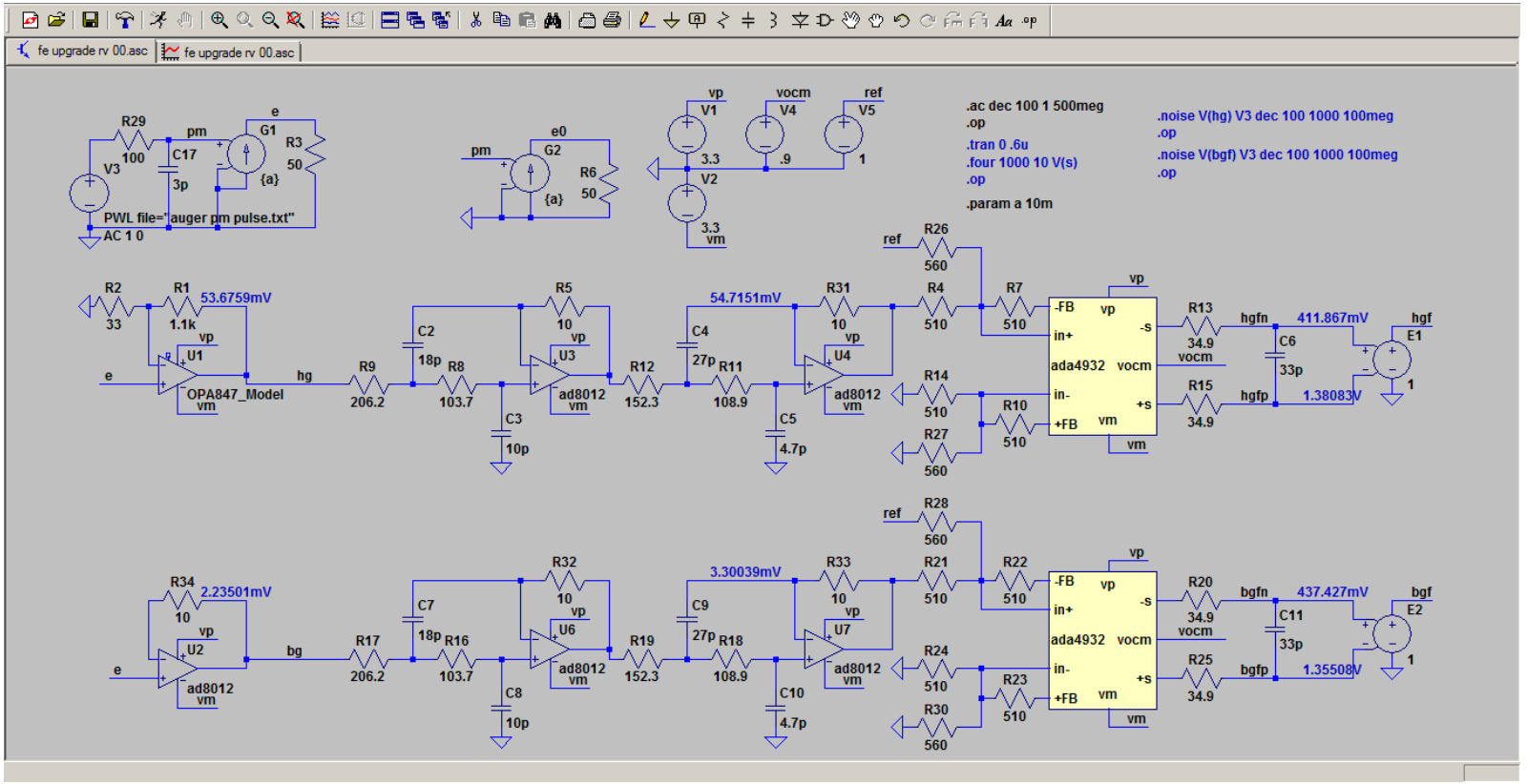
541mW
For each channel

Alternative upgrade scheme

Hervé Lebbolo

High gain

Low gain

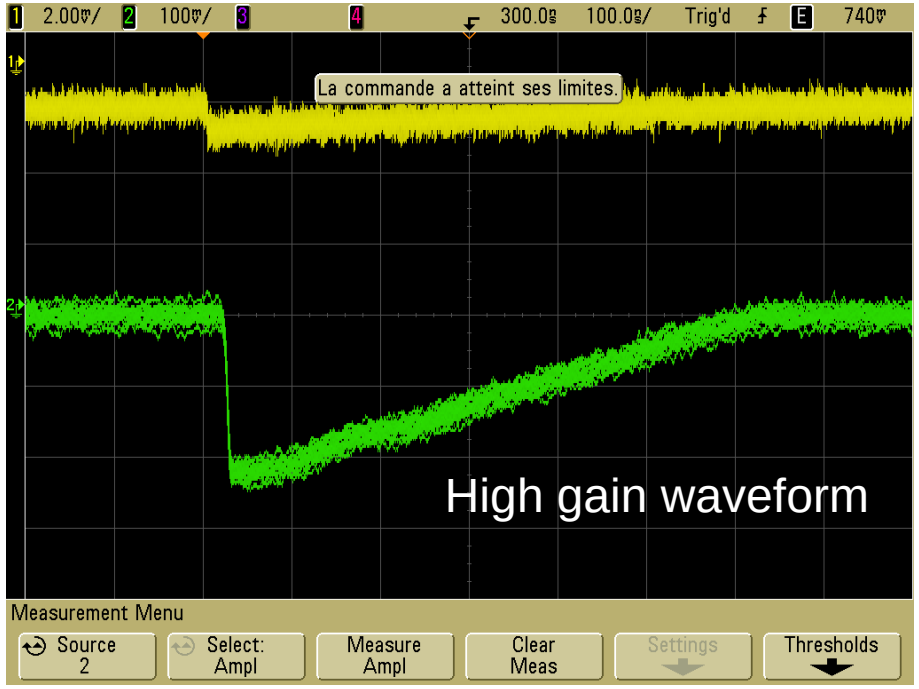


Each channel is made of one positive gain amplifier followed by a 4th order active filter and a unity gain differential ADC buffer ADA4932.
High gain is made with single low noise aop opa847
Low gain and active filter with aop AD8012

Alternative scheme status

Hervé Lebbolo

<u>Simulations :</u>
High gain total noise : 430µV rms
Low gain total noise : 90µV
Total power consumption : 180mW

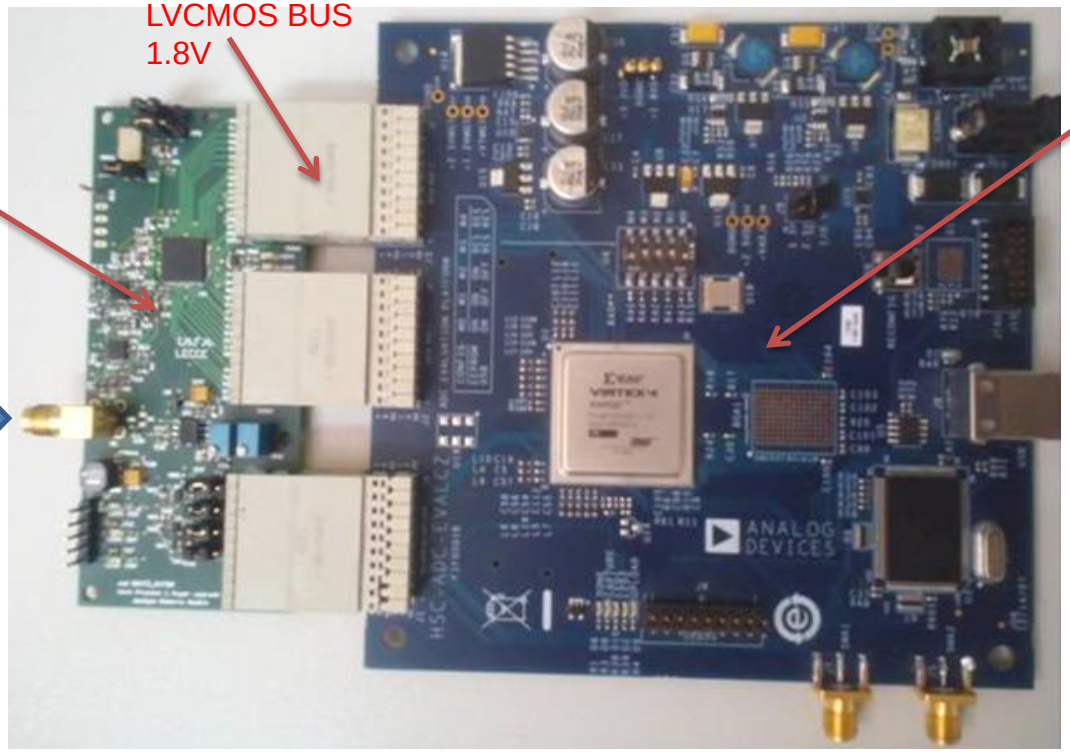


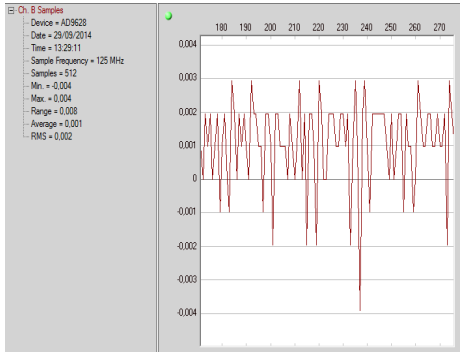
First tests performed without differential ADC buffer :

High gain noise : less than 360µV rms
Low gain noise : less than 180µV rms
Power consumption : ~170mW

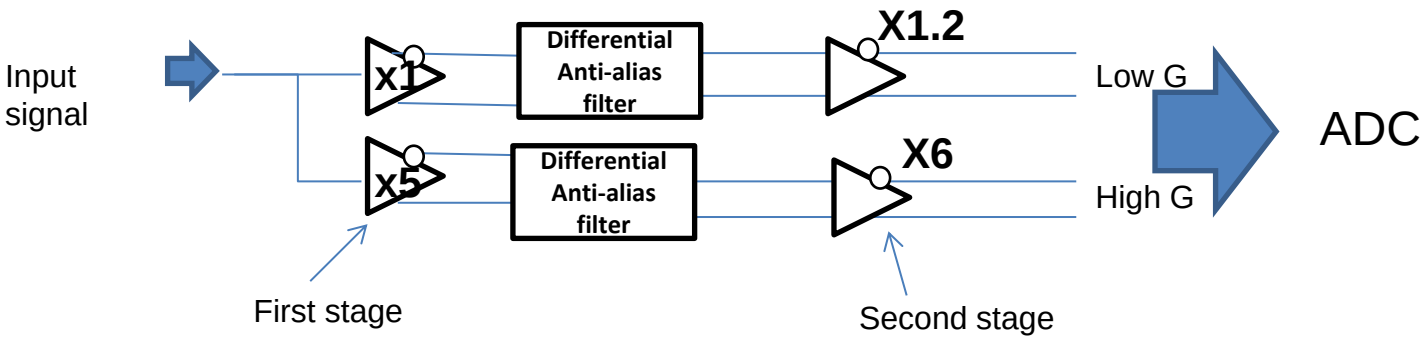
Next step : test of a complete dual channel with ADC and differential buffer.

Working Progress 1 - Lecce Prototype 1

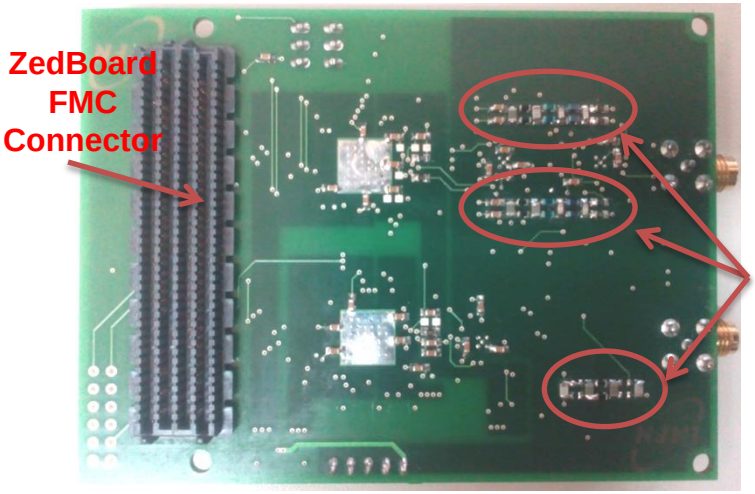


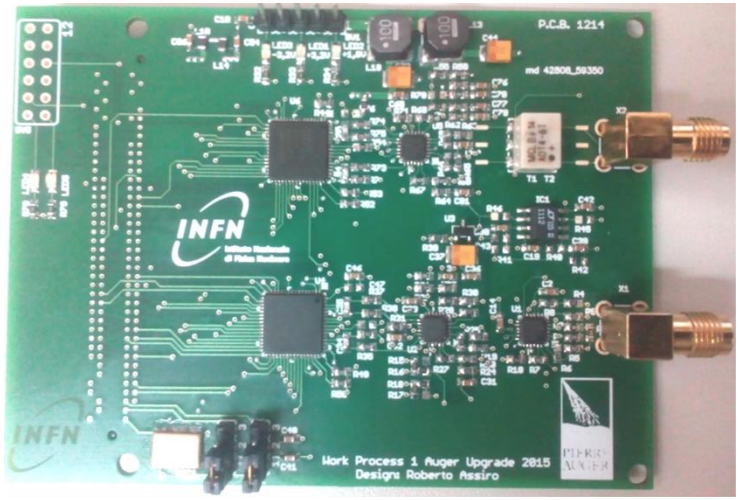


Front-end



Working Progress 1 - Lecce Prototype 2
Twin couple of ADC channels in two differents front-end solutions



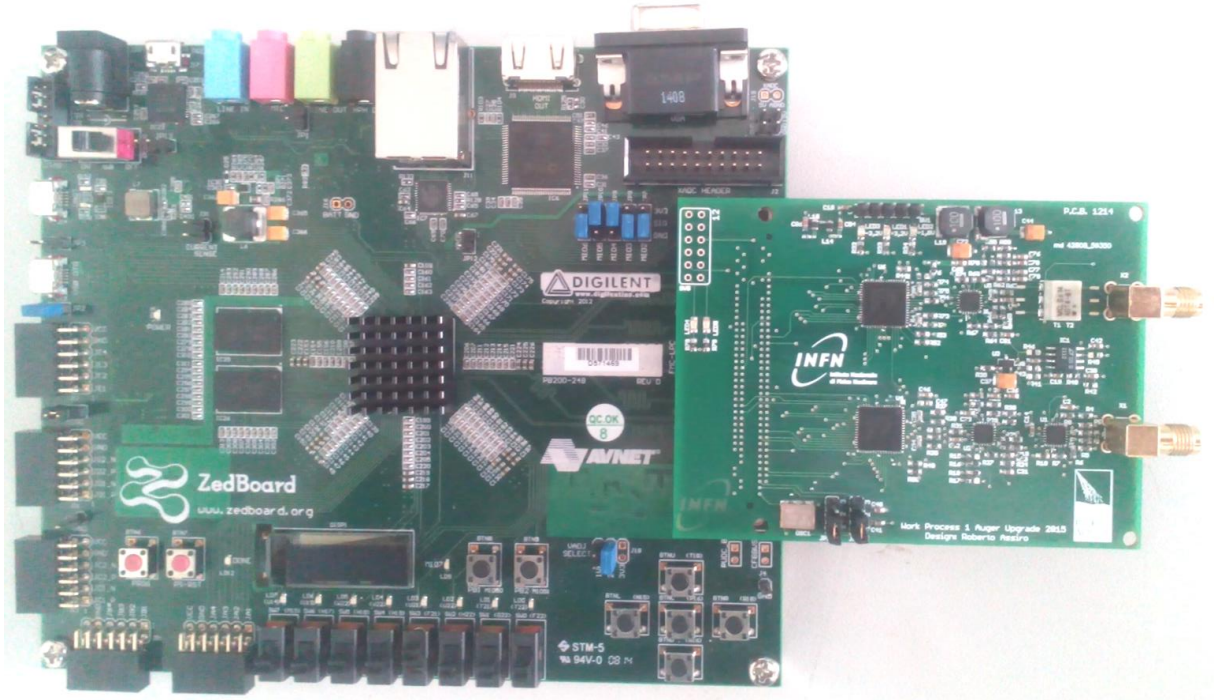


Channel2
(New solution)

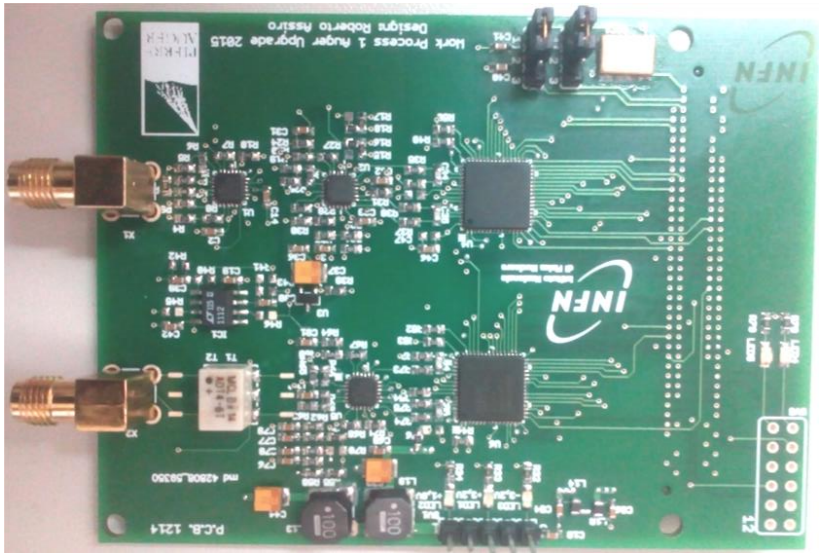
Channel1
(Actual solution)

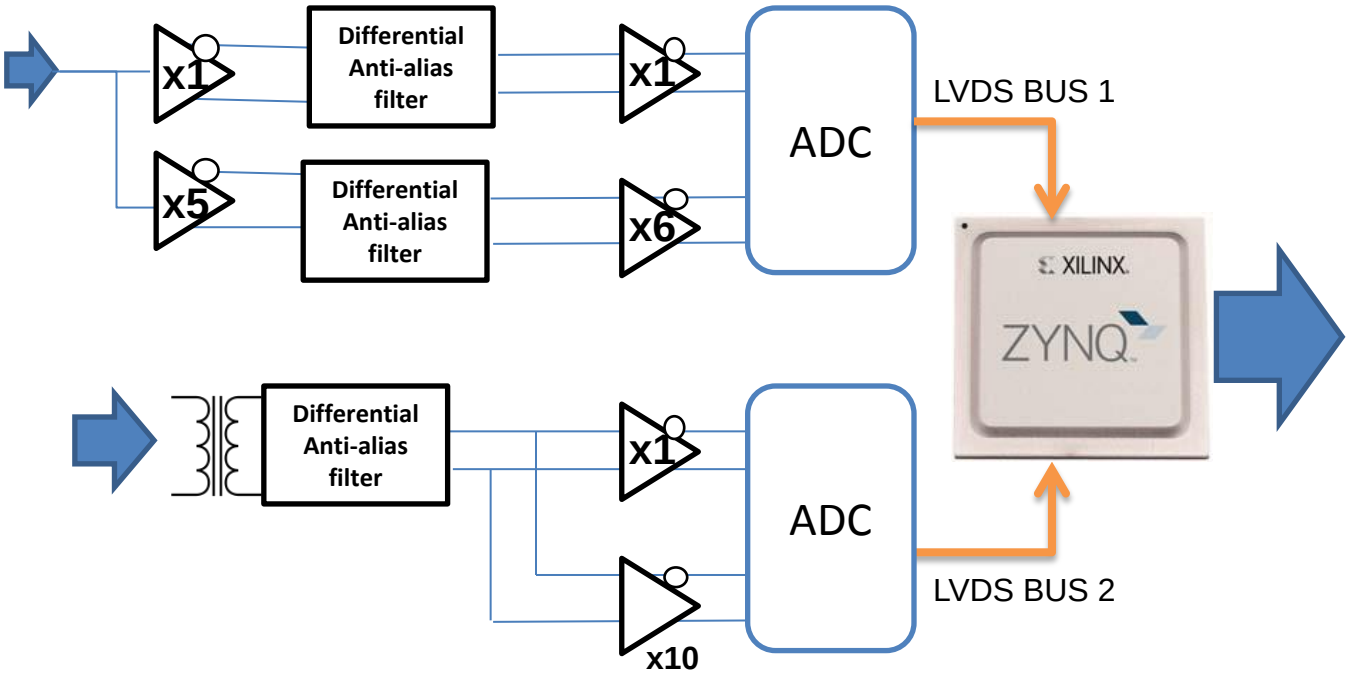
Targets for this prototype:

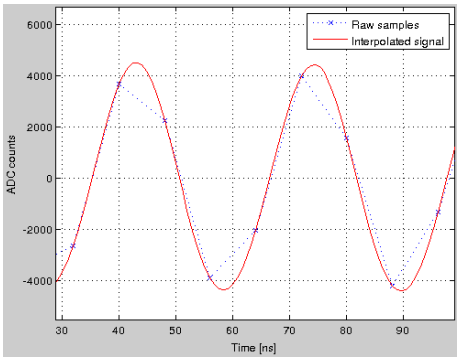
- Read ADC data by LVDS BUS of the Zynq
- Set the ADC via SPI interface
- Measures of noise of the front-end
-Test for the alternative solution of front –end
- Acquisition of PMT signal by Zynq

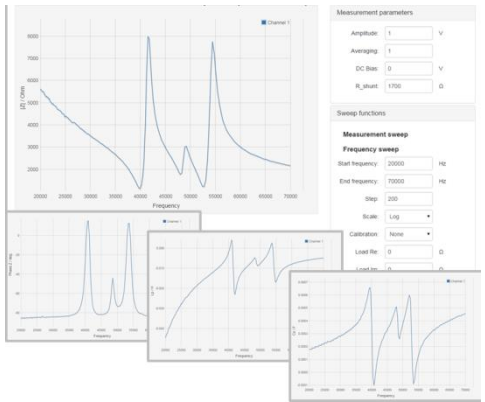


Working Progress 1 - Lecce Prototype 2









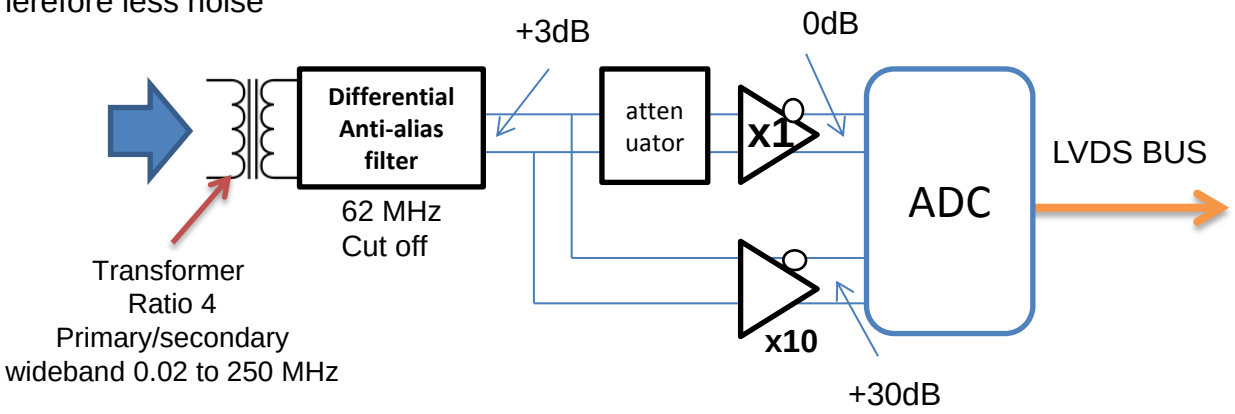
Front-end alternative solution

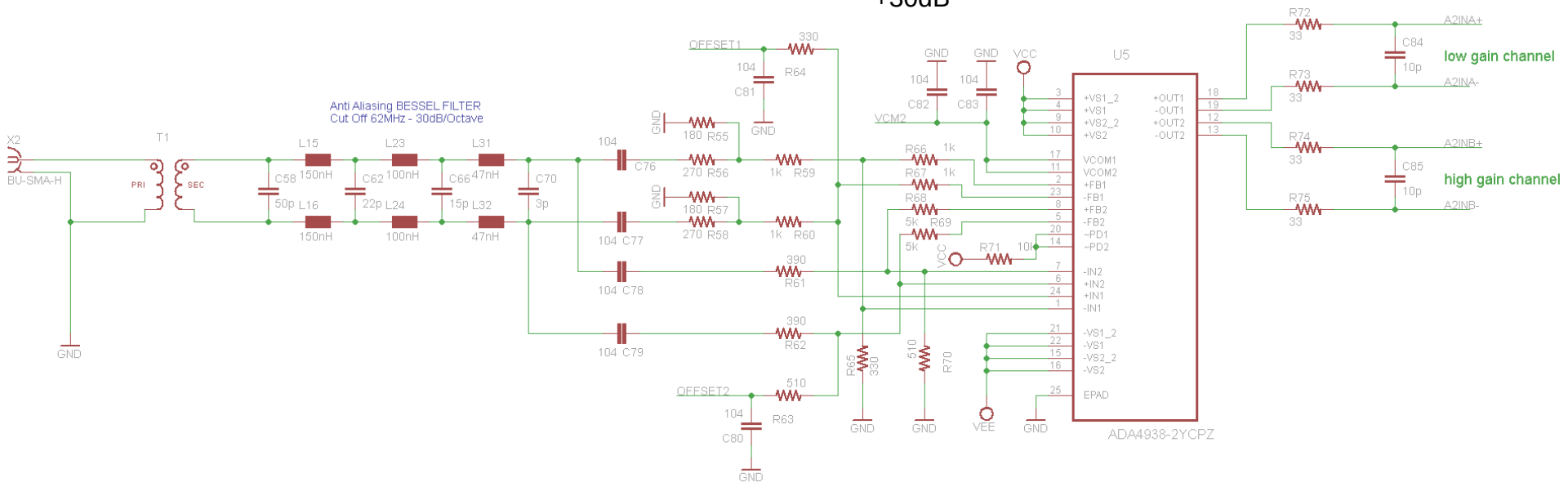
Features:

-Less power consumption. One stage for each channel

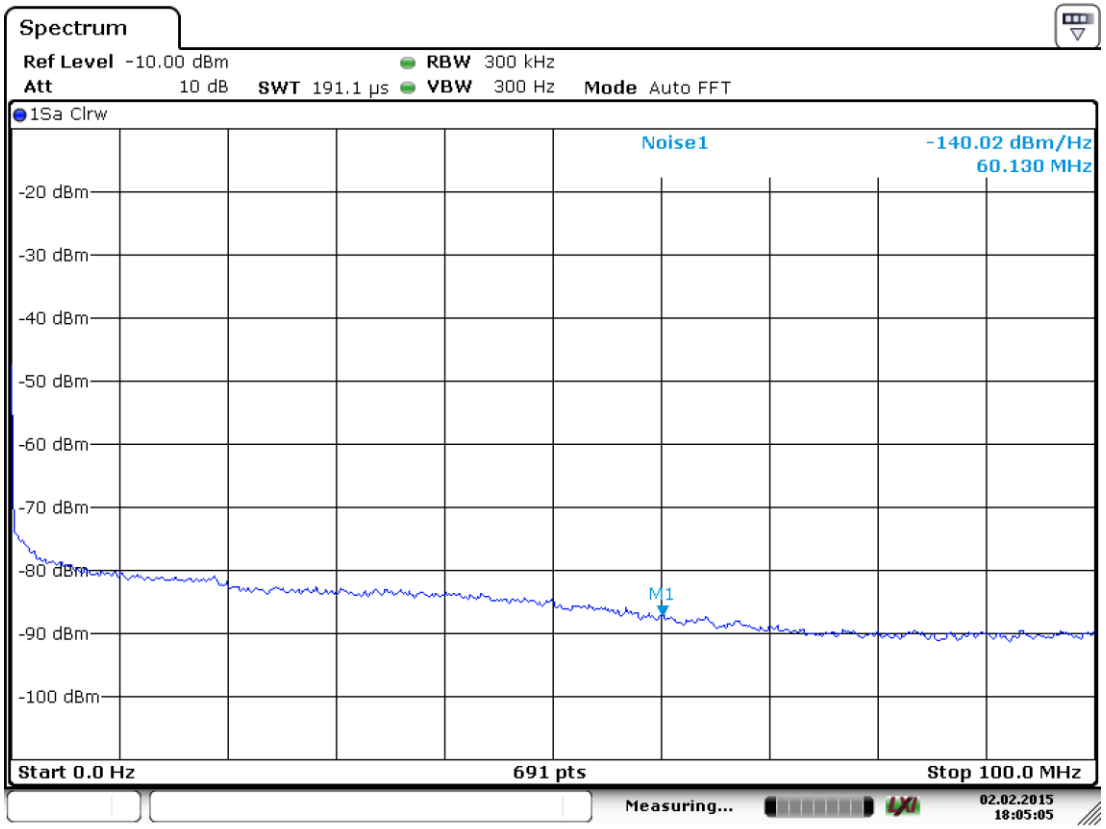
- One anti alias filter for both channels
- Less gain for each amplifier and therefore less noise
- Wideband 0.02 to 62 MHz (transformer low cut off)

In this solution we utilize the transformation ratio of the isolation transformer to get less gain of the amplifier stages and therefore less noise

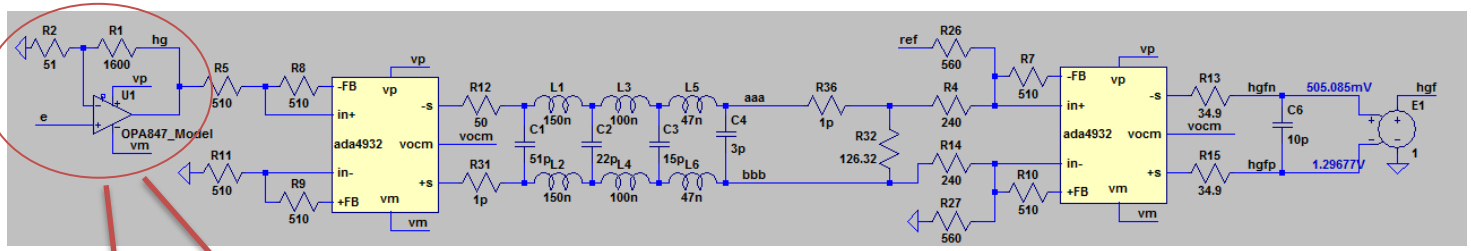


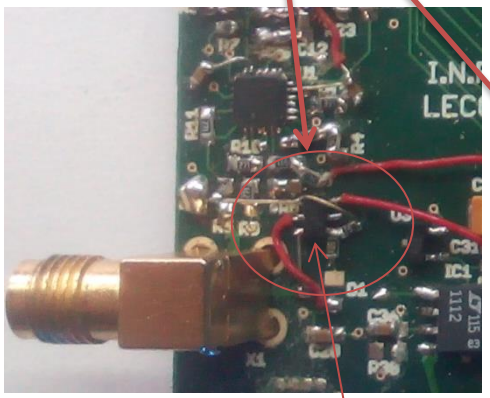


- Backup Slides



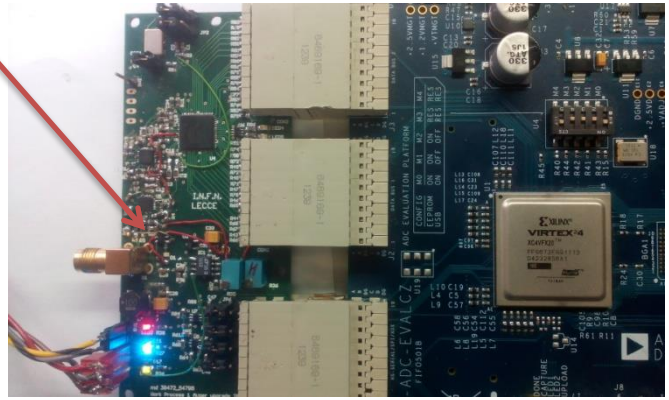
Measures of high gain channel simulated from Hervè Lebbolo



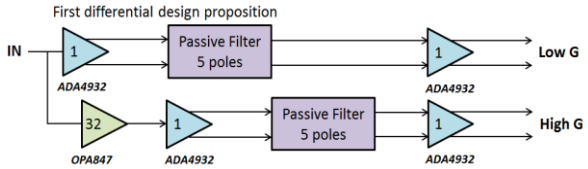


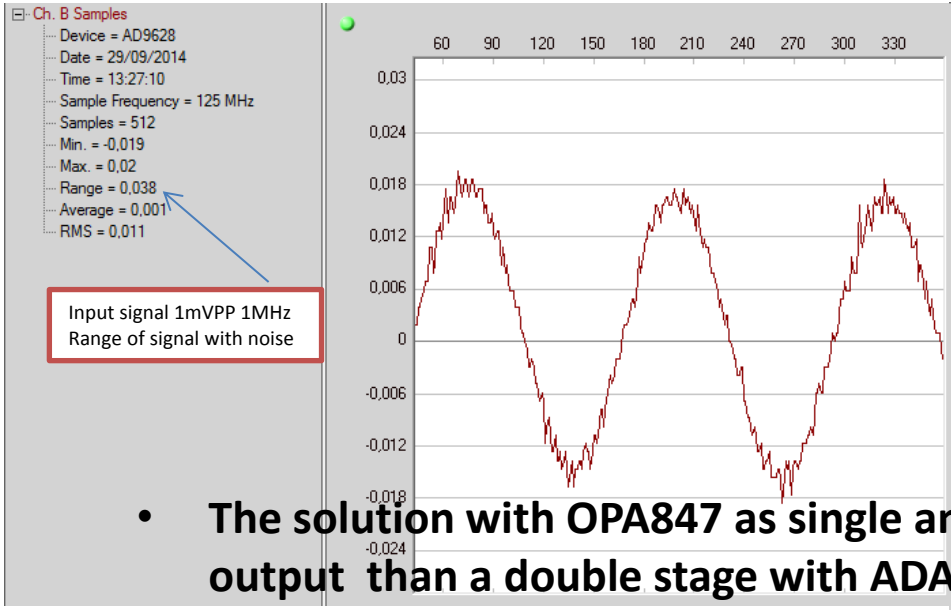
OPA 847

Modifications of front-end prototype board

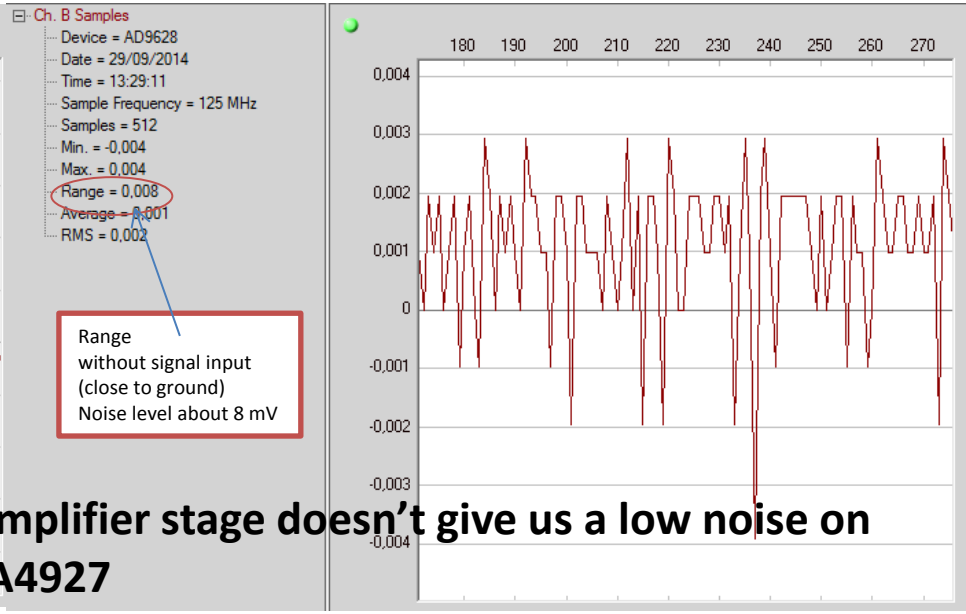


The proposed solution with one stage amplifier OPA847 with 32db of gain in my measurement does not change the output noise from our first Solution. Less than factor 2
It was tested with ADA4927 instead of ADA4932. May be it could be better to convert in differential (our solution) for a low noise interference before the amplification.





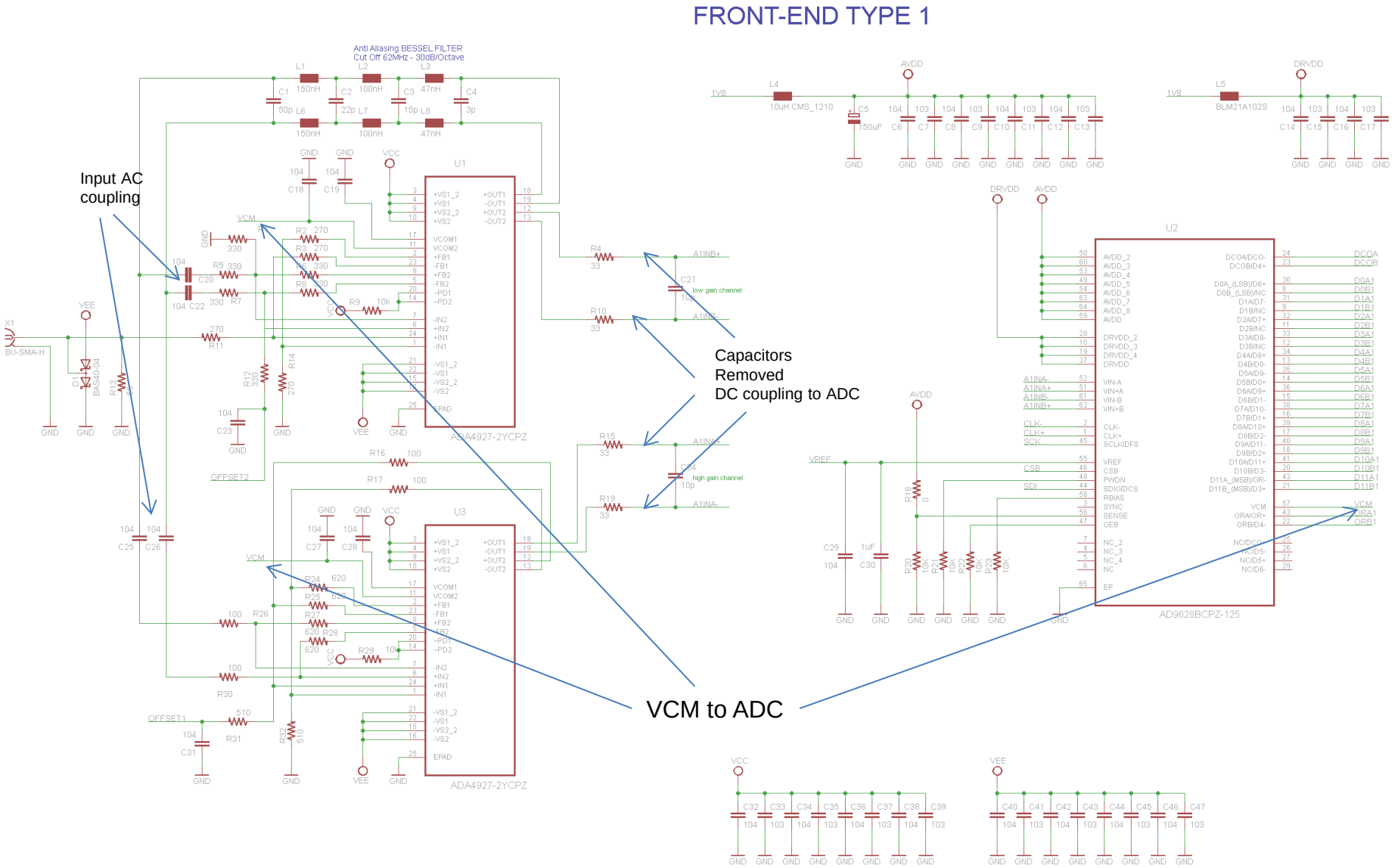
Input signal 1mVPP 1MHz
Range of signal with noise

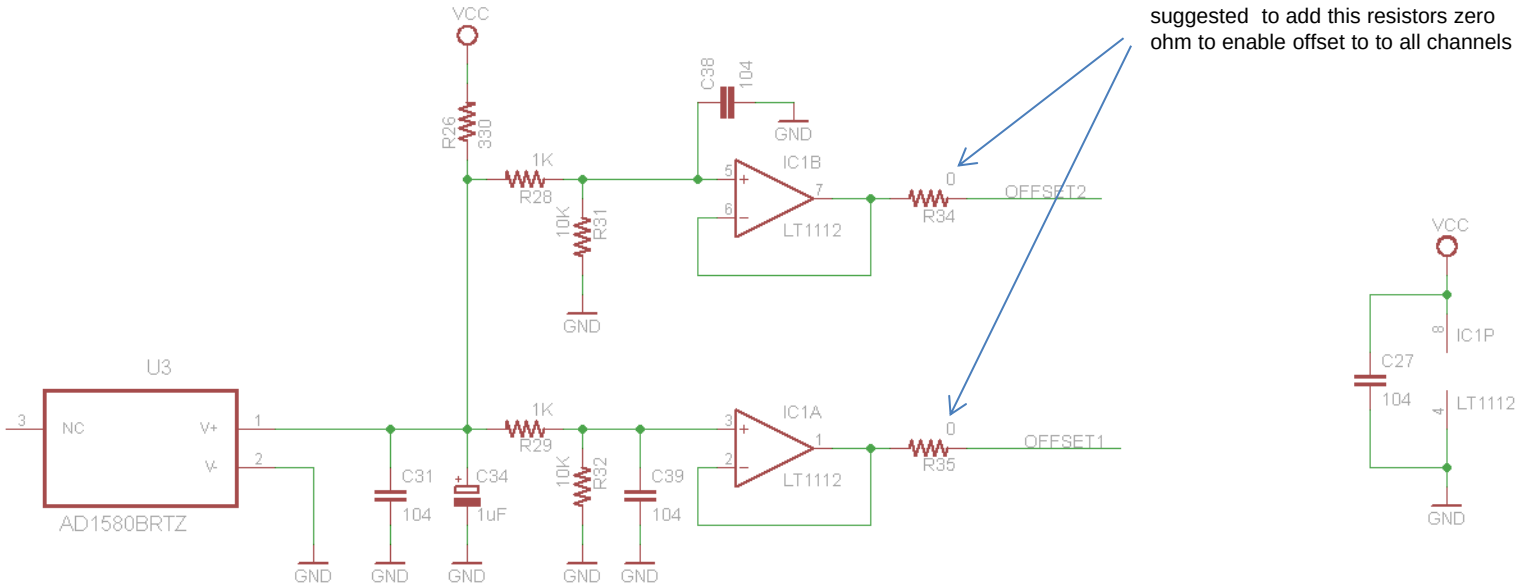


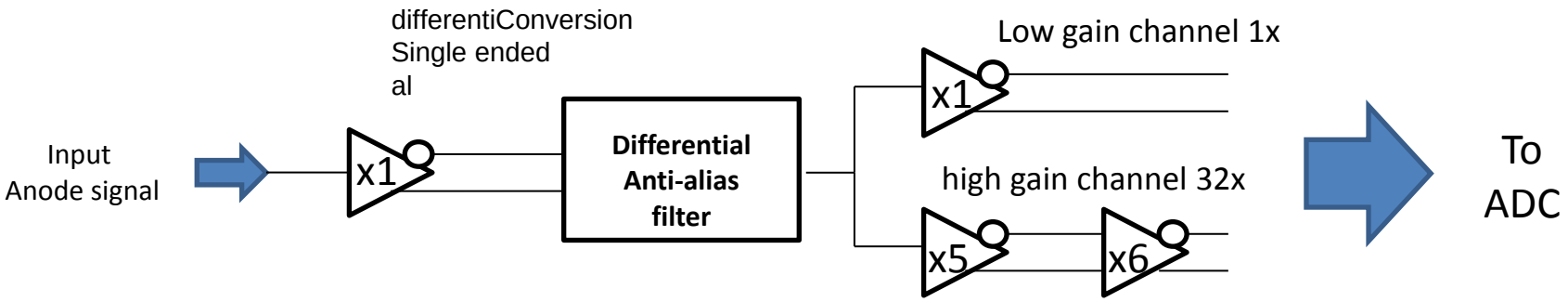
Range
without signal input
(close to ground)
Noise level about 8 mV

- **The solution with OPA847 as single amplifier stage doesn't give us a low noise on output than a double stage with ADA4927**

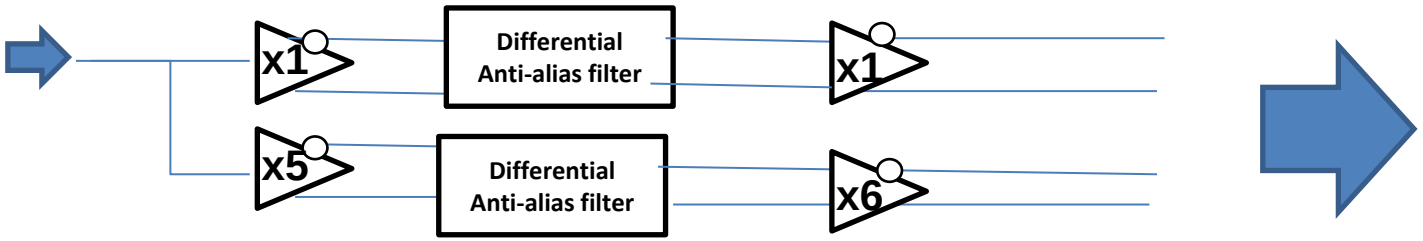
Modifications for the offset generation




suggested to add this resistors zero ohm to enable offset to to all channels
VCC
R26
330
1K
R28
10K
R31
GND
C38
104
GND
IC1B
LT1112
0
R34
OFFSET2
U3
NC
V+
V-
AD1580BRTZ
1K
R29
10K
R32
C31
104
C34
1uF
C39
104
IC1A
LT1112
0
R35
OFFSET1
VCC
C27
104
IC1P
LT1112
GND

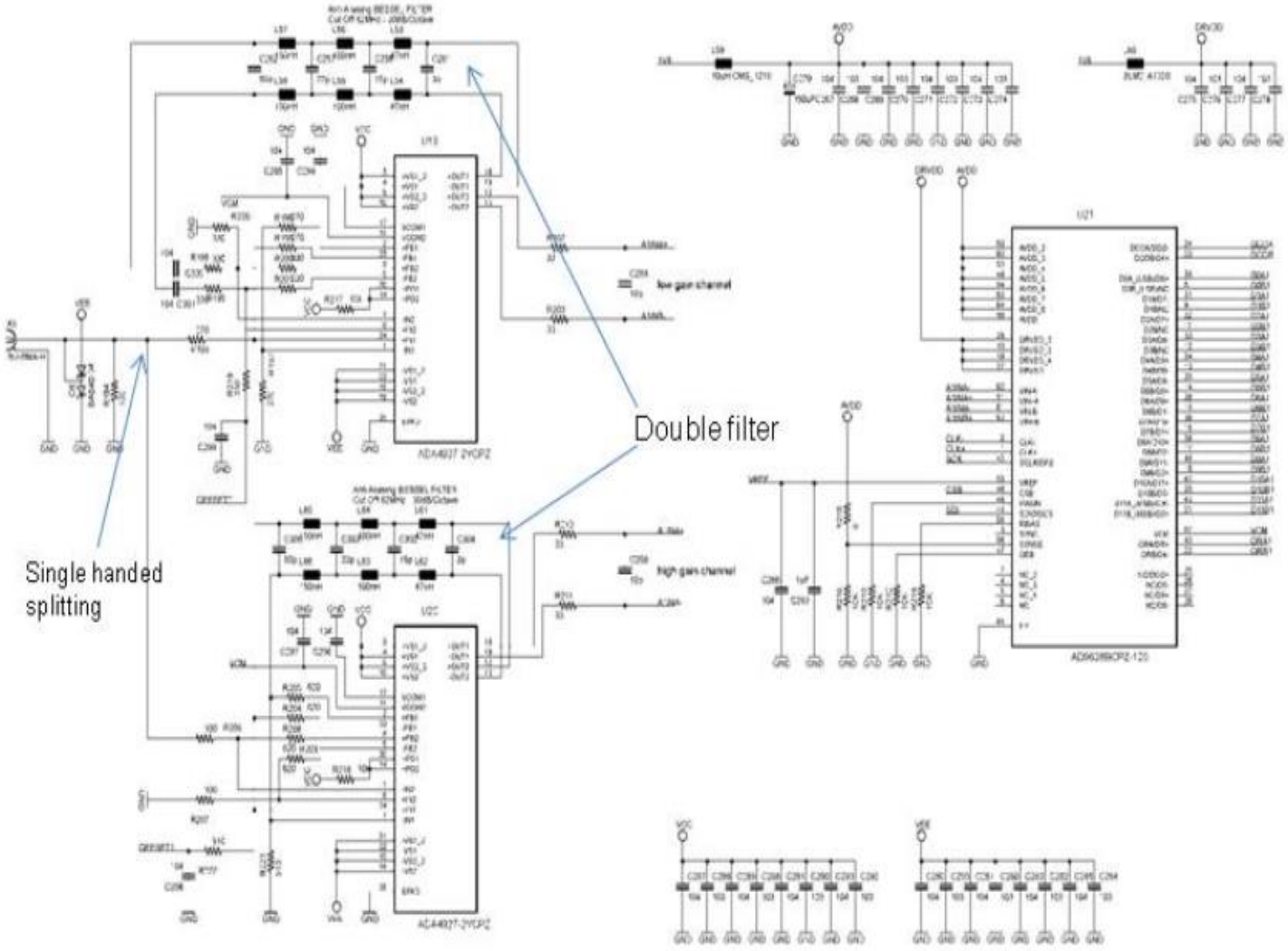


This is the old type 1 input, dedicated to the standard photonis PMT. This configuration is affected by a noise level of about 10 mV. In order to reduce the noise an alternative configuration has been presented, involving two separated filters. The space dedicated to each channel is enough, so we suggest to implement the following:



This configuration has been tested and the measured noise level was about a factor 2 lower

FRONT-END TYPE 1



Conclusions

Voltage reference is very important for the precision of analog conversion

Internal ADC generator for the common reference is a solution with very low thermal drift and the error for the load current (five ADC) is about 0.5 % (5mV on 1V)

The solution with external generator must have better features than internal generator and the circuit should be appropriate and stable.
The proposed external circuit solution requires an appropriate thermal exscursion test.
However, a solution with external generator could be provided and not mounted on the board.

The 2 filter configuration has a factor 2 less noise, so it is recommended.
Other options discussed in Grenoble have been tested, but the result are not satisfatory

We started working on the spi driver to be implemented in the zynq. We bought Zedboard with the zynq7000 evaluation board.