Pierre Auger Observatory

Surface Detector Electronics Upgrade
Critical Design Review
WP5 Design Report

Abstract:
This document describes the design report for the WP5 SDEU for the Critical Design Review, Orsay, 2015 February 4th.

Document written by: E Lagorio, J. Bouvier *Institute:* LPSC Grenoble		*Agreed by:*	P. Stassi
Date:	*15 January 2015*	*Date:*	*15 January 2015*
Local Reference:	*n/a*	*Project Reference:*	*WP05-LPSC-01C*

Table of Content

ACRONYMS

ADC	Analog to Digital Converter
ARM	Advanced RISC Machines
BGA	Ball Grid Array
CDR	Critical Design Review
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate
EEPROM	Electronically Erasable Programmable Read Only Memory
ER	Environmental Requirement
FPGA	Full Programmable Gate Array
FR	Functional Requirements
GPS	Global Positioning System
ICD	Interfaces Control Document
IR	Interface Requirements
LVDS	Low Voltage Differential Signaling
n/a	non applicable
OR	Operational Requirements
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PR	Physical Requirements
QR	Quality Requirements
RAM	Random Access Memory
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronic Upgrade
SOC	System On Chip
SR	Support Requirements
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UB	Unified Board
USB	Universal Serial Bus
USB OTG	USB On-The-Go
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VM	Verification Matrix
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
01	A	14/01/15		DRAFT for approbation
01	B	14/01/15	P. Stassi	First version
01	B	14/01/15	P. Stassi	Minor corrections

1. INTRODUCTION

This document describes the design report for the WP5 SDEU for the Critical Design Review, Orsay, 2015 February 4th

1.1 Reference documents

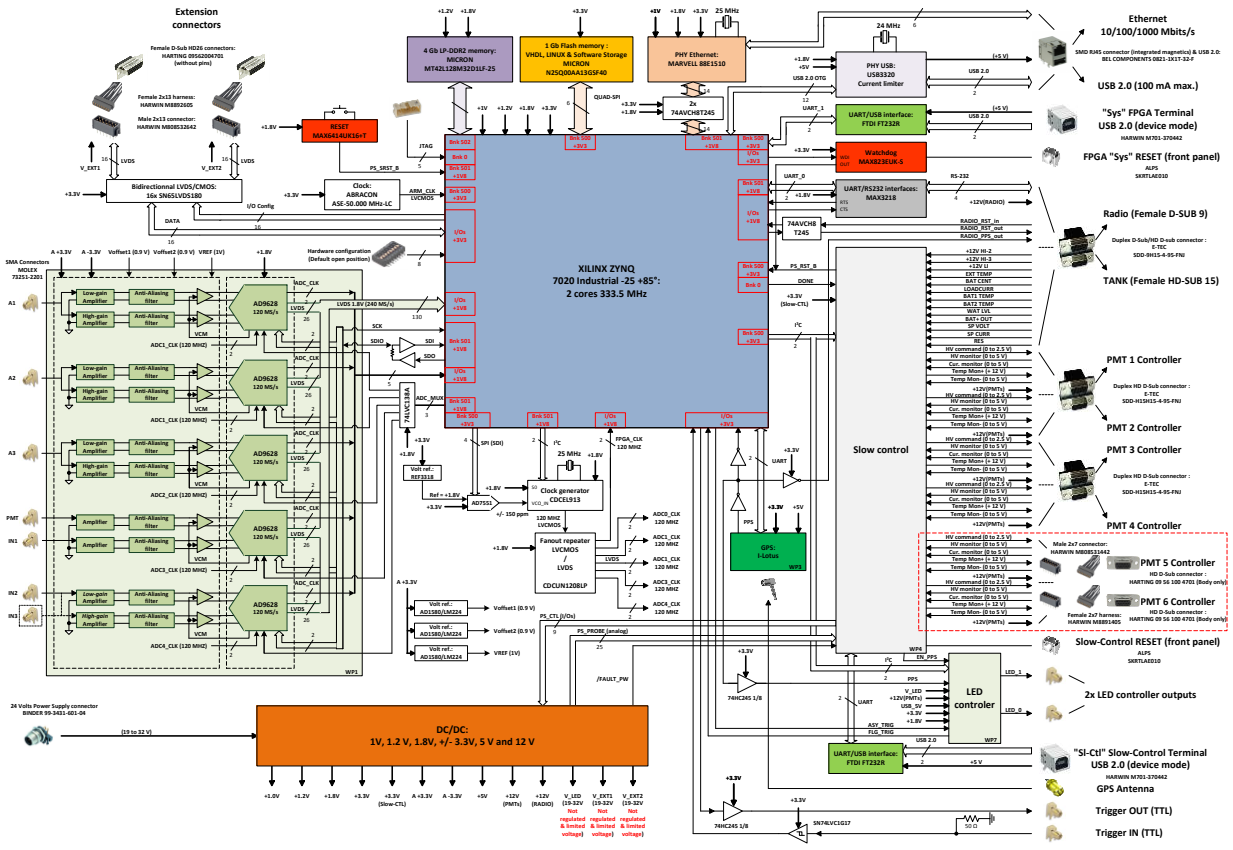
RD1 SDEU Critical Design Plan - *WP10LPSC14C_CDR_Plan*
RD2 SDEU technical specification document - *WP10LPSC03_SDEU_Specification.*

2 DESIGN CONCEPT AND SOLUTION SELECTED

The Work Package 5 is in charge of the hardware and firmware SDE electronic board architecture and other WP functions integration.

2.1 SDE architecture

The SDE update is based on a "System On Chip" (SOC) component Xilinx Zynq 7020. This one is built around two ARM Cortex A9 processor cores completed by programmable logic cells.
This electronic will integrate an operating system: Linux stored in EEPROM.
Following the SDE electronic architecture with the others Work Packages:



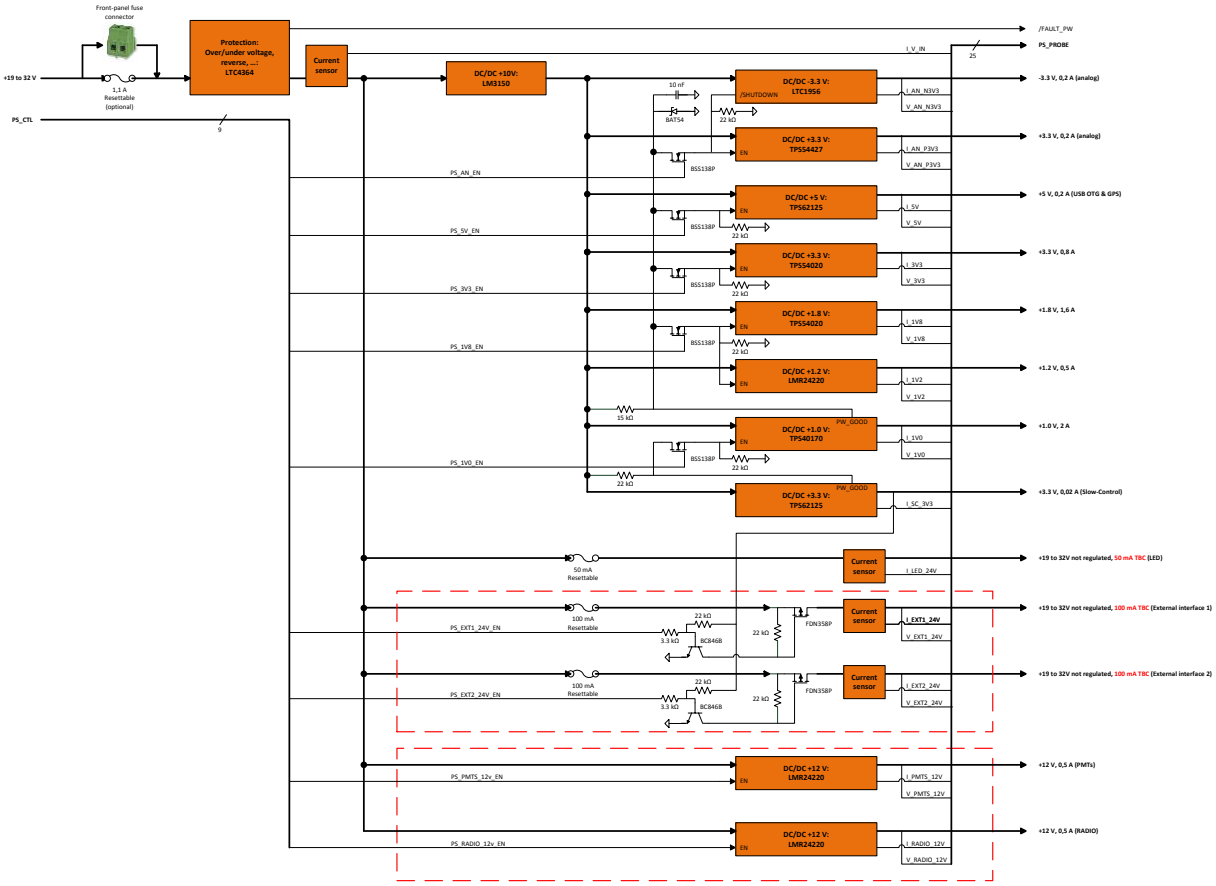
The main characteristics are:

- 10x ADCs 12 bits 120 MS/s

- Dual µ-processor ARM core Cortex A9 333 Mhz for the operating system and the local software applications.
- Gbits LP-DDR2 memory (Low Power DDR2)
- 1 Gbits Flash memory (storage memory)
- i-LOTUS GPS for the time tagging function.
- LINUX
- Online firmware & software updatable
- 10/100/1000 Mbits/s Ethernet and a master USB 2.0 interfaces link with external electronic.
- Slow-control system.
- Operating system console.

2.2 Power supplies

Power supplies are provided by several high efficiency DC/DC converters.



The SDE electronic board input power is electronically protected in current limitation and reverse voltage protection and also by fuse located on the front panel.
Each power supply can be enabled or disabled, monitored in voltage and current by the Slow-Control system (WP4).
The Slow-Control system manages a specific electronic startup sequence.
Three power outputs are protected and limited by specific fuses.

2.3 Ram LP-DDR2

The operating system needs to have ram component for running.
The DDR memory controller of the ZYNQ chip cannot handle more than one die of memory and the LPDDR2 memory chip than include one memory die has a maximum size of 4Gb (128M x 32 bit).
LP-DDR2 technology was chosen to meet the low power requirements.

2.4 Storage memory

The firmware, the operating system and applicative software are stored in an EEPROM. To meet the needs update remotely secured mode, it is necessary that the memory capacity in at least twice the size of the entire firmware, OS and applicative.
The memory will contain two sets, the first containing a non-editable version, factory defined. The second contains a version that can be updated during operation.
Moreover EEPROM may contain parameters defined by the applicative software.
In the current state of design, SDE's memory capacity has been maximized but may nevertheless be decreased without changing the PCB.

2.5 Ethernet

10/100/1000 Mb Ethernet interface is implemented for communication with external electronics.

2.6 USB 2.0

USB 2.0 interface is implemented for communication with external electronics.

2.7 Operating system consoles

A console output has been implemented for diagnostic purposes and debugging of the OS or the applicative software.

2.8 « Radio » serial interface

The Radio serial connection allows connecting to the radio network of Auger. Through this interface it is possible to remotely SDE, to update and retrieve stored data.

2.9 Extension connectors

SDE has two proprietary connections (protocols not specified for the moment) 8-bit LVDS each. They are designed for future usage.

2.10 Reset

There are 2 kind of RESET. The first one is hardware RESET, causing the complete re-initialization of FPGA firmware, OS and applicative software. The second one causes only a reboot of the OS and the applicative software.
The two types of reset are commanded by a push button, the first one on the front panel and the second one can be accessed on the board.
Note that the hardware RESET can also be activated by two other actions:

- A time overtakes of the Hardware Watchdog.
- An action by the Slow-control system.

2.11 Clocks generator

Due to the operation at 120 MHz, a clock generator and a distributor has been implemented. The necessity to have a stable clock requires controlling the generator by an analog signal generated by a DAC.
To ease the data acquisition of ADCs, all outgoing distributor lines clocks have the same length on the circuit board, and the outgoing data of ADCs will be in phase (excepted for the internal phase jitter).

2.12 GPS

For purposes of the internal function of Time Tagging, a GPS receiver is located on the board. It communicates with the FPGA through an RS-232 serial connection and generates a PPS synchronization signal.

2.13 ADCs interface.

The digitizing part is composed of 5 Dual ADCs. ADC management is done using SPI control signals. Data reading is done using 14 LVDS differential pairs per ADC.

2.14 Slow-Control and LED controller.

These systems communicate with the FPGA through a common I²C serial interface, the FPGA is the master and the Slow-Control and LED controller are at two slave addresses.

3 PRE-PROTOTYPE TEST BOARD DESIGN

For test and validation requirements, a pre-prototype board has been developed, including power supplies, the SOC, memories (LP-DDR2 and EEPROM), a dual ADC, clock generator and distributor, and a Slow-Control function emulation using a microcontroller PIC 18F4550.

4 TEST REPORT AND RESULTS ON PRE-PROTOTYPE.

All the features mentioned above sub sets were tested and validated. This board has also been used to develop in firmware an initialization algorithm of ADCs for the time synchronization of the data.

5 DESIGN STATUS OF THE PROTOTYPES

The prototype design is almost completed. It will be ready and be validated by other WPs mid-February. From that date will begin the realization by making 5 boards. Estimated time: 3 weeks.
The cabling will then be performed at KIT in Germany.
The part procurement is now realized at more than 95%.