Technical Design Document

Wp1: Analog PMTs signal processing

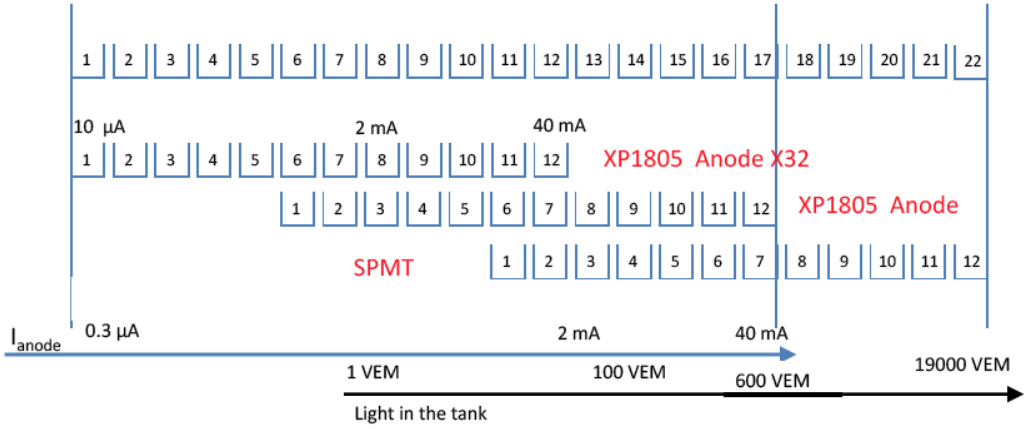
Ref: WP1INFNLE_SDEU_CDR_WP1_19Jan15

Specific requirements

The wp1 is in charge to design the analog PMTs processing signal. The new specific requirements are:

1) 5x2 differential channels, low noise (1/2 LSB < 25 0 μV), 12 bit, and 120 MHz ADC converter
2) Power < 0.5 Watt/channel
3) 10 Low pass Filter (Bandwidth < 60 MHz)
4) 3x2 channels to read the PMT anode signal and splitted in high (32 dB) and low (0 dB) gain + 4 single channels with possible different gain (1 Small PMT, 3 ASCII)
5) Analog signal dynamic range: from 100 mV to -1900 mV (5% of dynamic reserved for the undershoot)
6) 1 ms recovering time

In the following sheme, the dynamic range of the new electronic is shown:



The dynamic range scheme will allow moving the trigger threshold two bits higher and increasing the current dynamic range by a factor of 32.

The gain of the PMTs will be kept the same as before, 3 10^5. The muon peak will be in channel 200. An additional small PMT (SPMT) will be used to extend the dynamic range.

Design concept and solution selected

To obtain the requested performances various possibilities have been investigated. The idea is to split the PMTs anode signal in two channels: a 0 dB and a 32 dB channels. Filters for each channel will be implemented instead of a single filter for each anode to avoid to amplify the noise produced by the filters. The final adopted solution is the following:

a) Type 1 Input: The signal from the anode of the PMTs are splitted and amplified, by 0dB the low-gain channel and by 5dB the high-gain channel and made differential. This has been done using dual channel ADA4927 Operational Amplifier (OA). Then a 5 pole passive Low-band pass filter is

implemented using inductances and capacitors. Finally the last amplification stage is implemented using the same ADA4927 OA obtaining a 0 dB and a 6 dB gain on low-gain and high-gain channel respectively. At that stage are also implemented the V_{CM}, the common mode voltage reference, and the offset generator to make the ADC working in the correct dynamic range (form 100 mV to -1900mV)

b) Type 2 Input: The same solutions are adopted with the last 4 channels but with the possibility to split a single input on two channels or using two separated channels with the amplification tunable by the choice of the feedback resistors in both solutions. One of this will be used for the "Small PMT" and the other 3 for ASCII.

Design implementation, schematics

In Figure1 the implemented block diagram is shown where the detail of the passive filter is shown. The offset to the ADC differential input is implemented at the last amplification stage at the input of the OA. In Figure 2 the detailed design of type 1 input is shown.

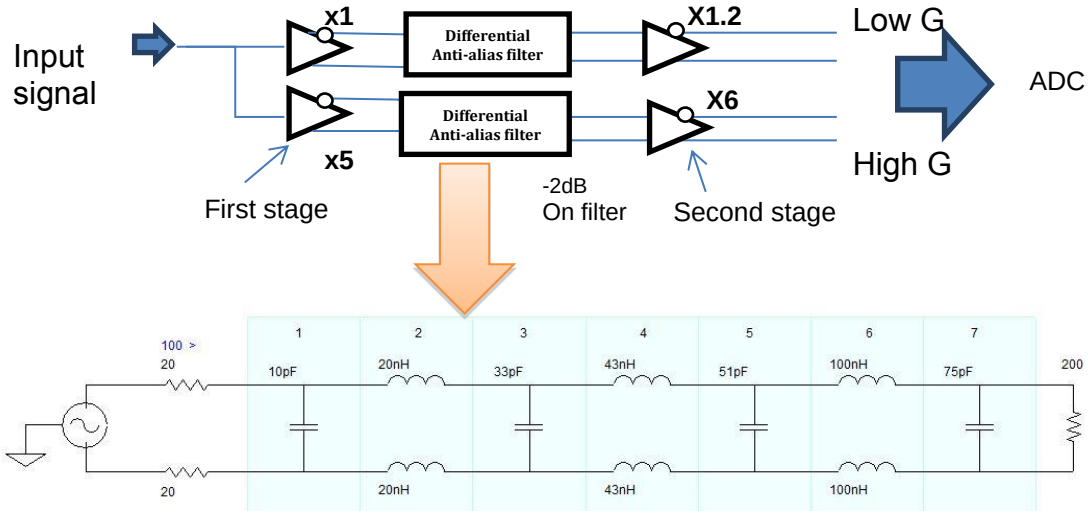


Figure 1: Type 1 input channel with the 2 gains. The anti-aliasing passive filter design is shown.

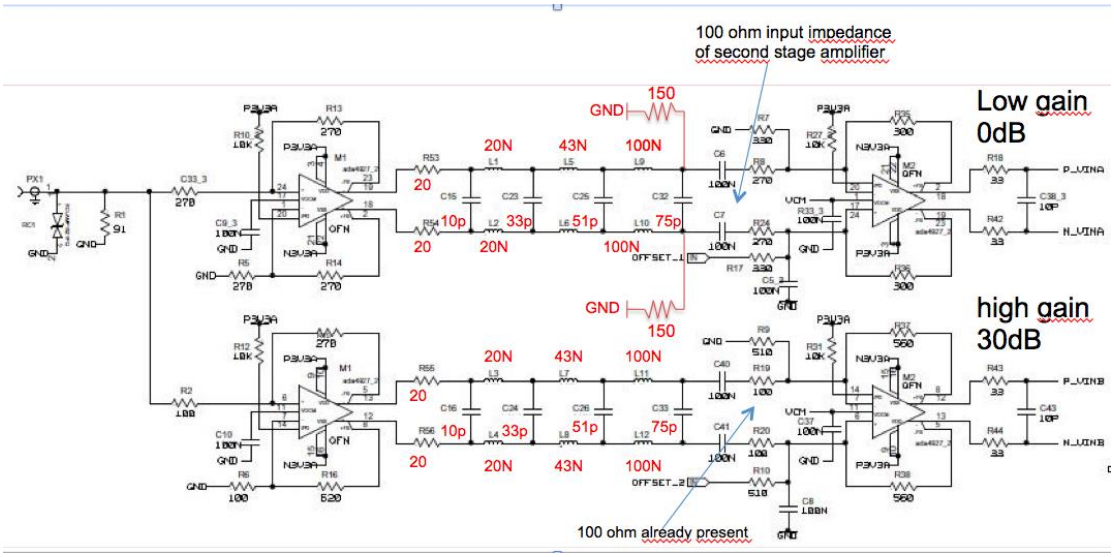
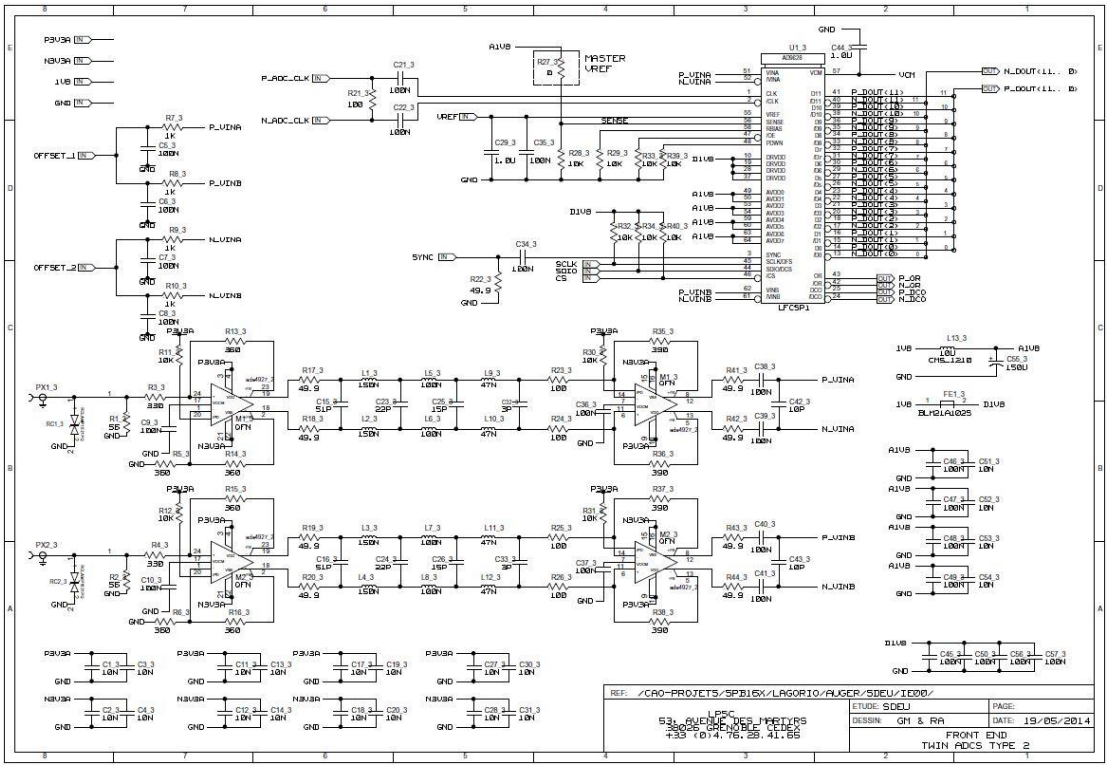


Figure 2: Detailed design of Type 1 input channel with the offset and V_{CM} solutions.



The offset can be supplied by a single generator and distributed on a common line to each ADC channel input. Due to the importance of the stability of those values, the possibility of activating dedicated offset generators for each channel has been implemented by mean of Zero resistors. In Figure 3 the offset generator details are shown.

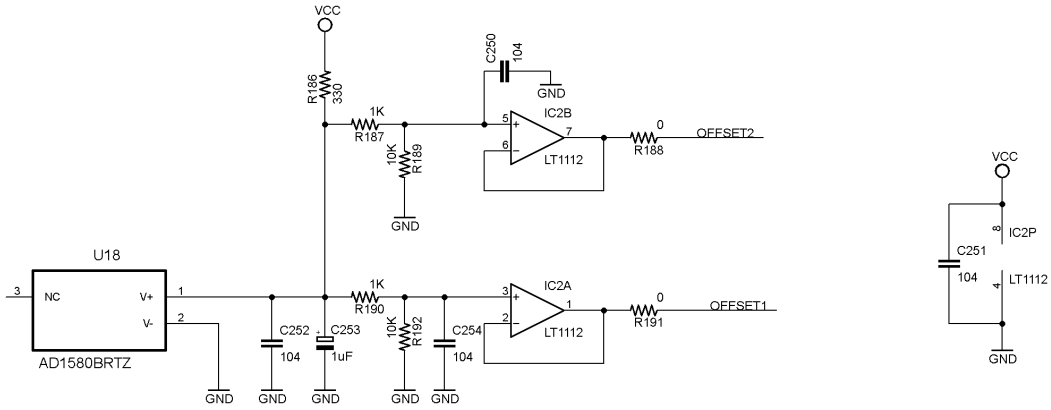


Figure 3: The offset generator design

The relative Schematics are the following:

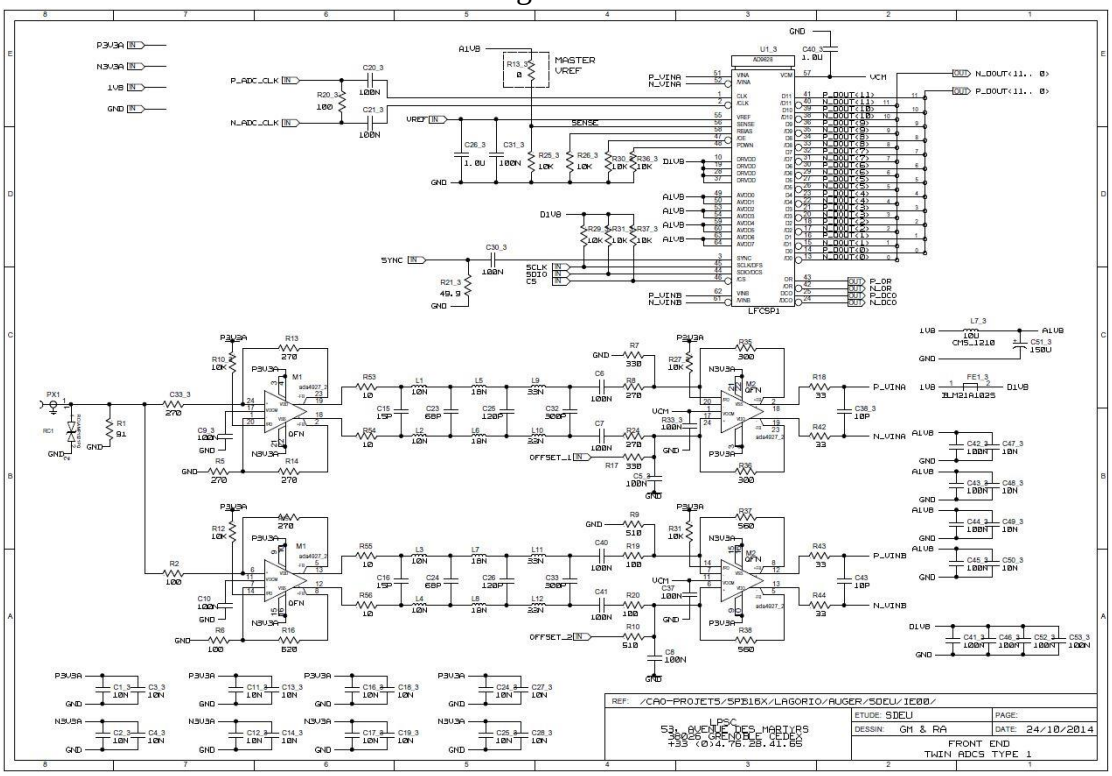
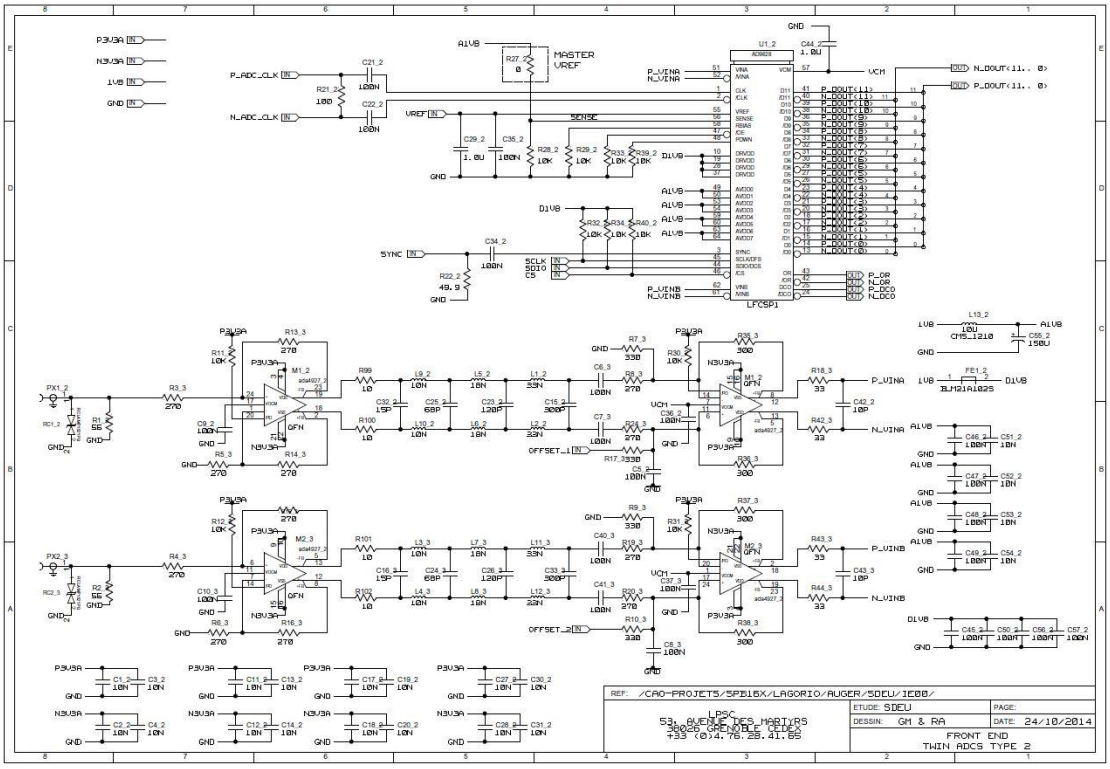


Figure 4: Front-end Type 1 with the two filters solution



Prototype test board design

Various prototype test boards have been designed in order to test the proposed solution. The last version proposed is a front-end board that can be inserted on the Analog Device test board in order to use the Analog Device tools to read the ADC.

Figure 5.: Front-end prototype test board

In Figure 6 a picture of the implemented prototype and in Figure 7 the relative schematics are shown.

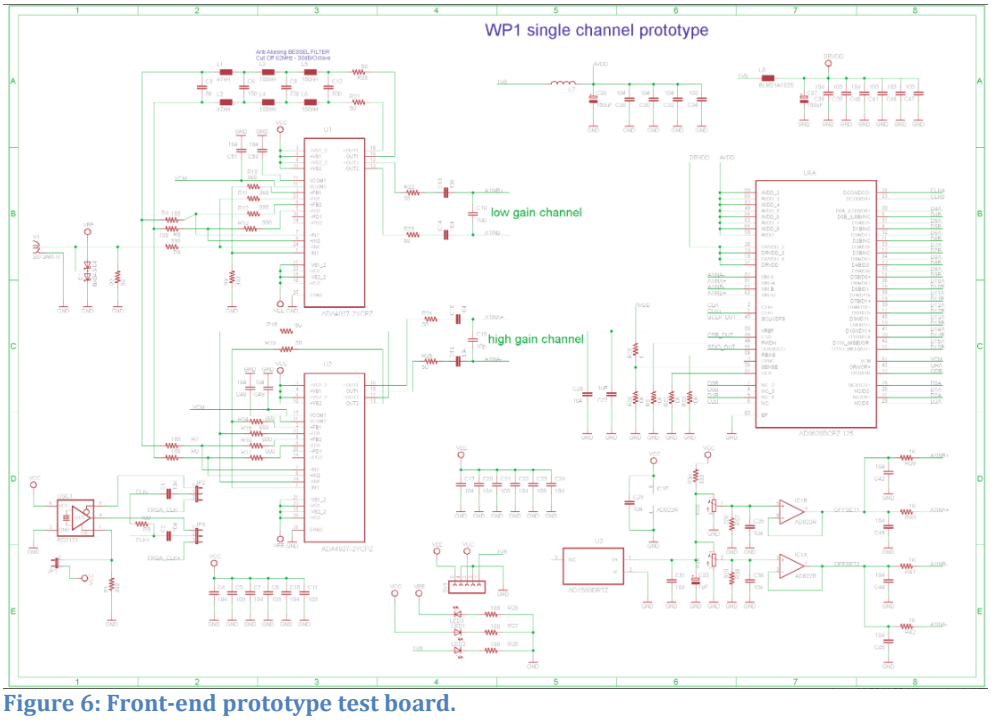


Figure 6: Front-end prototype test board.

A new prototype board has been designed to be tested on a Zedboard on which we are installing Petalinux in order to test the entire chain of initialization and acquisition of the ADC. The board will contain two ADCs with the possibility to test different input type and filter solutions.

Test report and results on prototype

Many test have been done. Here we report a synthesis.

Power consumption:

Work Package	Functions	Devices	Maximum current (mA) / power supply (V) / Devices											Max Power / Devices (mW)	Nb.	Powers	Powers / WP
			FPGA				Slow C	Analog		GPS	USB	Radio	PMT				
			1	1,2	1,8	3,3	3,3	3,3	-3,3	5	5	12	12				
WP1	Front-End	Anti aliasing filter (TBD)						0	0					0	3	0,00	
		Low-gain path filter proposal						2,8	2,8					18,48	3	55,44	
		High-gain path filter proposal						2,8	2,8					18,48	3	55,44	4216,38
		Differential amplifier (2xADA4927-2)						82	82					541,2	5	2706,00	
		12 bits ADC 120MS/s (Twin AD9628) proposal			155,5									279,9	5	1399,50	

The response of the filter is shown in Figure 8 the simulated filter is shown.

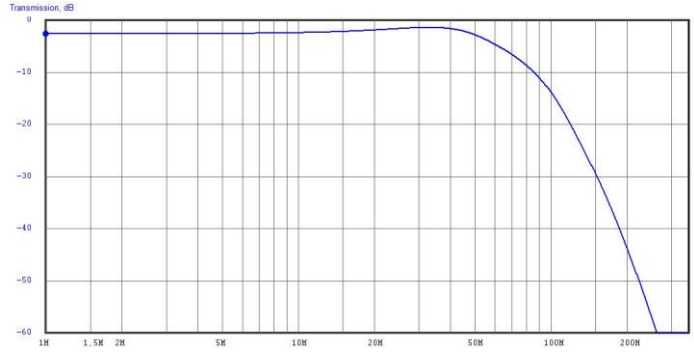


Figure 7: Simulated Filter

In Figure 9 the implemented filter response si shown for both the High Gain and Low Gain channels. The Cut-off frequency is 60 MHz and the High Gain is 30 dB.

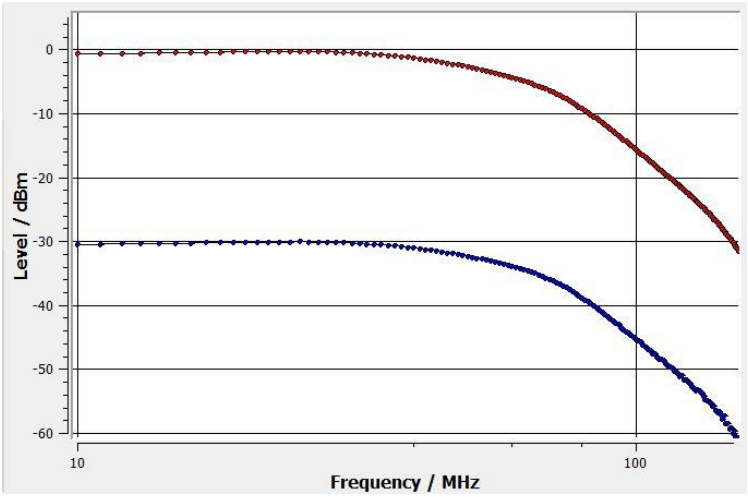
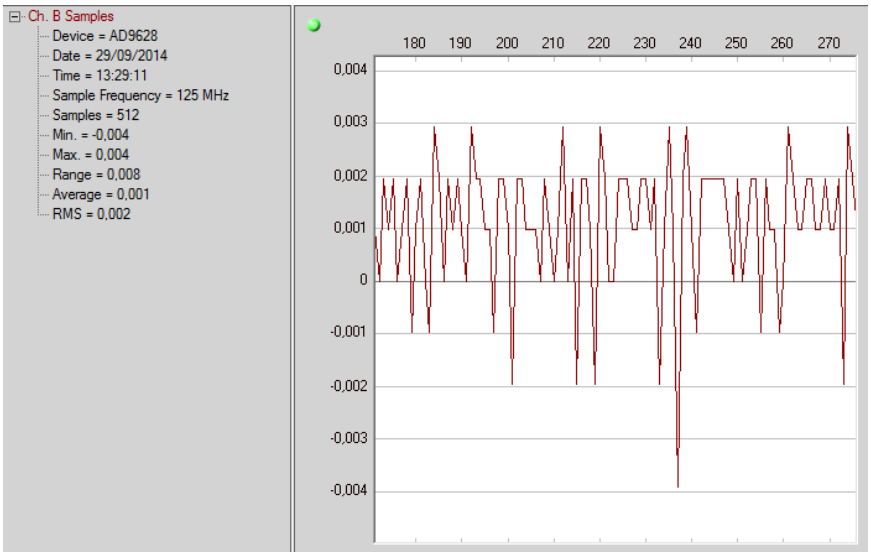


Figure 8: Implemented Filter Test. High Gain (Red Line) - Low Gain (Blue Line). The cutoff is 60 MHz.

The noise Level of the Low-Gain Channel is less than 500 µV (around 200 µV rms). The High-Gain Channel is at Level of 2 mV rms. Test on the final prototype board must be repeated.



Design Status

The Design for the first prototype boards is ready and already submitted to Grenoble working group. These are the actual designs:
(see WP5 report)