Pierre Auger Observatory

Surface Detector Electronics Upgrade Critical Design Review Plan

Abstract:
This document gives the organization of the Critical Design Review for the H/W design of the SDEU, held the 4th of February 2015.

Document written by:	P. Stassi Project System engineer	*Agreed by:*	T. Suomijärvi Task leader
Date:	*January 07, 2014*	*Date:*	*January 07, 2014*
Local Reference:	ATRIUM-xxxx	*Project Reference:*	*WP10LPSC14C*

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ACRONYMS

AD	Applicable Document
ADC	Analog to Digital Converter
AIT	Assembly, Integration and Tests
AIV	Assembly, Integration and Verification
BGA	Ball Grid Array
CAD	Computer Aided Design
CDR	Critical Design Review
CPU	Central Processing Unit
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
DRC	Design Review Checklist
ER	Environmental Requirement
FDIR	Failure Detection Isolation and Recovery
FMECA	Failure Mode Effect and Critical Analysis
FPGA	Full Programmable Gate Array
FR	Functional Requirements
Fs	Full scale
FTE	Full Time Equivalent
GPS	Global Positioning System
H/W	HardWare
ICD	Interfaces Control Document
IR	Interface Requirements
LED	light-emitting diode
Msp/s	Mega samples per second
n/a	non applicable
OR	Operational Requirements
OS	Operating System
PAO	Pierre Auger Observatory
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PMT	PhotoMultiplier Tube
PR	Physical Requirements
QMP	Quality Management Plan
QR	Quality Requirements
RD	Reference Document
RDA	Research and Development Array (Auger North)
RF	Radio Frequency
RID	Review Item Discrepancy
SD	Surface Detector
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronics Upgrade
SPMT	Small PMT
SR	Support Requirements
S/W	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UB	Unified Board
UC	Upgrade Committee
USB	Universal Serial Bus
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VM	Verification Matrix
WBS	Work Breakdown Structure
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
14	A	17/12/14	P. Stassi	First Issue
14	B	18/12/14	P. Stassi	Minor corrections
14	C	07/01/15	P. Stassi	Completion

1. INTRODUCTION AND REVIEW OBJECTIVES

This Critical Design Review (CDR) is a technical review on the SDEU hardware prototype design that aims to:

- Determine if the H/W design of the SDEU prototype has been done following the Development plan (RD1)
- Determine that the detailed H/W design satisfies the performance and engineering requirements of the development specification (RD2)
- Establish the detailed design compatibility with the existing Surface Detector system items of equipment.
- Insure that all risks or uncertainties have been identified and will be managed

This CDR ensures that the program can proceed with the construction of the SDEU Prototype and meet the performance requirements within cost, schedule and other system constraints.

This CDR involves a review of design documentation to ensure the design documents are consistent.

1.1 Applicable Documents

AD1 Pierre Auger Observatory Quality Assurance Plan, October 2000, V1
AD2 PAO SDE Quality Management Plan, SDE_QMP Rev 2002-04

1.2 Reference Documents

RD1 SDEU Development Plan, *WP10LPSC02_SDEU_Dev_Plan*.
RD2 SDEU technical specification document, *WP10LPSC03_SDEU_Specification.*

2. REVIEW DOCUMENTATION

The following table indicates the general data package provided to the CDR review board:

Designation	Reference	Revision
Section 01: Development Plan		
SDEU Development Plan	WP10LPSC02	I
Section 02: H/W Specifications		
SDEU Specifications	WP10LPSC03	G
Section 03: S/W Specifications		
SDEU OBSW Specification	WP6LPSC13	A
Section 04: Project Risks Analysis		
SDEU project Risks Analysis	WP10LPSC06	B
Section 05: FMECA - FDIR		
SDEU FMECA-FDIR	WP10LPSC10	B
Section 06: Tests Plan		
SDEU AIT-AIV Plan	WP10LPSC11	C
Section 07: ICD		
SDEU Electrical Interfaces Control Document	WP10LPSC05	D
SDEU Detectors Interfaces Control Document	WP10LPSC07	F
Section 08: WBS Cost estimate		
SDEU WBS	WP10LPSC08	J
Section 09: Schedule		
SDEU Project General Schedule	WP10LPSC04	J

Table 2a – Review data package for the CDR

Furthermore, each **WP** team involved in the H/W design (RD1 or see below) provides a technical design document containing:

- Specific requirements (if any)
- Design concept and solution selected
- Design implementation, schematics
- Prototype test board design
- Test report and results on prototype
- Design Status
- Presentation viewgraphs

#	*Names*
WP1	Analog PMTs signal processing
WP3	Time Tagging development
WP4	Slow Control development
WP5	UUB H/W Design & Integration
WP7	Calibration & Control tools development

Table 2b – WP involved in the H/W design

3. REVIEW ORGANIZATION

3.1 Events Schedule:

The review milestones are:

1. Sending the documents to the Review Board Members:
   January 19th 2015
2. Preparation of the meeting (teleconf): TBD
3. Sending to the project management the presentation package (viewgraphs, etc.):
   26th January 2015
4. Recommendations of the Review Board to the project management:
   February 20th 2015.

3.2 Review Agenda:

Wednesday 4 February 2015

9:30 – 16:00 SDEU CDR

- 9:30-10:00 Development plan – Project organization
- 10:00-10:30 Design Specifications

10:30-11:00 coffee break

- 11:00-13:00 Design Implementation
  - 11:00-11:30 WP5 Unified Board
  - 11:30-12:00 WP1 Analog PMT signal processing
  - 12:00 12:20 :WP3 Time Tagging
  - 12:20-12:40 WP4 Slow Control
  - 12:40-13:00 WP7 Calibration tools

13:00-14:00 Lunch

- 14:00-14:20 Interfaces
- 14:20 14:40 Technical risks, FMECA-FDIR
- 14:40-15:00 AIT-AIV Plan
- 15:00-15:30 Small PMT Design
- 15:30-16:00 Cost and Schedule

16:00-16:30 coffee break

Location: The CDR will be held at the IPNO, Orsay, France.

4 ATTENDEES FOR THE CDR

4.1 Review board:

Name / Affiliation	
Stéphane COLONGES / APC Paris	Chairman
Dominique BRETON / LAL Orsay	Electronic
Alexander MENSHIKOV / KIT Karlsruhe	Electronic

4.2 SDEU representatives:

Name / Affiliation	
Tiina SUOMIJARVI / IPNO	Project leader (WP10)
Patrick STASSI / LPSC	System engineer (WP10)
Giovanni MARSELLA / INFN Lecce	WP1 representative
Corbin COVAULT / CWU	WP3 representative
Karl-Heinz BECKER / WPU	WP4 representative
Eric LAGORIO / LPSC	WP5 representative
Luca LATRONICO / INFN Torino	WP7 representative

4.3 PAO representative:

Name / Affiliation	
Jonny KLEINFELLER / KIT Karlsruhe (TBC)	
TBD	

5 ANNEX

5.1 Review Item Discrepancy (RID):

See at the following page the Review Item Discrepancy template which can be used by the panel board during the review.

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**		**SDEU CDR**
ORIGINATOR name.	Date	RID Nº: RID-
RID TITLE:		
AREA :		
Document title / Nº-Ref / chapter / page:		
DISCREPANCY:		
INITIATOR RECOMMENDED SOLUTION:		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	

5.2 Design Review Checklist (DRC):

See at the following pages the Design Review Checklist template which can be used to help the panel board during the review.

Design Review Checklist

Checklist Description: This checklist captures common elements that should be present in any design. It is presented during the Design Review process to stimulate thought, guide brainstorming, and to ensure the design being outlined contains all proper design considerations. As the project architecture, system, and application design is being reviewed, assess the design considerations that apply to your subject matter expertise and business/technical needs.

Project Name:	**Review Date:**
Assessment and Recommendations: ☐ Approved without revision ☐ Approved with revisions (see Notes) ☐ Not approved	**Notes:**
Reviewer:	**Signature:**
Artifacts Reviewed: ☐ Technical Design Specification ☐ Implementation Plan	☐ Conceptual Architecture Review Checklist ☐ Requirements Traceability Matrix ☐ Other**:**

	General Design	Comments
☐	Does the design support both product and project goals?	
☐	Is the design feasible from a technology, cost, and schedule standpoint?	
☐	Have known design risks been identified, analyzed, and planned for or mitigated?	
☐	Are the methodologies, notations, etc. used to create and capture the design appropriate?	
☐	If possible, were proven past designs reused?	
☐	Does the design support proceeding to the next development step?	

	Design Considerations	Comments
☐	Does the design have conceptual integrity (i.e., does the whole design tie together)?	
☐	Can the design be implemented within technology and environmental constraints?	
☐	Does the design use standard techniques and avoid exotic, hard-to-understand elements?	
☐	Is the design unjustifiably complex?	
☐	Is the design lean (i.e., are all of its parts strictly necessary)?	
☐	Does the design create reusable components if appropriate?	
☐	Does the design allow for scalability?	
☐	Are all time-critical functions identified, and timing criteria specified for them?	
☐	Are the hardware environment completely defined, including engineering change levels and constraints?	
☐	Are the pre-requisite and co-requisite software and firmware clearly identified, including release levels and constraints?	

Requirements Traceability		Comments
☐	Does the design address all issues from the requirements?	
☐	Does the design add features or functionality, which was not specified by the requirements (i.e., are all parts of the design traceable back to requirements)?	
☐	If appropriate, has requirements coverage been documented with a completed requirements traceability matrix?	
☐	Are all of the assumptions, constraints, design decisions, and dependencies documented?	
☐	Have all reasonable alternative designs been considered, including not automating some processes in software?	
☐	Have all goals, tradeoffs, and decisions been described?	
☐	Have all interfacing systems been identified?	
☐	Are the error recovery and backup requirements completely defined?	
☐	Have the infrastructure e.g. backup, recovery, checkpoints been addressed?	
Consistency		**Comments**
☐	Does the design adequately address issues that were identified and deferred at previous upstream levels?	
☐	Is the design consistent with related artifacts (i.e., other modules, designs, etc.)?	
☐	Is the design consistent with the development and operating environments?	
Performance Reliability		**Comments**
☐	Are all performance attributes, assumptions, and constraints clearly defined?	
☐	If appropriate, are there justifications for design performance (i.e., prototyping critical areas or reusing an existing design proven in the same context)?	
Capacity Planning		**Comments**
☐	Does the design improve productivity?	
☐	Is scalability development into the plan and is maintainable?	
☐	Is Total Cost of Ownership (TCO) controlled or reduced?	
Maintainability		**Comments**
☐	Does the design allow for ease of maintenance?	
☐	If reusable parts of other designs are being used, has their effect on design and integration been stated?	
Compliance		**Comments**
☐	Does the design follow all standards necessary for the system? (i.e., date standards)	
☐	Have legal/regulatory requirements been assessed and accounted for?	