Pierre Auger Observatory

Surface Detector Electronics Upgrade Critical Design Review Panel Report

Abstract:
This document is the review board recommendation next to the Critical Design Review for the H/W design of the SDEU, held the 4th of February 2015.

Document written by: S.Colonges (APC – Paris) - Review Board chairman	*Agreed by:* Alexander MENSHIKOV / KIT Karlsruhe and Dominique BRETON / LAL Orsay – Review board members
Date: *February 04, 2015*	*Date:* *February 04, 2015*
Local Reference: ATRIUM-4387	*Project Reference:* *WP10APC01E*

Table of Content

ACRONYMS

AD	Applicable Document
ADC	Analog to Digital Converter
AIT	Assembly, Integration and Tests
AIV	Assembly, Integration and Verification
BGA	Ball Grid Array
CAD	Computer Aided Design
CDR	Critical Design Review
CPU	Central Processing Unit
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
DRC	Design Review Checklist
ER	Environmental Requirement
FDIR	Failure Detection Isolation and Recovery
FIDES	not an acronym, Latin word for “Trust”
FMECA	Failure Mode Effect and Critical Analysis
FPGA	Full Programmable Gate Array
FR	Functional Requirements
Fs	Full scale
FTE	Full Time Equivalent
F/W	FirmWare
GPS	Global Positioning System
H/W	HardWare
ICD	Interfaces Control Document
IR	Interface Requirements
LED	light-emitting diode
Msp/s	Mega samples per second
n/a	non applicable
OR	Operational Requirements
OS	Operating System
PAO	Pierre Auger Observatory
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PMT	PhotoMultiplier Tube
PR	Physical Requirements
QMP	Quality Management Plan
QR	Quality Requirements
RD	Reference Document
RDA	Research and Development Array (Auger North)
RF	Radio Frequency
RID	Review Item Discrepancy
SD	Surface Detector
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronics Upgrade
SPMT	Small PMT
SR	Support Requirements
S/W	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UB	Unified Board
UC	Upgrade Committee
USB	Universal Serial Bus
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VM	Verification Matrix
WBS	Work Breakdown Structure
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
01	A	4/02/15	S.Colonges	First Issue
01	B	13/02/15	A.Menshikov	
01	C	17/02/2015	D.Breton	
01	D	24/02/2015	S.Colonges	
01	E	24/02/2015	P. Stassi	Minors form corrections

1. ACKNOWLEDGEMENTS

The review board members congratulate the SDE Upgrade team for the work accomplished in preparation of this CDR. All the documents have been sent before the review according to the planning, allowing time for the panel to read them. It was a real pleasure to analyze all this information.

Special thanks to Patrick STASSI for his really huge work to prepare the data-package documents.

Many thanks to Tiina SÜOMIJARVI and Jim BEATTY, for the management of the SDEU electronic tasks.

The committee agreed to say, exhaustive specifications have been written. All work packages are almost complete.

2. PANEL EVALUATION

Specifications:

- The requirements have been exhaustively listed.
- Auger South and North experience (REX) is taken into account. Design team has audited Malargue Local Staff in order to identify all the failure causes occurred in the field.
-Work Packages have been correctly defined.
-Risks have been correctly identified.

Design:

-The FMECA and the reliability analysis have been initiated. Most critical functions and items are identified.
-All the work packages are on a good way to be completed.
-The most crucial work package is related to the Front End Electronics, due to the high level of the requirements. Multiple tradeoffs have been identified. Simulations have been performed. Test on prototypes boards should be completed. Conformity to requirements should be checked.

3. PANEL RECOMMENDATION

The team approves this critical design review.
The panel recommends manufacturing the first prototypes.
The UUB prototype is necessary to complete the design verification.

4. ITEMS RECOMMENDATION

4.1 Summary item discrepancy table

In the following table, a summary of RID is given with related priority

RID N°	WP	Priority	Short description / Comment
CDR-B-20150204-41	10	Low	Update AD1 and AD2
CDR-B-20150204-32	10	Low	Plan resources for trigger development year 4
CDR-B-20150204-06	10	Medium	Radio alternatives?
CDR-B-20150204-08	7	Low	Additional LED control output for plastic scintillators?
CDR-B-20150204-14	10	Low	Basic requirements documentation
CDR-B-20150204-16	10	Low	Decommissioning plan
CDR-B-20150204-27	10	Medium	Complete software specifications
CDR-B-20150204-01	10	Medium	Customs
CDR-B-20150204-09	10	Low	SDE-Co rent
CDR-B-20150204-10	10	Medium	Funding and currency conversion
CDR-B-20150204-15	10	Low	Risks organization and severity
CDR-B-20150204-04	**10**	**High**	Production split reliability impact
CDR-B-20150204-28	**10**	**High**	UUB: Derating analysis and flash mirror
CDR-B-20150204-30	**10**	**High**	Older components connected with UUB (solar panels, PMT, radio, sunsaver, TPCB…)
CDR-B-20150204-39	10	Low	Reliability evaluation
CDR-B-20150204-40	10	Medium	Tests – electrical verifications and ESD
CDR-B-20150204-17	**10**	**High**	ICD: Power budget – Acronyms – connectors names
CDR-EB-20150204-06	**5**	**High**	Level translator skew violate data skew requirements
CDR-B-20150204-37	10	Low	No planning alternatives – WP technical reports header and version
CDR-B-20150204-11	1 S	Medium	CAEN HV module information (reliability data, schematic…)
CDR-B-20150204-12	1	Medium	Check requirements conformity
CDR-B-20150204-19	1	Medium	60 MHz filter
CDR-B-20150204-13 CDR-B-20150204-20	**1** **1**	**High**	Front End amplifier chain
CDR-B-20150204-31	1	Medium	Front End Layout
CDR-B-20150204-21	**5**	**High**	ADC clock jitter
CDR-B-20150204-22	**1**	**High**	ADC external reference voltage
CDR-B-20150204-23	**1**	**High**	Front End simulation
CDR-B-20150204-24	1	Medium	Offset voltage drivers
CDR-B-20150204-25	5	Medium	FPGA LVDS I/O – I/O bank supply
CDR-B-20150204-33	1	Medium	Front End design choice and justification
CDR-EB-20150204-01	**1**	**High**	High gain noise level
CDR-EB-20150204-03	**1**	**High**	Front End – High gain amplifier behavior
CDR-EB-20150204-05	5	Medium	ADC clock
CDR-B-20150204-29	3	Low	Time tagging architecture not reported
CDR-B-20150204-34	3	Medium	GPS tests
CDR-B-20150204-26	4	Low	Slow control OFFSET
CDR-B-20150204-38	4	Low	Slow control maximum allowed input
CDR-B-20150204-02	5	Medium	UUB bill of material
CDR-B-20150204-03	5	Medium	UUB schematic and power protection
CDR-B-20150204-35	5	Medium	UUB ground schematic, lightning protection and ESD protection
CDR-B-20150204-06 CDR-B-20150204-07	5 5	Medium	UUB FPGA
CDR-B-20150204-18	**5**	**High**	UUB Power supply
CDR-B-20150204-36	5	Low	UUB PCB – layers identification
CDR-EB-20150204-02	5	Medium	Quad SPI flash reset behavior
CDR-EB-20150204-04	5	Medium	ADC clock and crosstalk

4.2 Review Item Discrepancy (RID):

WP10: Development Plan

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID- CDR-B-20150204-41
RID TITLE: Applicable document update	
AREA : Quality assurance – WP10	
Document title / Nº-Ref / chapter / page: AD1 and AD2	
DISCREPANCY: AD1 Pierre Auger Observatory Quality Assurance Plan, October 2000, V1 AD2 PAO SDE Quality Management Plan, SDE_QMP Rev 2002-04 not updated since 2000 and 2002 and for the SDE Update project	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: AD1 and AD2 must be updated (Quality is a continuous improvement).	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-32
RID TITLE: Trigger development – WP2	

AREA : Development plan – WP10

Document title / Nº-Ref / chapter / page: Development plan - WP10LPSC02J

DISCREPANCY:

No resources planned for the trigger development for year 4

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION :

Trigger is generally in continuous improvement. We recommend to plan resources for year 4 in order to work on the firmware updates

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP10: H/W Specifications

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-06
RID TITLE: Radio alternative	
AREA : H/W Specification – WP10	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -Old radio design: low data rate (Note: new radio from actual design are manufactured in the Netherland) -No radio alternative	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Propose an Ethernet powered radio alternatives (especially for infill region)	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Matthias KLEIFGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-14
RID TITLE: basics requirements justification	
AREA: H/W Specification – WP10	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -Basics requirements (120 MHz) not enough documented or explained	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Basics requirements (120 MHz signal sampling etc…) to justify by simulation of physics performance	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-16
RID TITLE: Decommissioning	
AREA: H/W Specification – WP10	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -Decommissioning plan not written for old Unified Board electronics. Some plans are to use UB for other projects R&D, test tank, extension… -Throw old UB is not allowed (contain lead)	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION : Write a decommissioning plan for old UB. Write a similar plan for future UUB	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP10: S/W Specifications

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-27
RID TITLE: S/W specification	
AREA: SW specification – WP10 - WP6	
Document title / Nº-Ref / chapter / page: OBSW specification /WP6LPS013A	
DISCREPANCY: -Software specification not complete	
INITIATOR RECOMMENDED SOLUTION	
PANEL RECOMMENDATION: Workgroup with software team to complete the specification. Use the return of experience of actual OS9000 software and Auger North software	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP10: Project Risks Analysis

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**			**SDEU CDR**
ORIGINATOR name.	COLONGES	Date: 04/02/2015	RID Nº: RID-CDR-B-20150204-01
RID TITLE: Customs			
AREA: Risk analysis – WP10			
Document title / Nº-Ref / chapter / page: Project Risk Analysis / WP10LPSC06C			
DISCREPANCY: -Customs and transport risk under estimated: risk of procedure change, new taxes, and delay…			
INITIATOR RECOMMENDED SOLUTION:			
PANEL RECOMMENDATION: - Establish a formal agreement with Argentinean government / customs			
Project Signature: System engineer: P. Stassi Date: 06/02/2015		Chairman Signature: S. Colonges Date: 04/02/2015	

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date : 04/02/2015	RID Nº: RID-CDR-B-20150204-09
RID TITLE: SDE-Co	
AREA: Risk analysis – WP10	
Document title / Nº-Ref / chapter / page: Project Risk Analysis / WP10LPSC06C	
DISCREPANCY: -Risk with long term SDE-Co building rent (depend on the owner)	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: - Buy the SDE-Co or establish a long term renting contract	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date: 04/02/2015	RID Nº: RID-CDR-B-20150204-10
RID TITLE: funding	
AREA: Risk analysis – WP10	
Document title / Nº-Ref / chapter / page: Project Risk Analysis / WP10LPSC06C	
DISCREPANCY: -Under evaluation of the risk funding (agencies funding uncertainties) -Margin when price are converted from Euros to Dollars	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: - Add a 30% margin when money conversion is necessary (not specific SDE problem, may be mitigated by US money) - Give a planning for longer path funding - Memorandum Of Understanding	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date : 04/02/2015	RID Nº: RID-CDR-B-20150204-15
RID TITLE: Risk organization	
AREA: Risk analysis – WP10	
Document title / Nº-Ref / chapter / page: Project Risk Analysis / WP10LPSC06C	
DISCREPANCY: -Risk are not organized into classes as described in 1.2.2 -Severity don't take into account detectability level	
INITIATOR RECOMMENDED SOLUTION: Severity = criticality*occurrence*detectability	
PANEL RECOMMENDATION: - Organize risks	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP10: FMECA - FDIR

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**			**SDEU CDR**
ORIGINATOR name.	COLONGES	Date : 04/02/2015	RID Nº: RID-CDR-B-20150204-04
RID TITLE: Split production			
AREA: Reliability – WP10			
Document title / Nº-Ref / chapter / page:			
DISCREPANCY: Production split between multiple production sites / country, will have high impact on reliability. Besides, split will generate important additional costs and will impact the planning INITIATOR RECOMMENDED SOLUTION:			
PANEL RECOMMENDATION: -Layout must be the same for some boards version -The assembly of pre-production boards must be performed on a single site in order to detect non conformities -Assembly instruction procedures and manufacturing tests must be the same for all produced board if the production must be split (not recommended) -Split production into 3 or 4 batches ➔ allows correcting non-conformities. Wait the delivery and inspection of the previous batch before starting further production (Even if batches produced in different site).			
Project Signature: System engineer: P. Stassi Date: 06/02/2015		Chairman Signature: S. Colonges Date: 04/02/2015	

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date : 04/02/2015	RID Nº: RID-CDR-B-20150204-28
RID TITLE: UUB - Derating analysis – Software corruption	

AREA: Reliability – WP10

Document title / Nº-Ref / chapter / page:

DISCREPANCY:

-Components rating have not been analyzed
-Protection against software corruption not described (Consider booting a recovery image of Linux in case of boot errors).

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:

- Perform derating analysis
- How software corruption is detected. How to switch to mirrored flash memory?

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date: 04/02/2015	RID Nº: RID-CDR-B-20150204-30
RID TITLE: Other components reliability	
AREA: Reliability – WP10	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: UUB will be connected with older component, designed for 20 years. All of them will have more than 10 years after UUB deployment.	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: - Maintenance or replacement of theses components (solar panel, TPCB, radio, PMT, sun saver…) must be evaluated.	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date: 04/02/2015	RID Nº: RID-CDR-B-20150204-39
RID TITLE: MTTF evaluation	

AREA: Reliability – WP10

Document title / Nº-Ref / chapter / page: FDIR Document – WP10LPSC10C

DISCREPANCY:

-Environmental constraints taken for the analysis not given in the report: Ambient temperature, temperature cycling, humidity, salt…
-Are all the reliability data come from MIL-HDBK-217F
-The MIL-HDBK-217F is obsolete (not updated since 20 years)
-Passives are not included in the criticality analysis
-Impact of interfaces, ESD protections, derating values?
-Unit for Item criticality (CR)? When a Cr value becomes critical? (table?)
-FPGA FIT: related power consumption? Related fill factor?

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:

- Add the passives + quartz + connectors
- Gives a global MTTF number
- Gives environmental constraints
- Use more recent reliability handbook if possible. Indicates when values come from manufacturer

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date: 04/02/2015	RID Nº: RID-CDR-B-20150204-40
RID TITLE: Tests – electrical verifications	
AREA: Tests – WP10	
Document title / Nº-Ref / chapter / page: AIT/AIV plan – WP10LPSC11D	
DISCREPANCY: -How the ESD test will be performed? -Verification matrix: be aware that you have the same copy/paste in 2.5 of WP10LPSC03H and in 7.5.1 of WP10LPSC11D. It's a little bit confused to paste this information in 2 different documents.	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: - Describes the facility used in order to perform the ESD test - In future design justification document, add the verification matrix with the additional column "validated" (Yes/No)	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP10: ICD

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-17
RID TITLE: Interface Control Document	
AREA: ICD – WP10	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -Power: 16,5 watts peak value. Mean value and margin not given. All the components have not been included in the power consumption analysis -Some acronyms are not explained (example: ASCII) or different acronyms are used to describe the same item -J21, J22, J25, J26 (PMT1Monit Vs PMTIMonit, PMT2Monit Vs PMTIIMonit), names risk of confusion (“case” sensitive), looks similar. -Risk of corrosion connectors	
INITIATOR RECOMMENDED SOLUTION: -Measure the mean total consumption including passives and finalized firmware. Compare with old UB mean consumption. Try to reduce the consumption in order to meet requirements -List all acronyms. Avoid multiple acronyms for same items -Change names for J25 and J26 connectors -Choose gold finished connectors (if available)	
PANEL RECOMMENDATION:	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP10: WBS Cost estimate: Remarks included in WP10: Risks analysis
WP10: Schedule

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Stéphane COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-37
RID TITLE: Planning scenarios	
AREA: Planning – WP10	
Document title / Nº-Ref / chapter / page: Schedule	
DISCREPANCY: -No alternative shown -No header and version on the document (some remark for costs and for WP technical reports)	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION : -Propose an alternative scenario in order to take into account possible funding delay -Add a header + version to the document	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP1: Analog PMT signal Processing

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**				**SDEU CDR**
ORIGINATOR name.	S Colonges	Date	04/02/2015	RID Nº: RID-B-20150204-11
RID TITLE: Small PMT				
AREA: Signal detection WP1-SPMT				
Document title / Nº-Ref / chapter / page:				
DISCREPANCY: -No schematic and reliability data for the commercial CAEN HV module -No ESS strategy described for the HV module -No information about base design. Protection against humidity (flying leads…)? Synergy with scintillators?				
INITIATOR RECOMMENDED SOLUTION:				
PANEL RECOMMENDATION : Ask information to CAEN. Ask for ESS for HV module. Add information about PMT base in the documentation. Check if single supply with multiple outputs is available.				
Project Signature: System engineer: P. Stassi Date: 06/02/2015			Chairman Signature: S. Colonges Date: 04/02/2015	

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**				**SDEU CDR**
ORIGINATOR name.	S Colonges	Date	04/02/2015	RID Nº: RID-B-20150204-12
RID TITLE: Front end performances				
AREA : Front End – WP1				
Document title / Nº-Ref / chapter / page:				
DISCREPANCY: -Specification conformity is not demonstrated and checked				
INITIATOR RECOMMENDED SOLUTION:				
PANEL RECOMMENDATION: Write a summary verification matrix to compare the different options. Write a Verification, Qualification and Validation plan				
Project Signature: System engineer: P. Stassi Date: 06/02/2015				Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**				**SDEU CDR**
ORIGINATOR name.	D Breton	Date	04/02/2015	RID Nº: RID-B-20150204-19
RID TITLE: 60 MHz filter				
AREA: Front End – WP1				
Document title / Nº-Ref / chapter / page:				
DISCREPANCY: -Low values of components may induce variability in the filter characteristics.				
INITIATOR RECOMMENDED SOLUTION: -Study the effect of low values components? Check the influence of potential parasitic capacitors or inductances. Determine if this effect is noticeable -Evaluate the interferences between magnetic field of neighbor inductances -Measure cross-talk between neighbor channels.				
PANEL RECOMMENDATION :				
Project Signature: System engineer: P. Stassi Date: 06/02/2015				Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. D Breton Date 04/02/2015	RID Nº: RID-B-20150204-13 and 20
RID TITLE: Front End amplifier chain	

AREA: Front End – WP1

Document title / Nº-Ref / chapter / page:

DISCREPANCY:

-No linearity measurement of the FE amplifier chain was shown
-No proof of high gain insensitivity to high gain saturation
-No real noise measurement result was shown
-Many solutions presented, but no real baseline

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:

Clearly present the options with thorough noise and linearity measurement for each (not only simulation)
Perform intermediate tests using prototype FE boards in order to compare solutions (best compromise). Integrate FE inside UUB after having validated the best option.

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**				**SDEU CDR**
ORIGINATOR name.	S Colonges	Date	04/02/2015	RID Nº: RID-B-20150204-31
RID TITLE: Front end layout				
AREA: Front End – WP1				
Document title / Nº-Ref / chapter / page:				
DISCREPANCY: -No information given about front end layout -No jitter measurement -Asymmetric lines input impedance?				
INITIATOR RECOMMENDED SOLUTION:				
PANEL RECOMMENDATION: Take care to analog/digital supply. Check the LVDS layout conformance with Xilinx recommendation (length…). Avoid ground loops and crosstalk. Low level noise require really small jitter, then measure the jitter and reduce if necessary				
Project Signature: System engineer: P. Stassi Date: 06/02/2015		Chairman Signature: S. Colonges Date: 04/02/2015		

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-B-20150204-22
RID TITLE: ADC external reference voltage	
AREA: Front End WP1	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -External reference voltage VREF demonstrates too big drift with temperature (75 µV/°C). ADC external reference voltage is not precise enough.	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: A single reference voltage LM4140 could replace the actual external reference voltage. Its drift is 3 µV/°C	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-B-20150204-23
RID TITLE: Front End simulation	

AREA : Front End – WP1

Document title / Nº-Ref / chapter / page:

DISCREPANCY:

-According to spice simulation the output noise density is 100 nV / $\sqrt{Hz}$. RMS noise at ADC input is $100nV \times \sqrt{60MHz} \approx 800\mu V$

- Front-end amplifier has a number of drawbacks (big noise, large power consumption, nonlinearity of low-gain channel during saturation of the hg channel, long recovery time from the saturation).
- Antialiasing filters are made with small caps (~10p), take care about their tolerances.

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION :

Consider another front end scheme (for example based on OPA847 Operational amplifier).
And/or use alternative scheme (Herve Lebbolo) presented in the report. It performs better in all respects. Modify filter design. Two poles can be implemented on the differential amplifier. Consider EMI susceptibility of the inductors used in the filters.

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-B-20150204-24
RID TITLE: Offset voltages drivers	

AREA : Front End – WP1

Document title / Nº-Ref / chapter / page:

DISCREPANCY:

Buffers driving OFFSET_1 and OFFSET_2 are not able to provide needed current at high frequencies.

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:
ADA4891 can be used, for example.

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Mathias KLEIFGES Date 04/02/2015	RID Nº: RID-B-20150204-33
RID TITLE: Trade off	

AREA: Front End – WP1 and WP1-SPMT

Document title / Nº-Ref / chapter / page:

DISCREPANCY:
-FE design chosen is not discussed version in last September meeting, but something between.
-When will the decision be made between PMT candidates
-Price difference?
-HV generation overlap with ASCII PMT?
-Set?
-What are the lessons learnt from Auger North SDE electronics?

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:

Design justification to be completed

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Jim BEATTY Date 04/02/2015	RID Nº: RID-EB-20150204-01
RID TITLE: High gain noise level	
AREA: Front End – WP1	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: High gain is factor 8 in voltage above specification. Overall noise factor is around 25 dB; Specifications implies 7 dB. Latest tests looks better.	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Need higher first stage gain with very low noise factor (3 dB). Consider unequal split to help.	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Hervé LEBOLLO Date 04/02/2015	RID Nº: RID-EB-20150204-03
RID TITLE: Amplifier behavior	
AREA : Front End – WP1	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: Behavior of amplifier high gain channel during saturation: -Increase of input impedance -Increase of input signal	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION : Need a buffer before	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP3: Time Tagging development

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Matthias Kleifges Date 04/02/2015	RID Nº: RID-CDR-B-20150204-29
RID TITLE: Time tagging	
AREA : WP3	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -Time tagging architecture / functional schematic not presented INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: -Include time tagging description inside the documentation	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Stéphane COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-34
RID TITLE: GPS	
AREA : WP3	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -The actual test from 0,5 to 35°C is not enough and not conform to Auger temperature range specification (-20 to + 70°C) -No information about M12M long term availability	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: -Test GPS behavior from -20°C (cold start of a tank during winter) to +70°C -Use a chronogram to describes the temperature cycling in the technical report -Take care about PPS fanout (the fanout was a problem in Auger South). See Auger south return of experience -Check with Ilotus the receiver availability	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP4: Slow Control Development

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-CDR-B-20150204-26
RID TITLE: Slow control Offset	
AREA: Slow Control – WP4	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: No possibility foreseen for remote uploading MSP430 SW from Linux side. INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Consider usage of bootstrap loader of the MSP430.	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-CDR-B-20150204-38
RID TITLE: Slow control maximum allowed input	
AREA: Slow Control – WP4	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: Multiplexer ADG608 at ADC inputs of the MSP430 can be damaged due to over-voltage	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Evaluate risk. Consider usage of over-voltage protection components.	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP5: UUB H/W Design and Integration

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. COLONGES **Date:** 04/02/2015	RID Nº: RID-CDR-B-20150204-02
RID TITLE: List of Component	
AREA: UUB – Bill of material – WP5	
Document title / Nº-Ref / chapter / page: SDEU IE00 Bill of material / SDE-002-002-IE00-EVAL04	
DISCREPANCY: -Packages / cases not listed -Component batches (date Code) not tracked -Purchasing not tracked -Different references for same components function/values	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: -Add a column for the package type in the BOM -Check that the BOM version is conform to the schematic version -Add columns to track date code, purchasing information (who, when, delivery date…) -Standardize the list of components. Reduce the quantity of equivalent references	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Patrick ALLISON Date 04/02/2015	RID Nº: RID-CDR-EB-20150204-06
RID TITLE: RGMII Interface spec violation	
AREA : ICD – WP5	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: Level translator violates data skew requirements of +/-50 ps -	
INITIATOR RECOMMENDED SOLUTION: Either move to new PHY or find another level translation solution which maintain skew requirements	
PANEL RECOMMENDATION:	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. COLONGES **Date:** 04/02/2015	RID Nº: RID-CDR-B-20150204-03
RID TITLE: UUB Schematic	

AREA: UUB – WP5

Document title / Nº-Ref / chapter / page:
WP5 Design report

DISCREPANCY:

-Schematics IE00: missing pages 7 to 12
-LTC4664: Power protection, hysteresis is not given
-No state-diagram of the slow-control system related to power management is presented. The Power-down, Power-save, Power-up battery voltage levels are not clearly defined (depending on its status entering power-save mode or shutting down the board completely).
-What is the fuse value and type?

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:
-Gives all schematics pages or change pages names
-Evaluate the lowest voltages admissible in order to avoid battery damage. Explain how the hysteresis is made: auto shut down value, and automatic power on value. The power on value must be higher than shut down value in order to avoid oscillation and allow battery charge. Panel suggest 24 Volts automatic power on and 22 Volts shut down (to be confirm with batteries characteristics)

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. COLONGES **Date :** 04/02/2015	RID Nº: RID-CDR-B-20150204-35
RID TITLE: UUB Lightning and EMC protection	

AREA : UUB – WP5

Document title / Nº-Ref / chapter / page:
WP5 Design report

DISCREPANCY:

-Not enough information about ground schematics, analog and digital supply
-Protection against lightning's (ground schematic?). Electrical field @ 1 km from a lightning?
-Reference of ESD suppressor protections? Protection level in kV?

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:
-Complete the technical report

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. COLONGES **Date :** 04/02/2015	RID Nº: RID-CDR-B-20150204-06 and 07
RID TITLE: UUB FPGA	

AREA: UUB – WP5

Document title / Nº-Ref / chapter / page:
WP5 Design report

DISCREPANCY:

-Missing FPGA firmware information ➔ big dependence with hardware
-Not enough free I/O Pin (98% used)
-No information about register and memory FPGA use
-No backup storage for the Zinq FW

-Is it possible to upgrade Zinq FW remotely

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:

-Check register number and memory size needed
-Evaluate if migration for biggest FPGA is necessary?
-Compiler should clear crosstalk with the actual pinout
-Plan a firmware design review
-Size of the FPGA programming file? (Time needed to download from the CDAS?)

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. COLONGES / MENSHIKOV **Date:** 04/02/2015	RID Nº: RID-CDR-B-20150204-18
RID TITLE: UUB Power supply	

AREA: UUB – WP5

Document title / Nº-Ref / chapter / page:
WP5 Design report

DISCREPANCY:

-DC-DC converters EMC, EMI, ripple and noise, accuracy and stability not measured
-Use of DC-DC converters for analog supplies looks dangerous. Analog supply has neither ripple filters nor LDO.

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:
-Power supply: full tests must be performed (EMI, EMC, ripple and noise, stability, accuracy…)
-Implement LDO regulator for analog supply
-Use screened inductors DC-DC converters
-Describe power management (power sequencing)

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. COLONGES **Date:** 04/02/2015	RID Nº: RID-CDR-B-20150204-36
RID TITLE: UUB PCB	

AREA: UUB – WP5

Document title / Nº-Ref / chapter / page:
WP5 Design report

DISCREPANCY:

-PCB layers identification

INITIATOR RECOMMENDED SOLUTION:

PANEL RECOMMENDATION:
-Write the layer number on each layer with a shift between each, in order to identify each layer by transparency

Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Patrick ALLISON Date 04/02/2015	RID Nº: RID-EB-20150204-02
RID TITLE: Quad SPI flash reset behavior	
AREA: UUB – WP5	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: See Xilinx design advisory (ARH 57744)	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: See Xilinx design advisory	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Zbigniew Date 04/02/2015	RID Nº: RID-EB-20150204-04
RID TITLE: Clock generator fractional mode	
AREA: UUB – WP5	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: Clock generator is coding in fractional mode (120 MHz / 25 MHz). Cristal 30 or 40 MHz would be better… LVDS lines terminated externally by a lot of 100 Ohms resistors	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Does the Xilinx compiler verify the crosstalk? ADC clocks outputs are set usually by the FPGA	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-B-20150204-21
RID TITLE: ADC clock jitter	
AREA: Front End clock – WP5	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -ADC clock 120 MHz has big jitter (>50ps). Is too high comparing the 500fs RMS requirement jitters for 120 MHz ADC.	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: A jitter cleaner AD9524 could be a solution (6 differential outputs) with VCXO from ON semiconductors of type NBVSPA015 ➔ provides a jitter <300 fs. The AD9524 needs an infrastructure for programming (internal EEPROM).	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Alexander Menshikov Date 04/02/2015	RID Nº: RID-B-20150204-25
RID TITLE: ADC LVDS outputs	
AREA: Front End - WP5	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: ADC data / clock LVDS outputs are terminated with 100 Ohms resistors. Zinq allows configure its LVDS inputs with internal 100 Ohms termination resistors, which reduce amount of components and ease PCB design.	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION: Consider instantiation of the termination inside Zinq.	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Dave NITZ Date 04/02/2015	RID Nº: RID-EB-20150204-05
RID TITLE: ADC clocks	
AREA: Front End Clock – WP5	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: Need to verify not using data clock from ADC works over whole temperature / voltage surge	
INITIATOR RECOMMENDED SOLUTION: Use clock from ADC to latch data	
PANEL RECOMMENDATION: Check the FPGA and ADC timing constraints	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

WP7: Calibration & Control Tools development: N/A

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. COLONGES Date 04/02/2015	RID Nº: RID-CDR-B-20150204-08
RID TITLE: Led flasher	
AREA: HW Specification – WP7	
Document title / Nº-Ref / chapter / page:	
DISCREPANCY: -Incomplete requirements for WCD / scintillator cross calibration using LED -No output implemented for additional led control	
INITIATOR RECOMMENDED SOLUTION:	
PANEL RECOMMENDATION : - Clarify requirements for cross calibration using LED (implement LED on scintillators?)	
Project Signature: System engineer: P. Stassi Date: 06/02/2015	Chairman Signature: S. Colonges Date: 04/02/2015

5 AUDIT

5.1 FIDES Audit checklist

The FIDES methodology identifies a list of recommendations, which, if followed, will facilitate construction of product reliability. This set of recommendations has been broken down into a set of questions.
The answer given to these questions permit learning about:
• A measurement of its ability to make reliable products,
• A quantification of the process factors used in the calculation models,
• The possibility of identifying improvement actions
For the CDR, we audit at this early stage the specification and design phase.

Audit question	Check / comment
Specifications	
Is there a financing item for the reliability studies? Have the needs been identified in terms of means and personnel?	Yes
Are the overall reliability requirements allocated to the subassemblies?	Yes
Is there a description and a characterization of the environment in which the system is going to be stored, transported, used and maintained?	Yes
System failures and degraded mode list have been established?	Yes
How is the demonstration of the system's reliability being considered?	
Has the System's utilization profile been defined for which the reliability performances are expected?	Yes
Context associated with a System's reliability requirements?	Yes
Is the feedback put to good use for maintaining a good level of confidence in the upholding of the reliability performances?	Yes
Is the reliability requirement expressed in quantitative terms?	Yes
Have the technical risks impacting reliability been identified?	Partially
Has a type of time measurement been identified (operating hours, flight hours, cycles, etc.) for the reliability performances?	Yes
Have the customer's requirements been identified, documented and traced?	Yes
Are the technological state of the art and the cost/performance optimization taken into account in the system's design at the time of the reliability requirement negotiations with the customer?	Yes
Is a system design review organized where the reliability aspects are examined?	Yes
Are the reliability requirements examined in a system requirements review?	CDR
Does the Operating Dependability discipline take part in the system's functional and detailed design?	Yes
Is the system's maintenance policy (requested by the customer) taken into account?	Yes
Has a System reliability plan been drawn up?	Partially
What process is implemented to ensure: the collection of technical events, the writing up of problem reports and the measurement of improving reliability? How are equipment changes managed?	To be defined

Design	
What steps have been taken to ensure that the personnel have the knowledge of the test means and of the standards and of how to interpret the measurements?	Training
Is the viewpoint of the various disciplines involved in engineering taken into account?	Yes
Are the subassembly's technical data available for the development of the production test?	TBD
Is there a list of substantiating items?	TBD
Is there a discipline procedures management system in place?	TBD
Is there a skill procedures management system in place?	TBD
Is there a preferential list of COTS items?	No
Is the most made of feedback to improve future designs?	Yes
Is there a database capitalizing on the reliability assessment studies?	Yes
Is there a database on the design history and substantiation?	TBD
Have the means been identified and implemented for protecting subassemblies during certain equipment production activities?	Yes
Have the technical risks impacting reliability been identified?	Yes
What is the process for constructing the reliability of the systems put in place in the company?	
Is it verified that test coverage is maximal and that it is based on the specification? Is there a substantiating document?	TBD
Are there procedures in place for verifying the design?	CDR
Is there a maintenance concept	Yes
Is a system design review organized where the reliability aspects are examined?	Yes
Is there a reliability management plans identifying the key skills (specialists)?	Partially
Is there a list of discipline recommendations on the handling and storage operations on the customer's premises?	Yes – to be documented
Is there an acceptance specification for the production tests?	Yes (to be update)
Is there a product/supplier qualification procedure?	No
Are there a definition of the test points and an application of the recommendations for the in-production tests?	No
Is there a procedure for qualifying the products and manufacturing process?	Yes – but to be completed
Are new components qualified before being used?	No
Is there analysis documentation for assessing the reliability?	Yes
Are there design rules in place for adapting the choice of a component for a given level of reliability?	Yes
Is there a formalized tool for calculating reliability? Is there a formalized reliability book (MIL, adjusted MIL, RDF, personal REX)?	Yes
Are the choices relative to test coverage documented?	
Are validated and recognized means of modeling used?	Yes

5.2 Design Review Checklists (DRC):

See in the following pages the Design Review Checklists, filled by the panel board after the review.

Design Review Checklist

Checklist Description: This checklist captures common elements that should be present in any design. It is presented during the Design Review process to stimulate thought, guide brainstorming, and to ensure the design being outlined contains all proper design considerations. As the project architecture, system, and application design is being reviewed, assess the design considerations that apply to your subject matter expertise and business/technical needs.

Project Name: SDEU	**Review Date: 04/02/2015**
Assessment and Recommendations: ☐ Approved without revision ☒ Approved with revisions (see Notes) ☐ Not approved	**Notes:**
Reviewer: S. Colonges	**Signature:**
Artifacts Reviewed: ☒ Technical Design Specification ☒ Implementation Plan	☒ Conceptual Architecture Review Checklist ☐ Requirements Traceability Matrix ☒ Other**:**

	General Design	Comments
☒	Does the design support both product and project goals?	
☒	Is the design feasible from a technology, cost, and schedule standpoint?	
☒	Have known design risks been identified, analyzed, and planned for or mitigated?	
☒	Are the methodologies, notations, etc. used to create and capture the design appropriate?	
☒	If possible, were proven past designs reused?	
☒	Does the design support proceeding to the next development step?	*Prototyping*

	Design Considerations	Comments
☒	Does the design have conceptual integrity (i.e., does the whole design tie together)?	
☒	Can the design be implemented within technology and environmental constraints?	
☒	Does the design use standard techniques and avoid exotic, hard-to-understand elements?	
☒	Is the design unjustifiably complex?	*Excepted some details*
☒	Is the design lean (i.e., are all of its parts strictly necessary)?	*Excepted some details*
☐	Does the design create reusable components if appropriate?	
☐	Does the design allow for scalability?	
☐	Are all time-critical functions identified, and timing criteria specified for them?	*FPGA firmware not described*
☒	Are the hardware environment completely defined, including engineering change levels and constraints?	
☐	Are the pre-requisite and co-requisite software and firmware clearly identified, including release levels and constraints?	*No data available*

Requirements Traceability		Comments
☒	Does the design address all issues from the requirements?	*Conformance matrix TBW*
☐	Does the design add features or functionality, which was not specified by the requirements (i.e., are all parts of the design traceable back to requirements)?	
☐	If appropriate, has requirements coverage been documented with a completed requirements traceability matrix?	
☒	Are all of the assumptions, constraints, design decisions, and dependencies documented?	*Most of*
☐	Have all reasonable alternative designs been considered, including not automating some processes in software?	*No other alternative has been presented (1)*
☒	Have all goals, tradeoffs, and decisions been described?	
☒	Have all interfacing systems been identified?	
☒	Are the error recovery and backup requirements completely defined?	*Not for the S/W and F/W*
☐	Have the infrastructure e.g. backup, recovery, checkpoints been addressed?	
Consistency		**Comments**
☐	Does the design adequately address issues that were identified and deferred at previous upstream levels?	*?*
☒	Is the design consistent with related artifacts (i.e., other modules, designs, etc.)?	
☐	Is the design consistent with the development and operating environments?	
Performance Reliability		**Comments**
☒	Are all performance attributes, assumptions, and constraints clearly defined?	
☒	If appropriate, are there justifications for design performance (i.e., prototyping critical areas or reusing an existing design proven in the same context)?	
Capacity Planning		**Comments**
☐	Does the design improve productivity?	*n/a*
☐	Is scalability development into the plan and is maintainable?	*n/a*
☐	Is Total Cost of Ownership (TCO) controlled or reduced?	*n/a*
Maintainability		**Comments**
☒	Does the design allow for ease of maintenance?	
☒	If reusable parts of other designs are being used, has their effect on design and integration been stated?	
Compliance		**Comments**
☒	Does the design follow all standards necessary for the system? (i.e., date standards)	*Almost*
☒	Have legal/regulatory requirements been assessed and accounted for?	

(1) What about the FE upgrade proposal from Zbigniew ? Need a justification for a new SDE design.

Design Review Checklist

Checklist Description: This checklist captures common elements that should be present in any design. It is presented during the Design Review process to stimulate thought, guide brainstorming, and to ensure the design being outlined contains all proper design considerations. As the project architecture, system, and application design is being reviewed, assess the design considerations that apply to your subject matter expertise and business/technical needs.

Project Name: SDEU	**Review Date: 04/02/2015**
Assessment and Recommendations: ☐ Approved without revision ☒ Approved with revisions (see Notes) ☐ Not approved	**Notes:**
Reviewer: D. Breton	**Signature:**
Artifacts Reviewed: ☒ Technical Design Specification ☒ Implementation Plan	☒ Conceptual Architecture Review Checklist ☐ Requirements Traceability Matrix ☒ Other**:**

	General Design	**Comments**
☒	Does the design support both product and project goals?	
☒	Is the design feasible from a technology, cost, and schedule standpoint?	
☒	Have known design risks been identified, analyzed, and planned for or mitigated?	
☒	Are the methodologies, notations, etc. used to create and capture the design appropriate?	
☒	If possible, were proven past designs reused?	
☒	Does the design support proceeding to the next development step?	*Prototyping*
	Design Considerations	**Comments**
☒	Does the design have conceptual integrity (i.e., does the whole design tie together)?	
☒	Can the design be implemented within technology and environmental constraints?	
☒	Does the design use standard techniques and avoid exotic, hard-to-understand elements?	
☒	Is the design unjustifiably complex?	*No, excepted some details*
☒	Is the design lean (i.e., are all of its parts strictly necessary)?	
☒	Does the design create reusable components if appropriate?	
☐	Does the design allow for scalability?	*Not at FPGA level*
☐	Are all time-critical functions identified, and timing criteria specified for them?	*FPGA firmware not described*
☒	Are the hardware environment completely defined, including engineering change levels and constraints?	
☐	Are the pre-requisite and co-requisite software and firmware clearly identified, including release levels and constraints?	*No yet*

Requirements Traceability		Comments
☒	Does the design address all issues from the requirements?	*Measurements to be done*
☐	Does the design add features or functionality, which was not specified by the requirements (i.e., are all parts of the design traceable back to requirements)?	
☐	If appropriate, has requirements coverage been documented with a completed requirements traceability matrix?	*Not yet*
☒	Are all of the assumptions, constraints, design decisions, and dependencies documented?	
☐	Have all reasonable alternative designs been considered, including not automating some processes in software?	*No other solution presented (1)*
☒	Have all goals, tradeoffs, and decisions been described?	*Besides point above*
☒	Have all interfacing systems been identified?	
☒	Are the error recovery and backup requirements completely defined?	
☐	Have the infrastructure e.g. backup, recovery, checkpoints been addressed?	
Consistency		**Comments**
☐	Does the design adequately address issues that were identified and deferred at previous upstream levels?	*No information about previous version*
☒	Is the design consistent with related artifacts (i.e., other modules, designs, etc.)?	
☒	Is the design consistent with the development and operating environments?	
Performance Reliability		**Comments**
☒	Are all performance attributes, assumptions, and constraints clearly defined?	
☒	If appropriate, are there justifications for design performance (i.e., prototyping critical areas or reusing an existing design proven in the same context)?	
Capacity Planning		**Comments**
☐	Does the design improve productivity?	*?*
☐	Is scalability development into the plan and is maintainable?	*?*
☐	Is Total Cost of Ownership (TCO) controlled or reduced?	*?*
Maintainability		**Comments**
☒	Does the design allow for ease of maintenance?	
☒	If reusable parts of other designs are being used, has their effect on design and integration been stated?	
Compliance		**Comments**
☒	Does the design follow all standards necessary for the system? (i.e., date standards)	*Quite well*
☒	Have legal/regulatory requirements been assessed and accounted for?	

(1)No other solution presented where they may exist. This should have been explained

Design Review Checklist

Checklist Description: This checklist captures common elements that should be present in any design. It is presented during the Design Review process to stimulate thought, guide brainstorming, and to ensure the design being outlined contains all proper design considerations. As the project architecture, system, and application design is being reviewed, assess the design considerations that apply to your subject matter expertise and business/technical needs.

Project Name: SDEU	**Review Date: 04/02/2015**
Assessment and Recommendations: ☐ Approved without revision ☒ Approved with revisions (see Notes) ☐ Not approved	**Notes:**
Reviewer: A. Menshikov	**Signature:**
Artifacts Reviewed: ☒ Technical Design Specification ☒ Implementation Plan	☒ Conceptual Architecture Review Checklist ☐ Requirements Traceability Matrix ☒ Other**:**

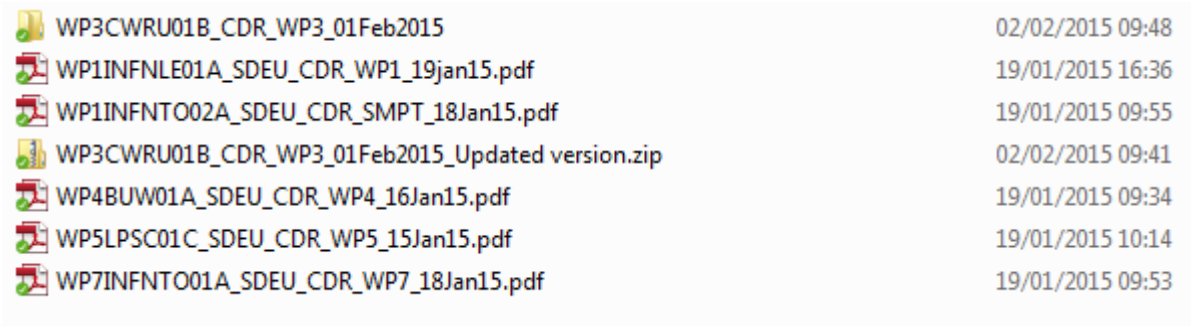
	General Design	**Comments**
☒	Does the design support both product and project goals?	
☒	Is the design feasible from a technology, cost, and schedule standpoint?	
☒	Have known design risks been identified, analyzed, and planned for or mitigated?	
☒	Are the methodologies, notations, etc. used to create and capture the design appropriate?	
☒	If possible, were proven past designs reused?	
☒	Does the design support proceeding to the next development step?	*Prototype*
	Design Considerations	**Comments**
☒	Does the design have conceptual integrity (i.e., does the whole design tie together)?	
☒	Can the design be implemented within technology and environmental constraints?	
☒	Does the design use standard techniques and avoid exotic, hard-to-understand elements?	
☒	Is the design unjustifiably complex?	*A few details*
☒	Is the design lean (i.e., are all of its parts strictly necessary)?	
☒	Does the design create reusable components if appropriate?	
☒	Does the design allow for scalability?	
☐	Are all time-critical functions identified, and timing criteria specified for them?	
☒	Are the hardware environment completely defined, including engineering change levels and constraints?	
☐	Are the pre-requisite and co-requisite software and firmware clearly identified, including release levels and constraints?	*No information*

Requirements Traceability		Comments
☒	Does the design address all issues from the requirements?	*Not completely*
☒	Does the design add features or functionality, which was not specified by the requirements (i.e., are all parts of the design traceable back to requirements)?	
☐	If appropriate, has requirements coverage been documented with a completed requirements traceability matrix?	
☒	Are all of the assumptions, constraints, design decisions, and dependencies documented?	
☒	Have all reasonable alternative designs been considered, including not automating some processes in software?	
☒	Have all goals, tradeoffs, and decisions been described?	
☒	Have all interfacing systems been identified?	
☒	Are the error recovery and backup requirements completely defined?	*Not for F/W and S/W*
☐	Have the infrastructure e.g. backup, recovery, checkpoints been addressed?	
Consistency		**Comments**
☐	Does the design adequately address issues that were identified and deferred at previous upstream levels?	
☒	Is the design consistent with related artifacts (i.e., other modules, designs, etc.)?	
☒	Is the design consistent with the development and operating environments?	
Performance Reliability		**Comments**
☐	Are all performance attributes, assumptions, and constraints clearly defined?	
☐	If appropriate, are there justifications for design performance (i.e., prototyping critical areas or reusing an existing design proven in the same context)?	
Capacity Planning		**Comments**
☐	Does the design improve productivity?	
☐	Is scalability development into the plan and is maintainable?	
☐	Is Total Cost of Ownership (TCO) controlled or reduced?	
Maintainability		**Comments**
☒	Does the design allow for ease of maintenance?	
☒	If reusable parts of other designs are being used, has their effect on design and integration been stated?	
Compliance		**Comments**
☒	Does the design follow all standards necessary for the system? (i.e., date standards)	
☒	Have legal/regulatory requirements been assessed and accounted for?	

The following table indicates the general data package provided for the CDR and used by the review board:

Designation	Reference	Revision
Section 01: Development Plan		
SDEU Development Plan	WP10LPSC02	J
Section 02: H/W Specifications		
SDEU Specifications	WP10LPSC03	H
Section 03: S/W Specifications		
SDEU OBSW Specification	WP6LPSC13	A
Section 04: Project Risks Analysis		
SDEU project Risks Analysis	WP10LPSC06	C
Section 05: FMECA - FDIR		
SDEU FMECA-FDIR	WP10LPSC10	C
Section 06: Tests Plan		
SDEU AIT-AIV Plan	WP10LPSC11	D
Section 07: ICD		
SDEU Electrical Interfaces Control Document	WP10LPSC05	E
SDEU Detectors Interfaces Control Document	WP10LPSC07	F
Section 08: WBS Cost estimate		
SDEU WBS	WP10LPSC08	J
Section 09: Schedule		
SDEU Project General Schedule	WP10LPSC04	K

Table 2a – Review data package for the CDR



End of document