Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. MENSHIKOV Date 04.02.15	RID N°: RID- CDR-B-20150204-21
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	
DISCREPANCY: (High priority) ADC clock 120MHz has big jitter (> 50ps). RMS jitter of 120MHz 12-bit ADC must be below 500fs	
INITIATOR RECOMMENDED SOLUTION: a jitte-cleaner AD9524 ~~pos~~ 6 differential outputs. With VCXO from ON-Semi of type NBVSPA15 ~~xx~~ it provides jitter below 300fs	
PANEL RECOMMENDATION :	
Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. MENSHIKOV Date 04.02.2015	RID N°: RID- CDR-B-20150204-22
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	
DISCREPANCY: (High priority) External reference voltage VREF demonstrates too big drift with temperature (~75μV/°C).	
INITIATOR RECOMMENDED SOLUTION: A single reference voltage IC of type LM4140 can replace the components (U34 + M1). The LM4140 has temperature drift 3ppm/°C (corresponds to 3μV/°C).	
PANEL RECOMMENDATION :	
Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	SDEU CDR
ORIGINATOR name. MENSHIKOV Date 04.02.2015	RID N°: RID- CDR-B-20150204-23
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	

DISCREPANCY: (High priority)
According to SPICE simulation the output noise density is $\approx 100\,nV/\sqrt{Hz}$.
RMS noise at ADC input is
$\approx 100\,nV/\sqrt{Hz} \cdot \sqrt{60\,MHz} \approx 800\,mV$.

INITIATOR RECOMMENDED SOLUTION:
Consider another front-end scheme
(for example, based on OA CPA847)

PANEL RECOMMENDATION :

Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. MENSHIKOV Date 04.02.2015	RID N°: RID- CDR-B-20150204-24
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	

DISCREPANCY:

Drivers of the offset voltages OFFSET-1 and OFFSET-2 must provide a big load current at high frequency. The operational amplifier M1 (LM224) is not able to do that.

INITIATOR RECOMMENDED SOLUTION:

AD4891 suits well for that application

PANEL RECOMMENDATION :

Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. MENSHIKOV Date 04.02.2015	RID N°: RID- CDR-B-20150204-25
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	

DISCREPANCY: (Wish)

ADC data/clock LVDS outputs are terminated with smp resistors 100 Ω.

Zinq allows to configure its LVDS inputs equipped with internal 100 Ω termination resistors.

INITIATOR RECOMMENDED SOLUTION:

Supply voltage of respective IO banks of the FPGA must be 2,5 V (instead of 1,8V)

PANEL RECOMMENDATION :

Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. MENSHIKOV Date 04.02.2015	RID N°: RID- CDR-B-20150204-26
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	

DISCREPANCY: (Wish)

The offset voltages OFFSET_1 and OFFSET_2 are set by resistive voltage deviders to certain value ~~at~~ during assembling.

INITIATOR RECOMMENDED SOLUTION:

If glow control µC MSP430 has spare DAC channels then they can be used for generating those offset voltages.

PANEL RECOMMENDATION :

Project Signature : Date:	Chairman Signature: Date: