



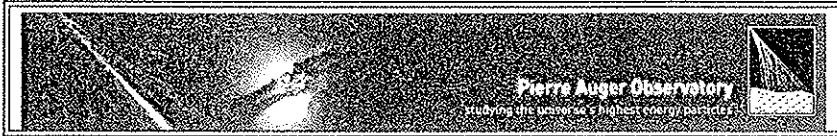
WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name. <i>MENSHIKOV</i>	Date <i>04.02.15</i>	RID N°: RID- <i>CDR-B-20150204-21</i>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>(High priority)</i> <i>ADC clock 120MHz has big jitter (&gt; 50ps),</i> <i>RMS jitter of 120MHz 12-bit ADC must be below 500fs</i>		
INITIATOR RECOMMENDED SOLUTION: <i>A jitter-cleaner AD9524 possess 6 differential</i> <i>outputs. With VCXO from ON-Semi of type</i> <i>NB VSPA15 <del>is</del> it provides jitter below 300fs</i>		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	



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07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name. <i>MENSHIKOV</i>	Date <i>04.02.2015</i>	RID N°: RID- <i>CDR-B-20150204-22</i>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: ( <i>High priority</i> ) <i>External reference voltage <math>V_{REF}</math> demonstrates too big drift with temperature (<math>\sim 75\mu V/^{\circ}C</math>).</i>		
INITIATOR RECOMMENDED SOLUTION: <i>A single reference voltage IC of type LM4140 can replace the components (U34 + M1). The LM4140 has temperature drift <math>3ppm/^{\circ}C</math> (corresponds to <math>3\mu V/^{\circ}C</math>).</i>		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	



WP10	LPSC	14C
07/01/15		10/13

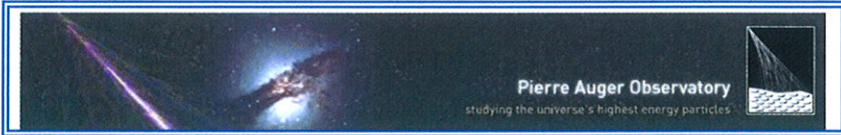
Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name: <b>MENSHIKOV</b>	Date: <b>09.02.2015</b>	RID N°: RID- <b>CDR-B-20150204-23</b>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: (High priority) According to SPICE simulation the output noise density is $\approx 100 \text{ nV}/\sqrt{\text{Hz}}$ . RMS noise at ADC input is $\approx 100 \text{ nV}/\sqrt{\text{Hz}} \cdot \sqrt{60 \text{ MHz}} \approx 800 \text{ mV}$ .		
INITIATOR RECOMMENDED SOLUTION: Consider another front-end scheme (for example, based on OA CPA847)		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	



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07/01/15		10/13

<b>Pierre Auger Observatory Upgrade Reviews</b>		<b>SDEU CDR</b>
<b>REVIEW ITEM DISCREPANCY</b>		
ORIGINATOR name. <i>MENSHIKOV</i>	Date <i>04.02.2015</i>	RID N°: RID- <i>CDR-B-20150204-24</i>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <del>Met</del> Drivers of the offset voltages OFFSET-1 and OFFSET-2 must provide a big <del>sink</del> load current at high frequency. The operational amplifier M1 (LM224) is not able to do that.		
INITIATOR RECOMMENDED SOLUTION: AD4891 suits well for that application		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	





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<b>Pierre Auger Observatory Upgrade Reviews</b> <b>REVIEW ITEM DISCREPANCY</b>		<b>SDEU CDR</b>
ORIGINATOR name: <i>MENSHIKOV</i>	Date: <i>04.02.2015</i>	RID N°: RID- <i>CDR-B-20150204-25</i>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>(Wish)</i> <i>ADC data/clock LVDS outputs are terminated with 50Ω resistors 100Ω.</i> <i>Zing allows to configure its LVDS inputs equipped with internal 100Ω termination resistors.</i>		
INITIATOR RECOMMENDED SOLUTION: <i>Supply voltage of respective IO banks of the FPGA must be 2,5V (instead of 1,8V)</i>		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	



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07/01/15		10/13

<b>Pierre Auger Observatory Upgrade Reviews</b>		<b>SDEU CDR</b>
<b>REVIEW ITEM DISCREPANCY</b>		
ORIGINATOR name: <i>MENSHIKOV</i>	Date: <i>04.02.2015</i>	RID N°: RID- <i>CDR-B-20150204-26</i>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>(Wish)</i> <i>The offset voltages OFFSET_1 and OFFSET_2 are set by resistive voltage dividers to certain value <sup>during</sup> <del>at</del> assembling.</i>		
INITIATOR RECOMMENDED SOLUTION: <i>If glow control µC MSP430 has spare DAC channels then they can be used for generating those offset voltages.</i>		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	