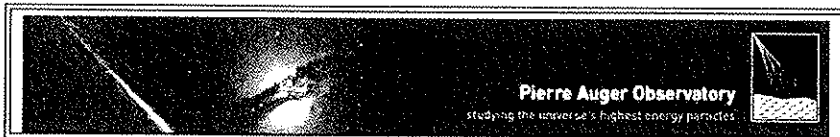




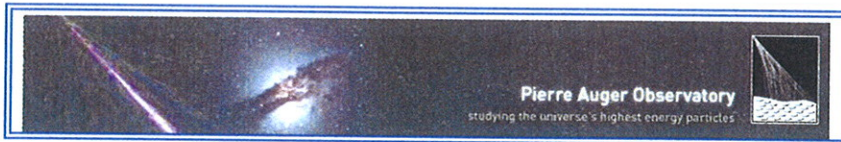
WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name: <i>J. Beatty</i>	Date <i>04/2/15</i>	RID N°: RID- <i>CDR-EB-20150204-01</i>
RID TITLE: <i>High Gain Noise Level</i>		
AREA : <i>WP1</i>		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>High gain noise is factor 8 in voltage above specification. Overall noise factor is ~25 dB; spec implies ~7 dB. Need higher first stage gain w/ very low (~3dB) noise factor.</i>		
INITIATOR RECOMMENDED SOLUTION: <i>Latest tests look better. Consider unequal split to help. Perhaps Herve has solved this with low power.</i>		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	



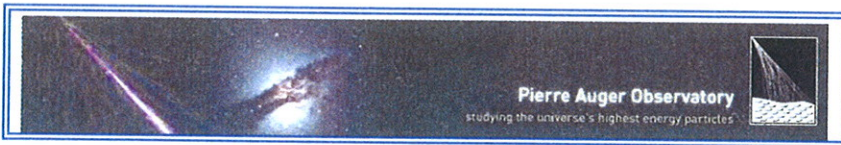
WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name: <i>Patrick Allison</i>	Date: <i>2/4/15</i>	RID N°: RID- <i>CDR-EB-20150204-02</i>
RID TITLE:		
AREA: <i>Quad SPI Flash reset behavior</i>		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>See Xilinx Design Advisory ^{AR#} 57744 (and email).</i>		
INITIATOR RECOMMENDED SOLUTION: <i>See email.</i>		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	



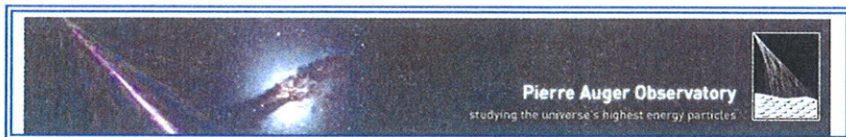
WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name. <i>Lehlobo Hlave</i>	Date <i>04/2/15</i>	RID N°: RID-
RID TITLE:		<i>CDR-EB-20150204-03</i>
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY:		
<p><i>Behaviour of first amplifier of high gain channel during saturation</i></p> <p><i>→ increase of input impedance</i></p> <p><i>→ increase of input signal</i></p>		
INITIATOR RECOMMENDED SOLUTION:		
<p><i>- need a buffer before</i></p>		
PANEL RECOMMENDATION :		
Project Signature :	Chairman Signature:	
Date:	Date:	



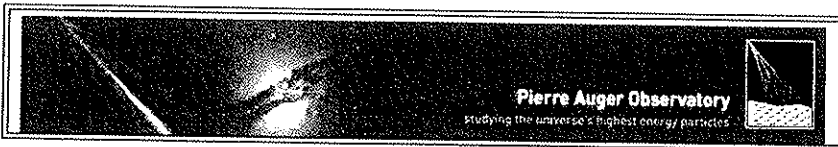
WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name. 1 <i>Zbigniew Sredzlow</i>	Date <i>04.02.2015</i>	RID N°: RID- <i>CDR-EB-20150204-04</i>
RID TITLE:		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>Clock generator is working in fractional mode $\frac{120 \text{ MHz}}{25 \text{ MHz}}$. Recommended integer mode \rightarrow crystal 30 MHz or 40 MHz</i>		
<i>LVDS lines terminated externally by a lot of 100 Ohms resistors \rightarrow recommended OCT</i>		
INITIATOR RECOMMENDED SOLUTION: <i>Does the Xilinx compiler verify the crosstalk between LVDS and Single Ended pins (SE) ?</i>		
PANEL RECOMMENDATION: <i>ADC clocks (outputs) are not used by the FPGA to adjust the maximal stable area per DAA. Recommended to use ADC output clocks connected to input PLLs for each ADC chip.</i>		
Project Signature : Date:	Chairman Signature: Date:	



WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name: <i>Nitz</i>	Date: <i>4-Feb</i>	RID N°: RID- <i>CDR-EB-20150204-05</i>
RID TITLE: <i>ADC clocks</i>		
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: <i>Used to verify not using data clock from ADCs works over whole temp & voltage range - for</i>		
INITIATOR RECOMMENDED SOLUTION: <i>Use clocks for ADC to latch data</i>		
PANEL RECOMMENDATION : <i>We recommend to use same clock to latch data. Carefully check the FPGA and check for timing constraints</i>		
Project Signature : Date:	Chairman Signature: Date:	



WP10	LPSC	14C
07/01/15		10/13

Pierre Auger Observatory Upgrade Reviews REVIEW ITEM DISCREPANCY		SDEU CDR
ORIGINATOR name: Patrick Allart	Date 2/5/15	RID N°: RID-
RID TITLE: RGMII interface spec violation		CDR-EB-20150204-06
AREA :		
Document title / N°-Ref / chapter / page:		
DISCREPANCY: See e-mail; level translator violates check to data data skew requirements of ± 50 ps.		
INITIATOR RECOMMENDED SOLUTION: Either move to new PHY or find another level translation solution which maintains skew requirements.		
PANEL RECOMMENDATION :		
Project Signature : Date:	Chairman Signature: Date:	