Pierre Auger Observatory Upgrade Reviews
REVIEW ITEM DISCREPANCY

SDEU CDR

ORIGINATOR name. J. Beatty Date 04/2/15

RID Nº: RID- CDR-EB-20150204-01

RID TITLE: High Gain Noise Level

AREA : WP1

Document title / Nº-Ref / chapter / page:

DISCREPANCY:

High gain noise is factor 8- in voltage above specification. Overall noise factor is ~25 dB; spec implies ~7 dB.

Need higher first stage gain w/ very low (~3dB) noise factor.

INITIATOR RECOMMENDED SOLUTION:

Latest tests look better.

Consider unequal split to help.

Perhaps Herve has solved this with low power

PANEL RECOMMENDATION :

Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Patrick Allison Date 2/4/15	RID N°: RID- CDR-EB-20150204-02
RID TITLE:	
AREA : Quad SPI Flash reset behavior	
Document title / N°-Ref / chapter / page:	
DISCREPANCY: See Xilinx Design Advisory AR# 57744 (and email).	
INITIATOR RECOMMENDED SOLUTION: See email.	
PANEL RECOMMENDATION :	
Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Lahlah Hervé Date 04/2/15	RID N°: RID- CDR-EB-20150204-03
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	
DISCREPANCY: Behavior of first amplifier of high gain channel during saturation → increase of input impédance → increase of input signal	
INITIATOR RECOMMENDED SOLUTION: - need a buffer before	
PANEL RECOMMENDATION :	
Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Zbigniew Szadkowski Date 04.02.2015	RID N°: RID- CDR-EB-20150204-04
RID TITLE:	
AREA :	
Document title / N°-Ref / chapter / page:	

DISCREPANCY:

Clock generator is working in fractional mode $\frac{120\ MHz}{25\ MHz}$. Recommended integer mode → crystal 30 MHz or 40 MHz

LVDS lines terminated externally by a bat of 100 Ohms resistors → recommended OK

INITIATOR RECOMMENDED SOLUTION:

Does the Xilinx compiler verify the crosstalk between LVDS and Single Ended pins (SE)?

PANEL RECOMMENDATION :

ADC clocks (outputs) are not used by the FPGA to adjust the maximal stable area per DAQ. Recommended to use ADC output clocks connected to input PLLs for each ADC chips.

Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews **REVIEW ITEM DISCREPANCY**	**SDEU CDR**
ORIGINATOR name. Nick Date 4-Feb	RID N°: RID- CDR-EB-20150204-05
RID TITLE: ADC clocks	
AREA :	
Document title / N°-Ref / chapter / page:	
DISCREPANCY: Need to verify not using Data clock from ADCs works over whole temp & voltage range. ~~For~~	
INITIATOR RECOMMENDED SOLUTION: Use clocks from ADC to latch Data	
PANEL RECOMMENDATION : We recommend to use same clock to latch data. Carefully check the FPGA and check for timing constraints	
Project Signature : Date:	Chairman Signature: Date:

Pierre Auger Observatory Upgrade Reviews

REVIEW ITEM DISCREPANCY

SDEU CDR

ORIGINATOR name. Patrick Allison Date 2/5/15

RID N°: RID-CDR-EB-20150204-06

RID TITLE: RGMII interface spec violation

AREA :

Document title / N°-Ref / chapter / page:

DISCREPANCY: See e-mail: level translator violates ~~clock to~~ data skew requirements of ±50 ps.

INITIATOR RECOMMENDED SOLUTION:

Either move to new PHY or find another level translation solution which maintains skew requirements.

PANEL RECOMMENDATION :

Project Signature : Date:	Chairman Signature: Date: