Pierre Auger Observatory

Surface Detector Electronics Upgrade SPECIFICATION

Abstract:
The SD electronics will be upgraded to increase its functionalities, capabilities and reliabilities This document describes the complete requirements needed for the upgrade.

Document written by:	P. Stassi Project System engineer	*Agreed by:*	T. Suomijärvi Task leader
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Table of Content

ACRONYMS

ADC	Analog to Digital Converter
BGA	Ball Grid Array
BSRU	Base Station Radio Unit
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
EAS	Extensive Air Shower
ER	Environmental Requirement
FDIR	Failure Detection, Isolation and Recovery
FPGA	Field Programmable Gate Array
FR	Functional Requirements
Fs	Full scale
GPS	Global Positioning System
ICD	Interfaces Control Document
IR	Interface Requirements
LED	Light Emitting Diode
LSB	Low Significant Bit
LVDS	Low Voltage Differential Signaling
Msp/s	Mega samples per second
n/a	non applicable
OR	Operational Requirements
OS	Operating System
PAO	Pierre Auger Observatory
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PMT	PhotoMultiplier Tube
PR	Physical Requirements
QR	Quality Requirements
RD	Reference Document
RDA	Research and Development Array
RF	Radio Frequency
RMS	Root Mean Square
SD	Surface Detector
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronics Upgrade
SR	Support Requirements
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TPCB	Tank Power Control Board
UB	Unified Board
UC	Upgrade Committee
USB	Universal Serial Bus
USB OTG	USB On-The-Go
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VM	Verification Matrix
WBS	Work Breakdown Structure
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
01	A	04/12/12	P. Stassi	1st DRAFT
01	B	19/12/12	P. Stassi	2nd DRAFT for approbation
01	C	11/01/13	T. Suomijarvi	1st diffused issue CB corrections
01	D	14/02/13	T. Suomijarvi	Update after Orsay meeting
01	E	18/03/13	T. Suomijarvi	Update after Col. Meeting @ Malargue
03	A	04/04/13	T. Suomijarvi	Change of document reference and file name
03	B	09/04/13	T. Suomijarvi	Update after phone meeting of 08 April 2013
03	C	06/06/13	T. Suomijarvi	Update after phone meeting of May 2013 @ Lisbon
03	D	07/10/13	T. Suomijarvi	Minor updates – Connectors pin out update
03	E	10/11/13	P. Stassi	Update after Orsay meeting 24-25 Oct 2013
03	F	23/01/2014	P. Stassi	J91-J92 connector pin-out modification
03	G	24/03/2014	P. Stassi	Verification Matrix update
03	H	27/11/14	P. Stassi	Update after Col. Meeting Nov. 2014 + ASCII interfaces
03	I	14/10/16	P. Stassi	Minors changes before Auger prime CDR

1 INTRODUCTION

The actual studies and results of the experimental data produced today at the Pierre Auger Observatory suggest new needs for capabilities, especially for the SD electronics (SDE). This document will review the complete requirement list for the SDE Upgrade (SDEU), including those relative to these new functionalities.

The system, concerned by the present requirements document can be defined in reference to the present (old) design of SD electronics (RD1) as:

- Unified Board
- Front End
- LED Flasher
- Environmental sensors
- GPS System
- Additional PMT

(Existing PMT unit will not be considered as well as the TPCB and the BSRU, Base Station Radio Unit)

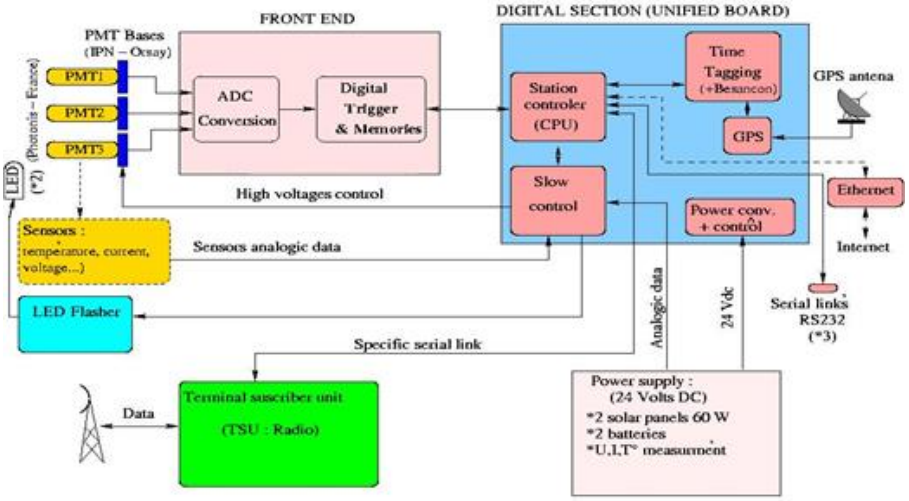


Figure 1a - diagram representing the present design of the SDE

The main component of the SDEU is the Upgraded Unified Board and it will be labeled in the present document "**UUB**".

1.1. Reference Documents

RD1 The Pierre Auger project, Technical Design Report, March 2004
RD2 Pierre Auger Project: RS-232 Communication Protocol, October 2002, V2.3
RD3 Pierre Auger Observatory Quality Assurance Plan, October 2000, V1
RD4 PAO SDE Quality Management Plan, SDE_QMP Rev 2002-04
RD5 existing UB mechanical housing description, no references
RD6 Small PMT, A proposal to extend the dynamic, range of the Auger SD for operations beyond 2015, M.Aglietta, A.Castellina, L.Latronico, S.Maldera, C.Morello, INAF and INFN, Torino, Italy. Initial draft release: February 12, 2013
RD7 Hatch Cover design, 6-20-02 Rev B, FNAL ref 5520.000-ME-360254
RD8 The Pierre Auger Observatory Upgrade, Preliminary Design Report, April 17, 2015

2 REQUIREMENTS

The Upgraded Unified Board (UUB) shall have the following requirements:

2.1. Functional requirements (FR)

(Representing what the UUB must do).

2.1.1. PMT signal conditioning and digitization

FR11: The UUB shall processes analog anode signals from the three PMTs. A low and high gain signal for each PMT shall be conditioned and digitized.

FR12: The total RMS integrated noise at the ADC input shall not exceed 0.5 LSB.

FR13: The UUB shall digitize the PMTs anode signals at a sampling frequency of 120 Msp/s with a resolution of 12 bits minimum with the adapted conditioning and gain circuitry.

FR14: Adapted anti-aliasing filters shall be implemented for each PMT signal inputs (60Mhz at -3dB) (<5% single time bin aliasing noise)

FR15: The UUB shall process analog signals from 2 additional PMTs from ASCII detector in 3 analog channels, one low gain for one of the 2 PMTs (or summation) and 2 high gains.

FR16: The high gain/low gain ratio shall be of 32.

FR17: The UUB shall processes analog anode signals from the fourth small additional PMT (RD6, the purpose is to increase the overall energy dynamic range).

2.1.2. Storage and Trigger construction

(current design RD1, page 222)

FR21: The trigger/memory circuitry shall evaluate the high-gain output of each PMT every 8.3 ns for interesting trigger patterns (see FR26), store the data in buffer and inform the micro-processor circuitry.

FR22: The trigger/memory circuitry shall generate a first level trigger based upon hardware analysis of the high gain PMT channel waveforms. The UUB micro-processor software shall imposes additional constraints to generate a level 2 trigger signal.

FR23: The goal of the first level trigger shall be to trigger efficiently on UHE cosmic ray air showers of energy $>10^{19}$eV, while simultaneously rejecting lower energy

showers and minimizing composition dependent trigger biases, within a rate constraint of 100 Hz.

FR24: The level 1 trigger shall be designed to be flexible and eventually modifiable in the future

FR25: The level 1 trigger shall start waveforms recording during 19.2 µs.

FR26: The triggers to be implemented are:
- Single bin (threshold) trigger
- Time-over-threshold (ToT) trigger
- Time-over-threshold-deconvolved (ToTd) trigger
- Multiplicity-of-positive-steps (MoPS) trigger
- Asymmetry based trigger
- External trigger input
- Shower memory buffers
- Muon memory buffers (& associated trigger)
- Scalers
- AMIGA trigger
- GPS synchronized trigger with specified delay from 1 PPS (for fake events and LED trigger)

FR27: The level 1 trigger shall provide signal to Time-Tagging circuitry allowing time step of trigger and determination of absolute time of each ADC bin.

2.1.3. Time Tagging

FR31: The UUB shall able to time tag each events, using the information given by a commercial GPS unit and a logic circuitry (in FPGA) based on the existing design, described in the RD1 document, point 2.2.3.4

FR32: The time tagging unit shall have a resolution of 4 ns or better, stable in temperature better than 5%.

2.1.4. Event Building and Processing

FR41: The UUB shall have a micro-processor able to perform the following tasks:
- Level 2 Trigger
- Data acquisition and event building with double buffering and recording
- Calibration process including analog inputs base line monitoring
- Data compression to fit the communication flux limit
- Communication with the slow control management unit.

2.1.5. The Slow Control management

FR51: The UUB shall have a slow control unit, allowing measurement and monitoring of at least 64 x 0 to 5 Volts analog input signals coded over 12 bits (can be multiplexed) and 8 logic inputs. Number of channel shall accommodate the designs for additional ASCII detector.

FR52: The UUB shall have a slow control unit able to generate at least 8 x 0 to 2.5 Volts analog buffered output signals coded from 12 bits and 8 logic buffered outputs.

FR53: The UUB shall have a slow control unit able to monitor internal parameters to perform a failure detection, isolation and recovery (FDIR) process on onboard power supplies and batteries voltage protection over 35 V and under 22 V).

FR54: The UUB slow control unit shall be able to manage all existing SDE environmental sensors (RD1) and additionally, a water temperature sensor and an atmospheric pressure sensor.

2.1.6. Calibration management

FR61: The UUB shall have a light generator unit (LED controller) able to generate two adapted signals with at least an amplitude of 20 Volts towards the two foreseen light devices (LED driver). The signal shall be controlled in time with a resolution of 4 ns and shall be synchronized to the time tagging signal (1PPS).

FR62: The light devices (LED driver) shall have at least the same specifications of the existing device.

FR63: The light generator unit (LED controller) and light devices (LED driver) shall measure the linearity of the SD photomultipliers (PMTs) over the full dynamic range of their acquisition channels, using the “two LEDs technique”.

FR64: The light generator unit (LED controller) and light devices (LED driver) shall measure the amplification ratio between overlapping acquisition channels, low and high gain of the SD PMT and the ASCII detector.

FR65: The light generator unit (LED controller) and light devices (LED driver) shall be able to create artificial EAS events of different topology on the ground SD array in order to:
- check the ACQ response for different event pattern,
- check the event reconstruction.

2.1.7. Communication management

FR71: The UUB shall include communication capabilities adapted to the existing unit (see Interfaces Requirements section) based on serial links.

FR72: The UUB shall include Ethernet communication capability.

FR73: The UUB shall include USB and USB OTG communication capability.

FR74: The UUB shall include digital communication capability for other detector systems, including synchronization signal.

2.1.8. Power supplies management

FR81: The UUB shall be able to produce all needed internal power supplies, regulated and stabilized, filtered and protected, from a single input of 24 Volts nominal but varying from 18 to 30 Volts.

FR82: The UUB internal power supplies shall be voltage monitored by the slow control unit (FR53).

2.2. Configurational requirements (CR)

(Representing the parts which compose the SDEU)

CR01: Each part of the UUB shall be contained in a single printed circuit board, excepted for the commercial GPS board, light generators (LED controller shall be on UUB PCB) and the mechanical housing.

CR02: The SDEU shall be composed at the minimum of the following components:

- **The PMTs signal Conditioning**
  - Amplifiers, filters, signal conditioning
- **The PMTs signal Digitizing**
  - ADCs
- **The Storage and Trigger construction**
  - Trigger algorithm in FPGA
- **Event Building and Processing**
  - CPU, memories, OS and software
- **The Slow Control management**
  - Environmental sensors reading, PMTs high voltages control and voltage and current monitoring, solar power system monitoring.
- **Calibration management**
  - light generators and light generators management
- **The Time Tagging**
  - Commercial GPS and time tagger in FPGA
- **Communication links management**
  - Serial, Ethernet, USB, external detectors digital interface
- **Power supplies management**
  - DC converters, filters and protections
- **Mechanics**
  - Housing, front panel, cables and connectors

2.2.1. *Product Breakdown Structure, (PBS)*

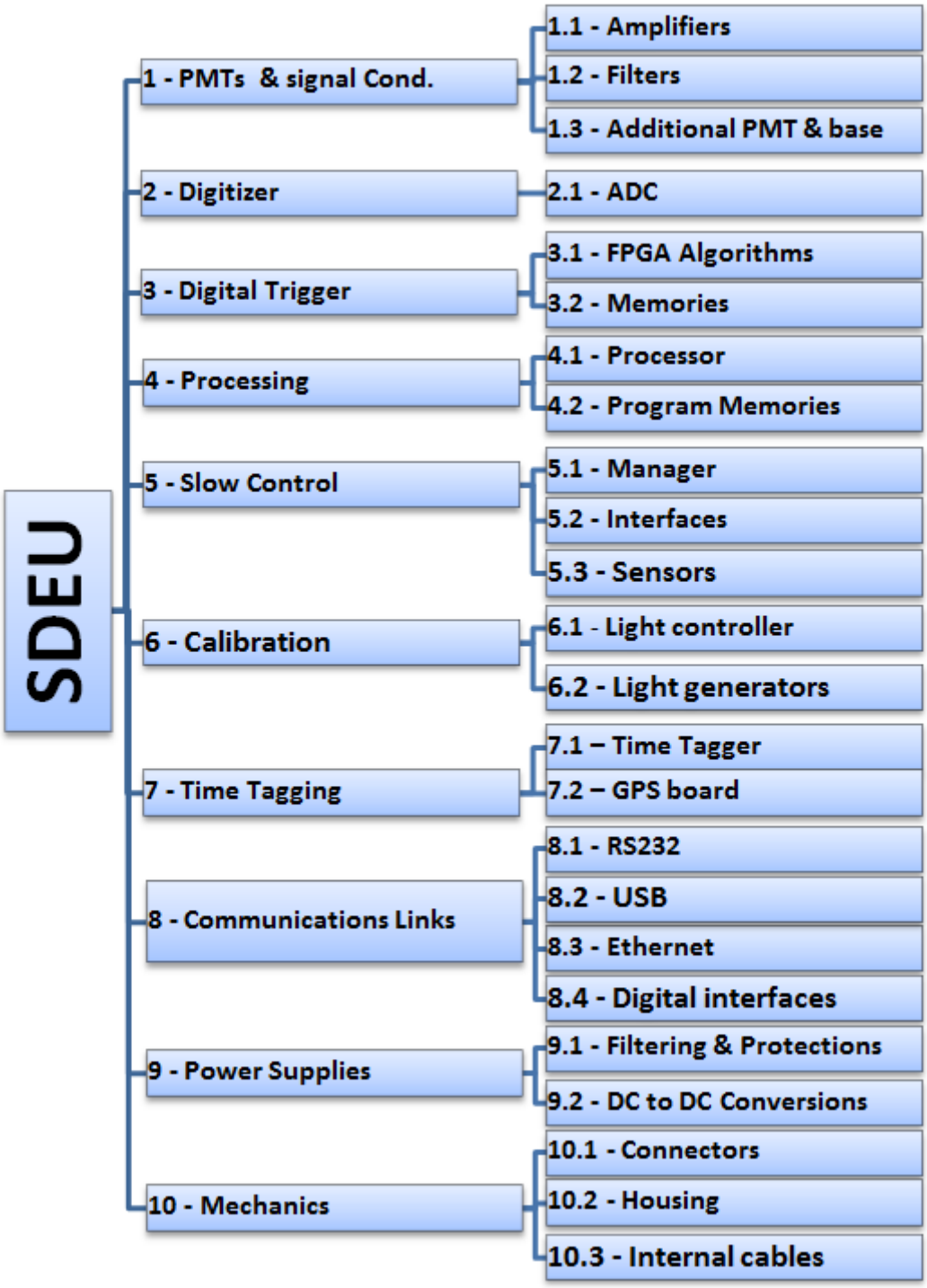


Figure 2.2.1a – Product Breakdown Structure

2.2.2. PBS#1, PMT & signal conditioning

CR11: The PMTs signal conditioning unit shall be composed of analog discrete components to perform the low noise amplification and filtering functionalities from the actively split PMT anode signals.

2.2.3. PBS#2, PMT signal digitizing

CR21: The Digitizer unit shall be composed of a number of commercial ADC equivalents to the number of analog inputs or split inputs (dual ADC chips with LVDS outputs are recommended).

2.2.4. PBS#3, Storage and trigger construction

CR31: The Digital Trigger unit shall be implemented in the unique FPGA component, following the architecture described in figure *2.2.4.a* below:

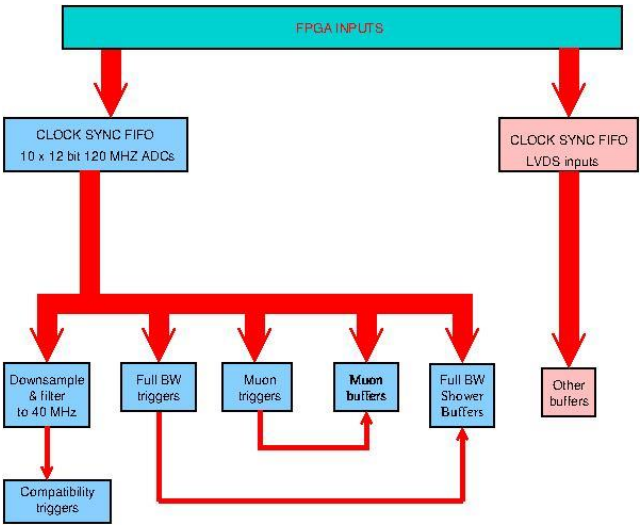


Figure 2.2.4a – Trigger architecture

CR32: External input and output Trigger signal shall be implemented (see Interfaces Requirements).

CR33: Memory minimum size requirements shall follow the values described in the table *2.2.4.b* below:

Item	# chan.	buffers /chan	# bits /bin	# bins /buffer	# bits extended	Notes
Shower memory buffer	6	2	16	2304	442368	Conservative – assume 16 bits for each 12 bit word
Slow ADC channel buffers	3	2	16	768	73728	Conservative – assume 16 bits for each 12 bit word
Muon buffers	3	2	16	3840	368640	Assume 64 bins/muon and 20ms long buffers
External	1	2	32	2304	147456	
TOTAL					**1,032,192**	

Table 2.2.4b – memory size requirement

2.2.5. PBS#4, Processing

CR41: The Processing unit shall be composed of a hardcore processor in the unique FPGA component, with adapted circuitry and memories.

CR42: The Processing unit shall have an adapted random access memory size of 512 Mo at the minimum.

CR43: The Processing unit shall have an adapted flash memory.

CR44: The Processing unit shall works under a micro-Linux operating system

CR45: The Processing unit shall have the adapted interfaces to be able to communicate with the other UUB units and the external world.

2.2.6. PBS#5, Slow control

CR51: The Slow Control unit shall be composed of separate (from the main processor) micro controller, ADCs, DACs and associated circuitry on the UUB board.

CR52: The Slow Control unit shall have analog inputs with 10 Kilo-Ohms impedance

CR53: The Slow Control unit shall include the water temperature and atmospheric pressure sensors and all existing sensors (RD1).

CR54: The Slow Control unit shall have a direct USB communication link (see Interface Requirements).

2.2.7. PBS#6, Calibration management

CR61: The Calibration unit shall include a light generator unit (LED controller) implemented on the UUB PCB, able to provide 20 Volts amplitude pulses. Controlled directly by the processing unit (FPGA).

CR62: The Calibration unit shall include an external dual light device adapted for SD PMT calibration purpose and ASCII detector (LED driver).

2.2.8. PBS#7, Time tagging

CR71: The Time Tagging unit shall be composed of a commercial, timing dedicated, GPS board[1] and a time tagging algorithm implemented in the unique FPGA.

2.2.9. PBS#8, Communications links

CR81: The UUB shall be able to manage at least 1 serial connection RS-232 type to communicate with the BSRU (radio).

CR82: The UUB shall be able to manage one Ethernet connection.

CR83: The UUB shall be able to manage 2 USB (2.0) and one USB-OTG connection.

CR84: The UUB shall be able to manage 2 digital connections for other detector systems, including synchronization signal, slow control and 24V power supply (CR93).

2.2.10. PBS#9, Power Supplies

CR91: The power supplies unit shall be composed of adapted to design DC to DC converters with the following requirements:
- Efficiency better than 80% (90% recommended)
- Large input range, from 18 to 30 Volts (24V nominal)
- Low ripple noise, less than 20mV

CR92: The 12V power supplies for PMTs bases and BSRU (radio) shall be separated (to avoid eventual failure propagation).

CR93: 24 Volts, filtered, non-regulated and controlled shall be provided on the extensions connectors.

2.2.11. PBS#10, Mechanics

CR101: The mechanical housing shall be composed of an aluminum extruded RF proof box, identical to the existing design (the existing box can be reused) and a metallic front panel, adapted to the new connectors type and their disposition.

[1] E.g., or M12M Timing Oncore™ from I-Lotus.

2.3. Interface requirements (IR)

(Representing the interfaces between the UUB parts and external world).

2.3.1. Electrical Interfaces

IR11: All the electrical interfaces between the UUB and the PMTs shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2 (excepted for the dynode connectors).

IR12: All the electrical interfaces between the UUB and the Radio module shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2.

IR13: All the electrical interfaces between the UUB and GPS antenna and the tank control (from TPCB) shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2.

IR14: All additional the electrical interfaces between the UUB and external world are described in the following *2.3.1.a* table:

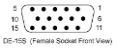
(see next page)

Conn. ID	*Name*	*Signal Name*	*Pin[2] #*	*Direction*	*Signal description*	*Connector type*
J11	PMT A1	Anode PMT1	n/a	IN	50Ω, -2V Fs	SMA, socket 
J12	PMT A2	Anode PMT2	n/a	IN	50Ω, -2V Fs	
J13	PMT A3	Anode PMT3	n/a	IN	50Ω, -2V Fs	
J14	PMT 4	PMT4	n/a	IN	50Ω, -2V Fs	
J15	DET IN1	Input 1	n/a	IN	50Ω, -2V Fs	
J16	DET IN2	Input 2	n/a	IN	50Ω, -2V Fs	
J17	DET IN3	Input 3	n/a	IN	50Ω, -2V Fs	
J21	PMT 1 Monit.	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	
J22	PMT 2 Monit.	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	
J23	PMT 3 Monit.	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	

[2] From the UUB point of view only

Conn. ID	*Name*	*Signal Name*	*Pin[2] #*	*Direction*	*Signal description*	*Connector type*
J24	PMT 4 Monit[3].	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	
J25	PMT I Monit.	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	
J26	PMT II Monit.	HV command	2	OUT	DC, 0 to 2.5V	DB15HD socket 
		HV monitor	1	IN	DC, 0 to 5V	
		Cur. monitor	3	IN	DC, 0 to 5V	
		Temp. Mon +	4	OUT	DC, +12V	
		Temp Mon -	9	IN	DC, 0 to 5V	
		NC	11	n/a	Not currently used	
		NC	13	n/a	Not currently used	
		+12V	5	OUT	DC, +12V	
		GND	6	n/a	Ground	
		GND	7	n/a	Ground	
		GND	8	n/a	Ground	
		GND	10	n/a	Ground	
		GND	12	n/a	Ground	
		GND	14	n/a	Ground	
		GND	15	n/a	Ground	

[3] Small PMT.

J31	Slow Control	+12V HI-1	5	OUT	DC +12V through 1KΩ	DB15HD socket 
		+12V HI-2	4	OUT	DC +12V through 1KΩ	
		+12V HI-3	2	OUT	DC +12V through 1KΩ	
		+12V LI	1	OUT	DC +12V through 22KΩ	
		EXT TEMP	7	IN	0 to +5 V	
		BAT CENT	3	IN	0 to +5 V	
		LOADCURR	8	IN	0 to +5 V	
		BAT1 TEMP	9	IN	0 to +5 V	
		BAT2 TEMP	10	IN	0 to +5 V	
		WAT LVL	11	IN	0 to +5 V	
		BAT+ OUT	12	IN	0 to +5 V	
		SP VOLT	13	IN	0 to +5 V	
		SP CURR	14	IN	0 to +5 V	
		Not Used	15	n/a	Not Used	
		GND	6	n/a	GND	
J41	GPS Board	RxD1	1	IN	Receive Data (3V logic)	10 pin (2x5) socket 
		TxD1	2	OUT	Transmit Commands (3V logic)	
		+3V PWR	3	OUT	Regulated 3Vdc supply	
		1PPS	4	IN	1 pulse-per-second input	
		Ground	5	n/a	Signal and Power common	
		Battery	6	OUT	Optional External Backup	
		Reserved	7	n/a	Not currently used	
		RTCM In	8	OUT	RTCM correction output	
		Antenna Bias	9	OUT	3V-5V antenna bias output	
		Reserved	10	n/a	Not currently used	
J51	Main Power	24VDC	1	IN	DC, +20 to +30V	Binder 99-3431-202-04 
		GND	2	n/a	n/a	
J61	LED FLASH 1	Uout 1	n/a	OUT	+0 to +20V	SMA, socket 
J62	LED FLASH 2	Uout 2	n/a	OUT	+0 to +20V	
J71	External Trigger	EXT TRIG	n/a	IN	TTL	
J72	Internal Trigger	INT TRIG	n/a	OUT	TTL	
J81	USB SYS	VCC	1	OUT	+5V	USB Type B, Socket 
		D-	2	IN/OUT	Data -	
		D+	3	IN/OUT	Data +	
		GND	4	n/a	GND	
J82	USB Slow Ctrl	VCC	1	OUT	+5V	
		D-	2	IN/OUT	Data -	
		D+	3	IN/OUT	Data +	
		GND	4	n/a	GND	
J83	USB OTG	VCC	1	OUT	+5V (100mA maxi)	USB Type A, Socket 
		D-	2	IN/OUT	Data -	
		D+	3	IN/OUT	Data +	
		GND	4	n/a	GND	
J84	Ethernet	T+	1	OUT	Transmit +	RJ45, Socket 
		T-	2	OUT	Transmit -	
		R+	3	IN	Receive +	
		NC	4	n/a	Reserved	
		NC	5	n/a	Reserved	
		R-	6	IN	Receive -	
		NC	7	n/a	Reserved	
		NC	8	n/a	Reserved	

J85	TELECOM	SU PWR	1	OUT	SU Power, DC +12V (14V, max)	SUBD9, socket 
		SU RXD	2	IN	SU RXD	
		SU TXD	3	OUT	SU TXD	
		1PPS	4	OUT	One pulse per second,+3.3V	
		GND	5	n/a	Ground	
		TELRESCPU	6	IN	SU Reset out, see SU spec., RD2	
		RTS	7	OUT	SU RTS	
		CTS	8	IN	SU CTS	
		CPURESTEL	9	OUT	SU Reset in, see SU spec., RD2	
J91	EXT 1	D1+	1	IN or OUT	Configurable	HE26 HARWIN M808542642 2x13 pin 
		D1-	2	IN or OUT	Configurable	
		VCC[4]	3	OUT	+24V, unregulated, switchable	
		GND	4	n/a	Ground	
		D0+	5	IN or OUT	Configurable	
		D0-	6	IN or OUT	Configurable	
		D2+	7	IN or OUT	Configurable	
		D2-	8	IN or OUT	Configurable	
		VCC[4]	9	OUT	+24V, unregulated, switchable	
		GND	10	n/a	Ground	
		D4+	11	IN or OUT	Configurable	
		D4-	12	IN or OUT	Configurable	
		D3+	13	IN or OUT	Configurable	
		D3-	14	IN or OUT	Configurable	
		VCC[4]	15	OUT	+24V, unregulated, switchable	
		GND	16	n/a	Ground	
		D5+	17	IN or OUT	Configurable	
		D5-	18	IN or OUT	Configurable	
		D6+	19	IN or OUT	Configurable	
		D6-	20	IN or OUT	Configurable	
		VCC[4]	21	OUT	+24V, unregulated, switchable	
		GND	22	n/a	Ground	
		D7+	23	IN or OUT	Configurable	
		D7-	24	IN or OUT	Configurable	
		VCC[4]	25	OUT	+24V, unregulated, switchable	
		GND	26	n/a	Ground	

[4] 100 mA maximum per connector

Conn. ID	*Name*	*Signal Name*	*Pin[5] #*	*Direction*	*Signal description*	*Connector type*
J92	EXT 2	D1+	1	IN or OUT	Configurable	HE26 HARWIN M808542642 2x13 pin 
		D1-	2	IN or OUT	Configurable	
		VCC[6]	3	OUT	+24V, unregulated, switchable	
		GND	4	n/a	Ground	
		D0+	5	IN or OUT	Configurable	
		D0-	6	IN or OUT	Configurable	
		D2+	7	IN or OUT	Configurable	
		D2-	8	IN or OUT	Configurable	
		VCC[6]	9	OUT	+24V, unregulated, switchable	
		GND	10	n/a	Ground	
		D4+	11	IN or OUT	Configurable	
		D4-	12	IN or OUT	Configurable	
		D3+	13	IN or OUT	Configurable	
		D3-	14	IN or OUT	Configurable	
		VCC[6]	15	OUT	+24V, unregulated, switchable	
		GND	16	n/a	Ground	
		D5+	17	IN or OUT	Configurable	
		D5-	18	IN or OUT	Configurable	
		D6+	19	IN or OUT	Configurable	
		D6-	20	IN or OUT	Configurable	
		VCC[6]	21	OUT	+24V, unregulated, switchable	
		GND	22	n/a	Ground	
		D7+	23	IN or OUT	Configurable	
		D7-	24	IN or OUT	Configurable	
		VCC[6]	25	OUT	+24V, unregulated, switchable	
		GND	26	n/a	Ground	
J93	JTAG System	GND	1	n/a	Ground	HE14 2x7 pin 
		+3.3V Bias	2	OUT	DC, +3.3 Volts	
		GND	3	n/a	Ground	
		JTAG TMS	4	IN	0 to +3.3V	
		GND	5	n/a	Ground	
		JTAG TCK	6	IN	0 to +3.3V	
		GND	7	n/a	Ground	
		JTAG TDO	8	OUT	0 to +3.3V	
		GND	9	n/a	Ground	
		JTAG TDI	10	IN	0 to +3.3V	
		GND	11	n/a	Ground	
		Not Used	12	n/a	Not currently used	
		GND	13	n/a	Ground	
		Not Used	14	n/a	Not currently used	
J94	JTAG Slow Ctrl	JTAG TDO	1	OUT	0 to +3.3V	HE14 2x7 pin 
		VCC OUT	2	OUT	DC, +3.3 Volts	
		JTAG TDI	3	IN	0 to +3.3V	
		VCC IN	4	IN	DC, +3.3 Volts	
		JTAG TMS	5	IN	0 to +3.3V	
		Not Used	6	n/a	Not currently used	
		JTAG TCK	7	IN	0 to +3.3V	
		Not Used	8	n/a	Not currently used	
		GND	9	n/a	Ground	
		Not Used	10	n/a	Not currently used	
		JTAG RST	11	IN	0 to +3.3V	
		Not Used	12	n/a	Not currently used	
		Not Used	13	n/a	Not currently used	
		Not Used	14	n/a	Not currently used	

[5] From the UUB point of view only
[6] 100 mA maximum per connector

Table 2.3.1a – Electrical Interfaces Signal breakout

IR15: The UUB shall provide external LVDS connection (EXT 1 and EXT 2) for other detector systems, including synchronization signal. The front panel connectors pin out for those extension connections, are described in the table 2.3.1.b below.

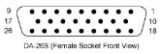
UUB Conn. ID	***Name***	***Signal Name***	***UUB connector HE26, 2x13 Socket***  ***Pin#***	***Front Panel connector SUBDHD26 Socket***  ***Pin#***	***Signal description***
J91 J92	EXT 1 EXT 2	D1+	1	10	Configurable
		D1-	2	11	Configurable
		VCC	3	3	+24V, unregulated, switchable
		GND	4	4	Gnd
		D0+	5	1	Configurable
		D0-	6	2	Configurable
		D2+	7	18	Configurable
		D2-	8	19	Configurable
		VCC	9	12	+24V, unregulated, switchable
		GND	10	13	Gnd
		D4+	11	14	Configurable
		D4-	12	15	Configurable
		D3+	13	5	Configurable
		D3-	14	6	Configurable
		VCC	15	20	+24V, unregulated, switchable
		GND	16	21	Gnd
		D5+	17	22	Configurable
		D5-	18	23	Configurable
		D6+	19	8	Configurable
		D6-	20	9	Configurable
		VCC	21	7	+24V, unregulated, switchable
		GND	22	16	Gnd
		D7+	23	17	Configurable
		D7-	24	26	Configurable
		VCC	25	24	+24V, unregulated, switchable
		GND	26	25	Gnd

Table 2.3.1b – Front panel Extension connectors pin out

2.3.2. Mechanical Interfaces

IR21: The UUB mechanical interfaces shall be identical to the mechanical interfaces of the existing UB (RD5).

IR22: The UUB mechanical front panel shall have the same external dimensions of the existing UB front panel.

IR23: All UUB new electrical connection toward the inner tank shall use the existing feed through (RD7, hatch cover design document).

2.4. Physical requirements (PR)

(Representing the physical characteristics of the UUB).

PR1: The cabled PCB of the UUB shall be within the following dimensions:

- width = 240 mm.
- length = 340 mm.
- height = 32 mm.

As defined for the existing UB in the RD1 document, paragraph 2.2.4.6.

PR2: The complete mass of the UUB shall not exceed 10 Kg.

PR3: The UUB PCB shall have at least six layers minimum, with one layer for ground plane and one layer for power supplies. Class VI, minimum isolation distances 0.12mm.

2.5. Environmental requirements (ER)

(Representing the conditions under which the UUB has to perform its functions).

ER1: The UUB shall be able to resist in operation to a temperature range from -20 to +70 degrees Celsius and in storage from -40 to +80 degrees Celsius. Other parts of the SDEU (located in the tank) shall be able to resist to a lower temperature range, -50 degrees Celsius.

ER2: The UUB shall be able to resist in operation to an average hygrometry between 30 and 80%.

ER3: The UUB system shall include all necessary electrical protection for internal (over current) and external surges.

ER4: The UUB shall be able to resist in operation to storm lightning occurring at a distance of 1 km.

ER5: The UUB shall not exhibit any malfunction, degradation of performance or deviation from specified indications when test spikes are applied to the dc power input leads or electromagnetically coupled into the equipment wiring.

The values of E (amplitude) and t (duration) of each spike are given below:
- Spike #1 E = ± Twice the nominal line voltage, t = 10 microseconds ± 20 %
- Spike #2 E = ± Twice the nominal line voltage, t = 0.15 microseconds ± 20 %

ER6: The UUB shall resist, out of operation, to long distance cargo flight and dirty road transportation, with an adapted packaging.

2.6. Quality requirements (QR)

(Representing how well the UUB perform its functions).

QR1: The UUB system shall be included in the overall Pierre Auger Observatory Quality Assurance Plan, (RD3).

QR2: The UUB system shall follow policies and procedure described in the Pierre Auger Observatory Surface Detector Electronics Quality Management Plan, (RD4).

2.7. Operation requirements (OR)

(Representing how shall be the operability of the UUB).

OR1: The UUB system shall be entirely autonomously powered through the existing power system. In the scope of a further extension, the total consumption shall not exceed 10W, including existing BSRU (radio, 1.1W average, 3.6W peak) and PMT Bases (1.5W).

OR2: The UUB system shall be entirely controlled and monitored through the main radio communication system (BSRU).

OR3: The UUB system shall be able to detect major failure and send alarm and/or initiate a recovery process with an internal monitoring system.

OR4: The software used in the UUB system shall be written in a standard language and widely documented to allow modification by people not involved in the primary design phase.

OR5: The software used in the UUB system shall be easily downloadable through the main radio communication system and from maintenance device (computer) connected on site.

OR6: The UUB shall be able to be in operation 24 hours over 24 hours, during 15 years.

2.8. Support requirements (SR)

(Representing the support the UUB needs to performs its functions).

SR1: The UUB system shall be designed to limit onsite maintenance at the maximum.

SR2: Hardware and software tools and test benches shall be developed and provided to facilitate the onsite support of the UUB system.

SR3: Adequate quantity (15%) of spare of the major elements of the SDEU (UUB, light generators, GPS boards, small PMT & bases, sensors) shall be procured and stored to facilitate onsite maintenance, in addition of the attrition (2 to 3%) for the part procurement.

SR4: The UUB system design shall allow people not involved in the design performing general maintenance operations, after a short training.

SR5: All support operation on the UUB system shall be completely documented, traced and recorded.

2.9. Verification requirements (VR)

(Representing the methods used to verify the UUB requirements).

VR1: The UUB system requirements listed in the present document shall be verified following the verification matrix displayed below.

2.9.1. Verification Matrix

Four methods are used to verify the RDS requirements:

- **Inspection (I)**. The requirement implementations are verified by a visual inspection of the system and its sub systems.
- **Review of Design (R)**. The requirement implementations are verified by a review of the design documents (schematics, reports, pictures, etc.) of the system and its sub systems.
- **Analysis (A)**. The requirement implementations are verify through analysis reports, showing result on mathematical or software models of the sub system concerned.
- **Test (T)**. The requirement implementations are verified through test reports showing results on test procedures applied on the system and its sub systems.

The verifications can be performed at two levels, **System** (S) or **Sub System** (SS) or **Both** (B)

Verification Matrix			
Requirements		Verification	
ID	Text	Method	Level
FR11	The UUB shall processes analog anode signals from the three PMTs. A low and high gain signal for each PMT shall be conditioned and digitized.	T	B
FR12	The total RMS integrated noise at the ADC input shall not exceed 0.5 LSB.	R	SS
FR13	The UUB shall digitize the PMTs anode signals at a sampling frequency of 120 Msp/s with a resolution of 12 bits minimum with the adapted conditioning and gain circuitry.	R	B
FR14	Adapted anti-aliasing filters shall be implemented for each PMT signal inputs (60Mhz at -3dB) (<5% single time bin aliasing noise)	T	B
FR15	The UUB shall process analog signals from 2 additional PMTs from ASCII detector in 3 analog channels, one low gain for one of the 2 PMTs (or summation) and 2 high gains.	R	SS
FR16	The high gain/low gain ratio shall be of 32.	T	SS
FR17	The UUB shall processes analog anode signals from the fourth small additional PMT (RD6, the purpose is to increase the overall energy dynamic range).	R	SS
FR21	The trigger/memory circuitry shall evaluate the high-gain output of each PMT every 8.3 ns for interesting trigger patterns (see FR26), store the data in buffer and inform the micro-processor circuitry.	R	S
FR22	The trigger/memory circuitry shall generate a first level trigger based upon hardware analysis of the high gain PMT channel waveforms. The UUB micro-processor software shall imposes additional constraints to generate a level 2 trigger signal.	T	B
FR23	The goal of the first level trigger shall be to trigger efficiently on UHE cosmic ray air showers of energy >1019eV, while simultaneously rejecting lower energy showers and minimizing composition dependent trigger biases, within a rate constraint of 100 Hz.	T	B
FR24	The level 1 trigger shall be designed to be flexible and eventually modifiable in the future	R	SS
FR25	The level 1 trigger shall start waveforms recording during 19.2 µs	R	SS
FR26	The triggers to be implemented are: etc..	R-T	B
FR27	The level 1 trigger shall provide signal to Time-Tagging circuitry allowing time step of trigger and determination of absolute time of each ADC bin.	T	S
FR31	The UUB shall able to time tag each events, using the information given by a commercial GPS unit and a logic circuitry (in FPGA) based on the existing design, described in the RD1 document, point 2.2.3.4	T	B
FR32	The time tagging unit shall have a resolution of 4 ns or better, stable in temperature better than 5%.	T	SS
FR41	The UUB shall have a micro-processor able to perform the following tasks: - Level 2 Trigger - Data acquisition and event building with double buffering and recording - Calibration process including analog inputs base line monitoring - Data compression to fit the communication flux limit - Communication with the slow control management unit.	R	S
FR51	The UUB shall have a slow control unit, allowing measurement and monitoring of at least 64 x 0 to 5 Volts	R	SS

Verification Matrix			
Requirements		Verification	
ID	Text	Method	Level
	analog input signals coded over 12 bits (can be multiplexed) and 8 logic inputs. Number of channel shall accommodate the designs for additional ASCII detector.		
FR52	The UUB shall have a slow control unit able to generate at least 8 x 0 to 2.5 Volts analog buffered output signals coded from 12 bits and 8 logic buffered outputs.	**R**	**SS**
FR53	The UUB shall have a slow control unit able to monitor internal parameters to perform a failure detection, isolation and recovery (FDIR) process on onboard power supplies and batteries voltage protection over 35 V and under 22 V)	**T**	**S**
FR54	The UUB slow control unit shall be able to manage all existing SDE environmental sensors (RD1) and additionally, a water temperature sensor and an atmospheric pressure sensor.	**T**	**SS**
FR61	The UUB shall have a light generator unit (LED controller) able to generate two adapted signals with at least an amplitude of 20 Volts towards the two foreseen light devices (LED driver). The signal shall be controlled in time with a resolution of 4 ns and shall be synchronized to the time tagging signal (1PPS)	**T**	**S**
FR62	The light devices (LED driver) shall have at least the same specifications of the existing device	**R**	**SS**
FR63	The light generator unit (LED controller) and light devices (LED driver) shall measure the linearity of the SD photomultipliers (PMTs) over the full dynamic range of their acquisition channels, using the "two LEDs technique"	**T**	**S**
FR64	The light generator unit (LED controller) and light devices (LED driver) shall measure the amplification ratio between overlapping acquisition channels, low and high gain of the SD PMT and the ASCII detector.	**T**	**S**
FR65	The light generator unit (LED controller) and light devices (LED driver) shall be able to create artificial EAS events of different topology on the ground SD array in order to: - check the ACQ response for different event pattern, - check the event reconstruction	**T**	**S**
FR71	The UUB shall include communication capabilities adapted to the existing unit (see Interfaces Requirements section) based on serial links	**R**	**S**
FR72	The UUB shall include Ethernet communication capability.	**R**	**S**
FR73	The UUB shall include USB and USB OTG communication capability**.**	**R**	**S**
FR74	The UUB shall include digital communication capability for other detector systems, including synchronization signal.	**T**	**S**
FR81	The UUB shall be able to produce all needed internal power supplies, regulated and stabilized, filtered and protected, from a single input of 24 Volts nominal but varying from 18 to 30 Volts.	**T**	**B**
FR82	The UUB internal power supplies shall be voltage monitored by the slow control unit (FR53).	**R**	**S**
CR01	Each part of the UUB shall be contained in a single printed circuit board, excepted for the commercial GPS board, light generators (LED controller shall be on UUB PCB) and the mechanical housing.	**I**	**S**
CR02	The SDEU shall be composed at the minimum of the following components:	**R**	**S**
CR11	The PMTs signal conditioning unit shall be composed of analog discrete components to perform the low noise amplification and filtering functionalities from the actively split PMT anode signals.	**I**	**B**
CR21	The Digitizer unit shall be composed of a number of commercial ADC equivalents to the number of analog inputs or split inputs (dual ADC chips with LVDS outputs are recommended).	**R**	**S**
CR31	The Digital Trigger unit shall be implemented in the unique FPGA component, following the architecture described in *figure 2.2.4*.a below:	**R**	**B**
CR32	External input and output Trigger signal shall be implemented (see Interfaces Requirements).	**I**	**S**
CR33	Memory minimum size requirements shall follow the values described in the table *2.2.4.b* below:	**R**	**S**
CR41	The Processing unit shall be composed of a hardcore processor in the unique FPGA component, with adapted circuitry and memories	**R**	**S**
CR42	The Processing unit shall have an adapted random access memory size of 512 Mo at the minimum	**R**	**S**
CR43	The Processing unit shall have an adapted flash memory	**R**	**S**
CR44	The Processing unit shall works under a micro-Linux operating system	**R**	**S**
CR45	The Processing unit shall have the adapted interfaces to be able to communicate with the other UUB units and the external world.	**R**	**S**
CR51	The Slow Control unit shall be composed of separate (from the main processor) micro controller, ADCs, DACs and associated circuitry on the UUB board	**R**	**B**
CR52	The Slow Control unit shall have analog inputs with 10 Kilo-Ohms impedance	**T**	**SS**
CR53	The Slow Control unit shall include the water temperature and atmospheric pressure sensors and all existing sensors (RD1).	**R**	**S**
CR54	The Slow Control unit shall have a direct USB communication link (see Interface Requirements)	**R**	**S**
CR61	The Calibration unit shall include a light generator unit (LED controller) implemented on the UUB PCB, able to provide 20 Volts amplitude pulses. Controlled directly by the processing unit (FPGA).	**T**	**S**
CR62	The Calibration unit shall include an external dual light device adapted for SD PMT calibration purpose and ASCII detector (LED driver).	**R**	**S**
CR71	The Time Tagging unit shall be composed of a commercial, timing dedicated, GPS board and a time tagging algorithm implemented in the unique FPGA.	**R**	**S**
CR81	The UUB shall be able to manage at least 1 serial connection RS-232 type to communicate with the BSRU (radio).	**R**	**S**
CR82	The UUB shall be able to manage one Ethernet connection.	**R**	**S**
CR83	The UUB shall be able to manage 2 USB (2.0) and one USB-OTG connection.	**R**	**S**

Verification Matrix			
Requirements		Verification	
ID	Text	Method	Level
CR84	The UUB shall be able to manage 2 digital connections for other detector systems, including synchronization signal, slow control and 24V power supply (CR93)	R	S
CR91	The power supplies unit shall be composed of adapted to design DC to DC converters with the following requirements: - Efficiency better than 80% (90% recommended) - Large input range, from 18 to 30 Volts (24V nominal) - Low ripple noise, less than 20mV	R - T	S
CR92	The 12V power supplies for PMTs bases and BSRU (radio) shall be separated (to avoid eventual failure propagation).	R	S
CR93	24 Volts, filtered, non-regulated and controlled shall be provided on the extensions connectors	T	S
CR101	The mechanical housing shall be composed of an aluminum extruded RF proof box, identical to the existing design (the existing box can be reused) and a metallic front panel, adapted to the new connectors type and their disposition.	I	S
IR11	All the electrical interfaces between the UUB and the PMTs shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2 (excepted for the dynode connectors).	R	S
IR12	All the electrical interfaces between the UUB and the Radio module shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2.	T	S
IR13	All the electrical interfaces between the UUB and GPS antenna and the tank control (from TPCB) shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2.	T	S
IR14	All additional the electrical interfaces between the UUB and external world are described in the following *2.3.1.a* table:	R	S
IR15	The UUB shall provide external LVDS connection (EXT 1 and EXT 2) for other detector systems, including synchronization signal. The front panel connectors pin out for those extension connections, are described in the table 2.3.1.b below.	R - T	S
IR21	The UUB mechanical interfaces shall be identical to the mechanical interfaces of the existing UB (RD5).	R	S
IR22	The UUB mechanical front panel shall have the same external dimensions of the existing UB front panel.	R	S
IR23	All UUB new electrical connection toward the inner tank shall use the existing feed through (RD7, hatch cover design document).	R	S
PR1	The cabled PCB of the UUB shall be within the following dimensions:	I	S
PR2	The complete mass of the UUB shall not exceed 10 Kg.	I	S
PR3	The UUB PCB shall have at least six layers minimum, with one layer for ground plane and one layer for power supplies. Class VI, minimum isolation distances 0.12mm	I	S
ER1	The UUB shall be able to resist in operation to a temperature range from -20 to +70 degrees Celsius and in storage from -40 to +80 degrees Celsius. Other parts of the SDEU (located in the tank) shall be able to resist to a lower temperature range, -50 degrees Celsius	T	B
ER2	The UUB shall be able to resist in operation to an average hygrometry between 30 and 80%	T	S
ER3	The UUB system shall include all necessary electrical protection for internal (over current) and external surges.	T	S
ER4	The UUB shall be able to resist in operation to storm lightning occurring at a distance of 1 km.	T	S
ER5	The UUB shall not exhibit any malfunction, degradation of performance or deviation from specified indications when test spikes are applied to the dc power input leads or electromagnetically coupled into the equipment wiring.	T	S
ER6	The UUB shall resist, out of operation, to long distance cargo flight and dirty road transportation, with an adapted packaging.	T	S
QR1	The UUB system shall be included in the overall Pierre Auger Observatory Quality Assurance Plan, (RD3).	R	B
QR2	The UUB system shall follow policies and procedure described in the Pierre Auger Observatory Surface Detector Electronics Quality Management Plan, (RD4)	R	B
OR1	The UUB system shall be entirely autonomously powered through the existing power system. In the scope of a further extension, the total consumption shall not exceed 10W, including existing BSRU (radio, 1.1W average, 3.6W peak) and PMT Bases (1.5W)	T	B
OR2	The UUB system shall be entirely controlled and monitored through the main radio communication system (BSRU).	T	S
OR3	The UUB system shall be able to detect major failure and send alarm and/or initiate a recovery process with an internal monitoring system	T	S
OR4	The software used in the UUB system shall be written in a standard language and widely documented to allow modification by people not involved in the primary design phase	R	B
OR5	The software used in the UUB system shall be easily downloadable through the main radio communication system and from maintenance device (computer) connected on site	T	B
OR6	The UUB shall be able to be in operation 24 hours over 24 hours, during 15 years.	A	B

Verification Matrix			
Requirements		Verification	
ID	Text	Method	Level
SR1	The UUB system shall be designed to limit onsite maintenance at the maximum	**R**	**B**
SR2	Hardware and software tools and test benches shall be developed and provided to facilitate the onsite support of the UUB system	**R**	**B**
SR3	Adequate quantity (15%) of spare of the major elements of the SDEU (UUB, light generators, GPS boards, small PMT & bases, sensors) shall be procured and stored to facilitate onsite maintenance, in addition of the attrition (2 to 3%) for the part procurement	**I**	**B**
SR4	The UUB system design shall allow people not involved in the design performing general maintenance operations, after a short training	**I**	**B**
SR5	All support operation on the UUB system shall be completely documented, traced and recorded	**I**	**B**

Table 2.9.1a – Verification Matrix

VR2: The test plan for the integrated SDEU shall be performed according to the RD3 document.

End of the document