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# Surface Detector Electronics Upgrade

## Critical Design Review

**Orsay, 04 February 2015**

**Tiina Suomijärvi, Patrick Stassi, Jim Beatty, SDEU design group**



V4

# Outline

- Introduction & physics requirements
- Development plan & organization
- Technical specification
- Design implementation
  - Upgraded Unified Board – WP5
  - Analog PMT signal processing – WP1
  - Time Tagging - WP3
  - Slow Control - WP4
  - Calibration Tools – WP7
- Interfaces
- Risks, FMECA, FDIR
- AIT-AIV Plan
- Small PMT design
- Cost and Schedule

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# Introduction & Physics requirements

# Pierre Auger Observatory

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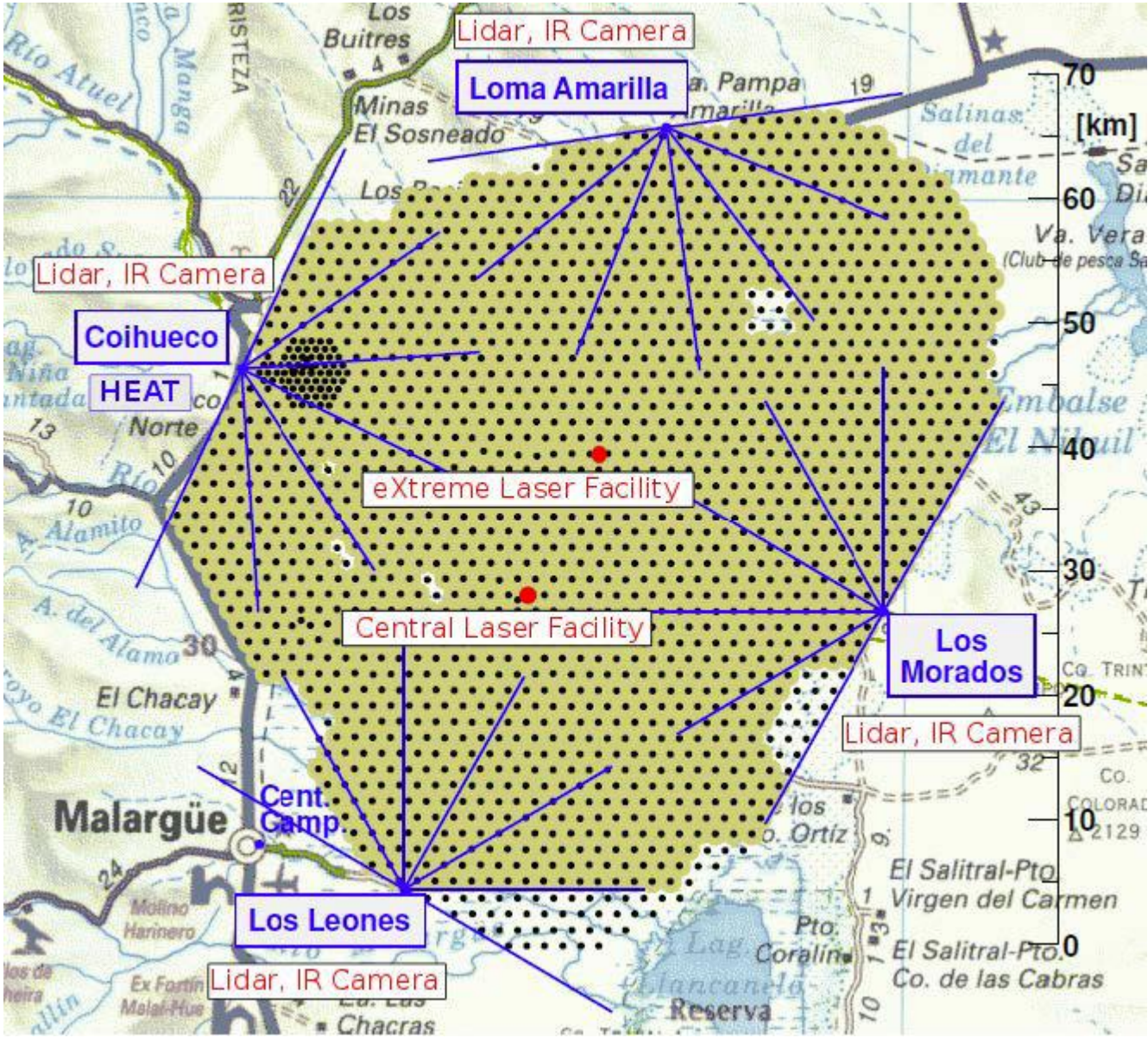
**Surface Array**

*1600 detector stations*
*1.5 Km spacing*
*3000 Km$^2$*
*INFILL array:*
*60 detector stations*
*750 m spacing*

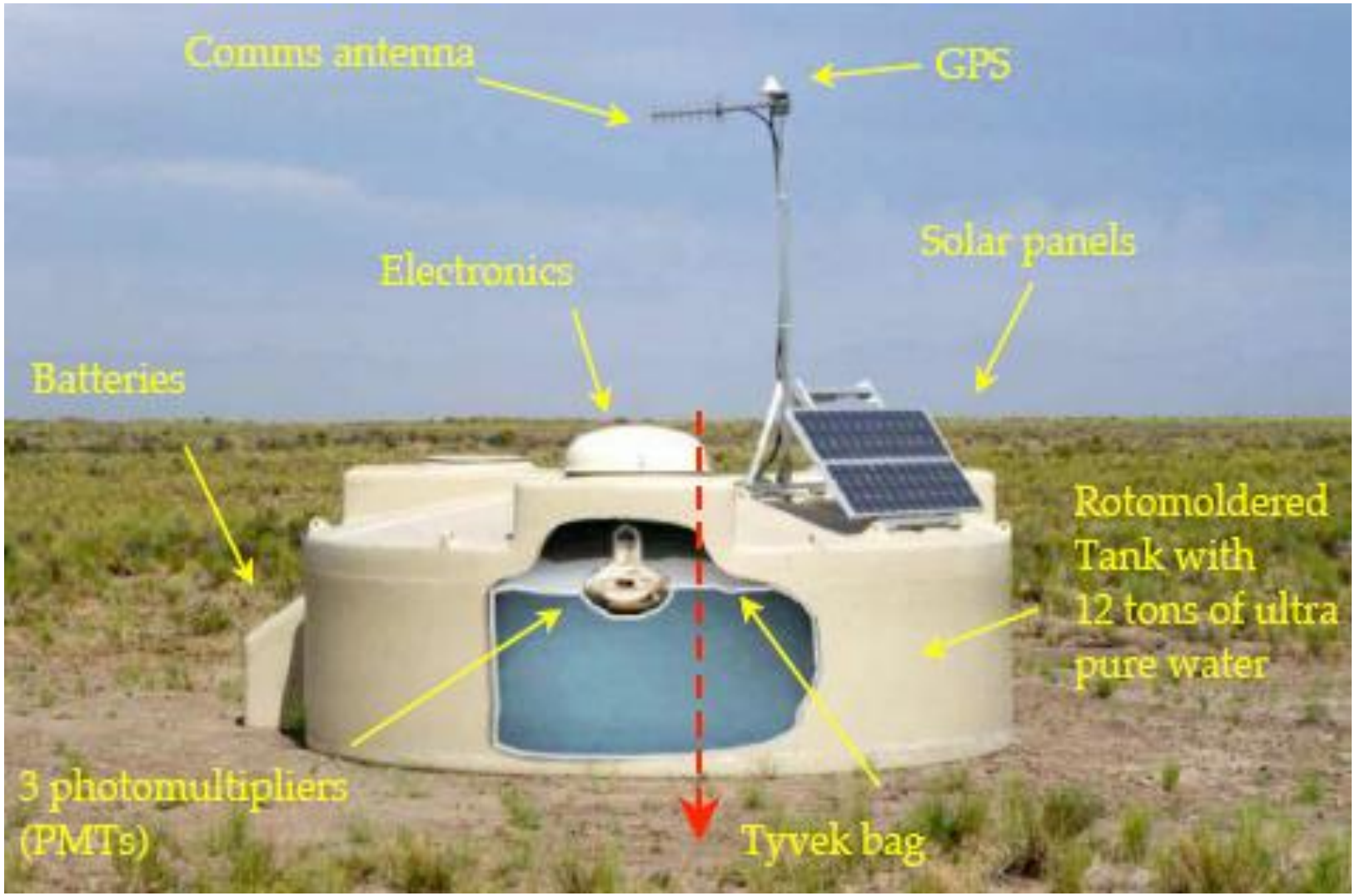
**Fluorescence Detectors**

*4 Telescope enclosures*
*6 Telescopes per enclosure*
*24 Telescopes total*
*HEAT: 3 Telescopes*

The full efficiency of the SD trigger is reached at 3 $10^{18}$ eV. For the Infill array the full efficiency is reached at 3 $10^{17}$ eV.



# Surface Detector




Power budget is 10 W per station.
The 900MHz COMMS transmission is 150 bytes/s/station.

# Current electronics (SDE)

## Ekit

Signals are read out by three 9" XP1805 photomultipliers.

Signals from anode and dynode outputs are filtered with an anti-aliasing filter and sampled with **40 MHz, 10 bit** FADC.

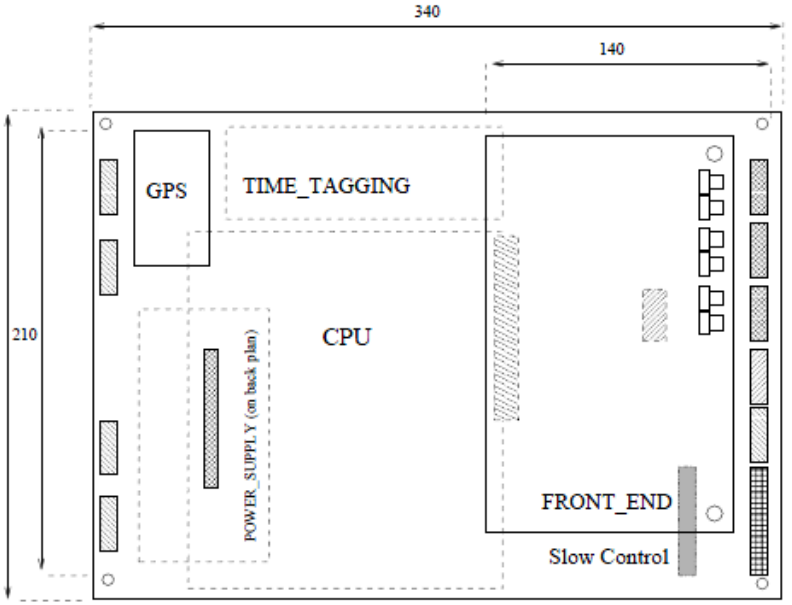
Total dynamic range: from few to about $6 \times 10^4$ photoelectrons (about **600 VEM**)

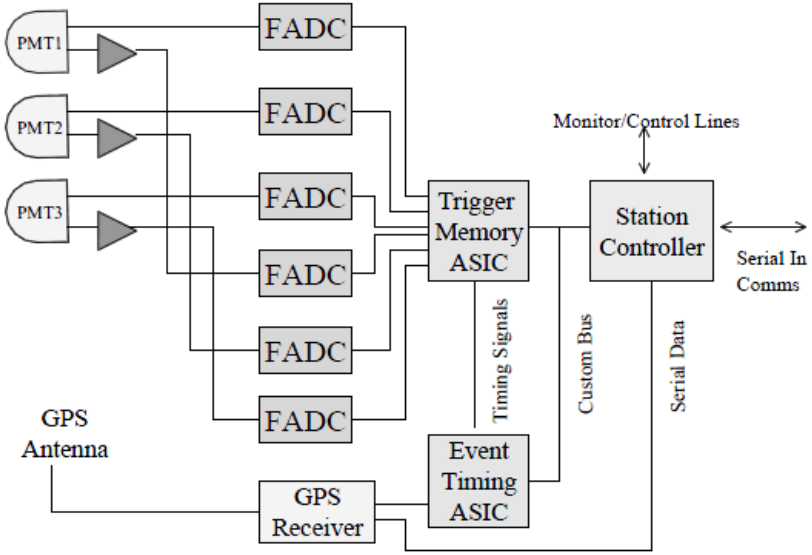
Two shower triggers are used: Threshold and time over threshold trigger

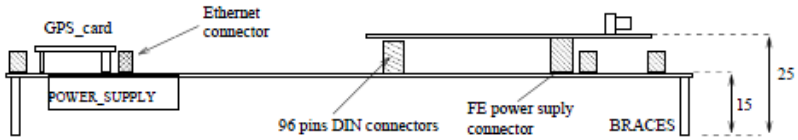
A common time base is established by using the GPS system (Motorola OnCore UT receiver) providing a one pulse/s which is used to synchronize a 100 MHz clock serving to timetag trigger.


Each detector station has an IBM 403 PowerPC processor for local data acquisition, software trigger and detector monitoring, and memory for data storage.

# Current electronics (SDE)

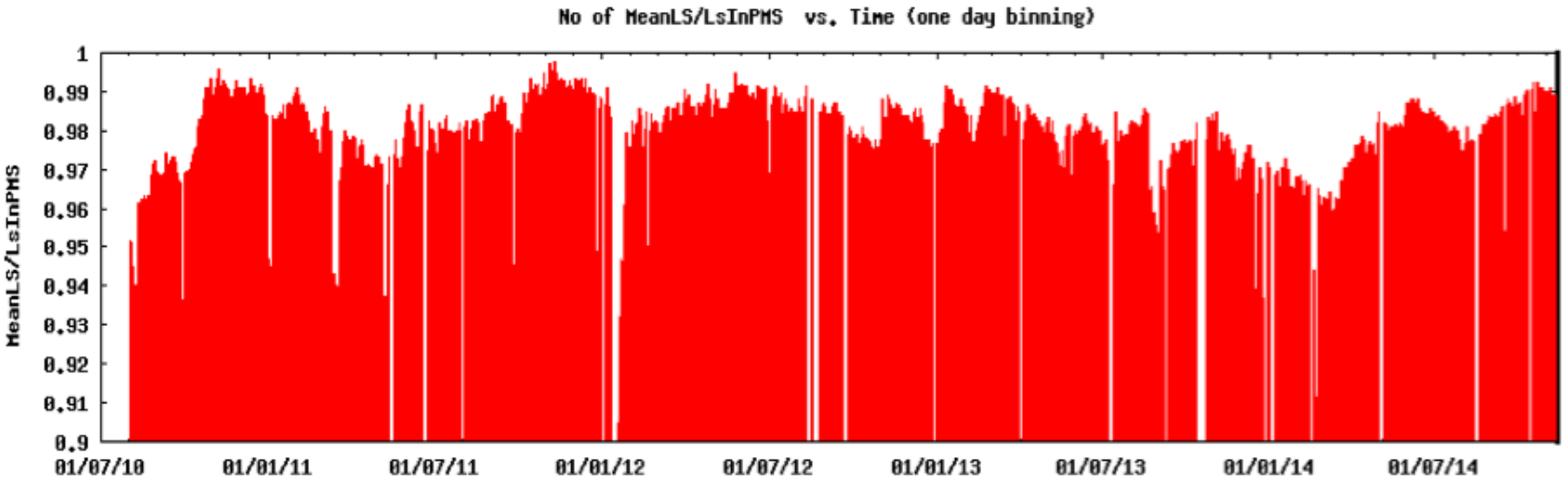


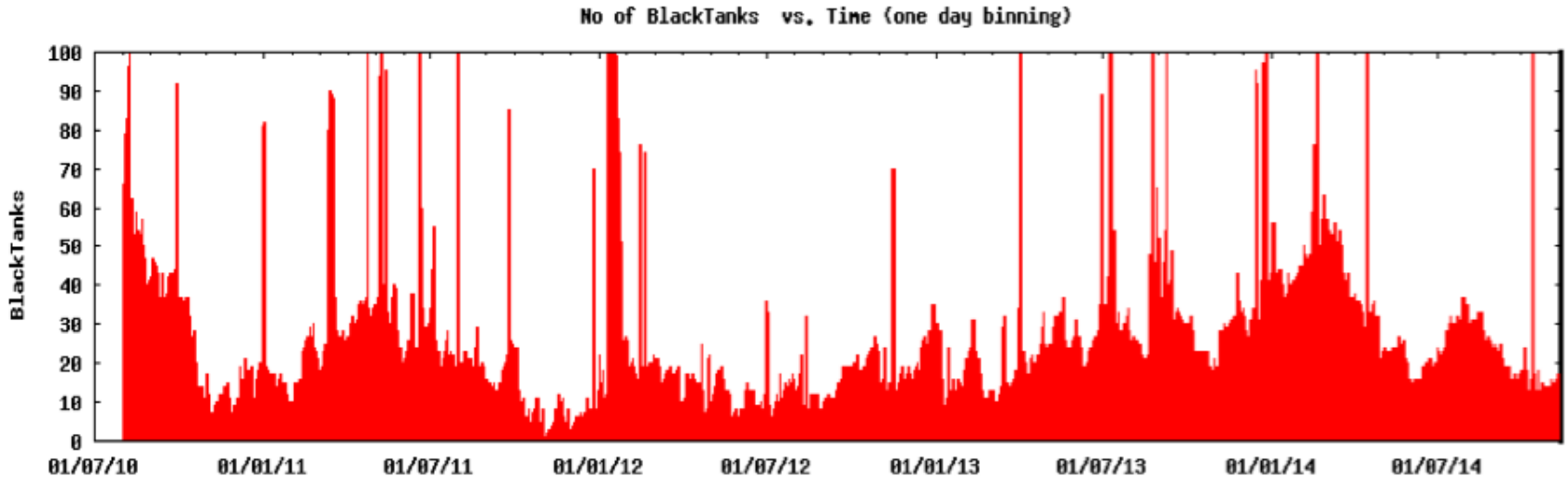




Calibration with background muons.
LED system (not used for calibration).

# Performance




Trigger efficiency is typically better than 98%.



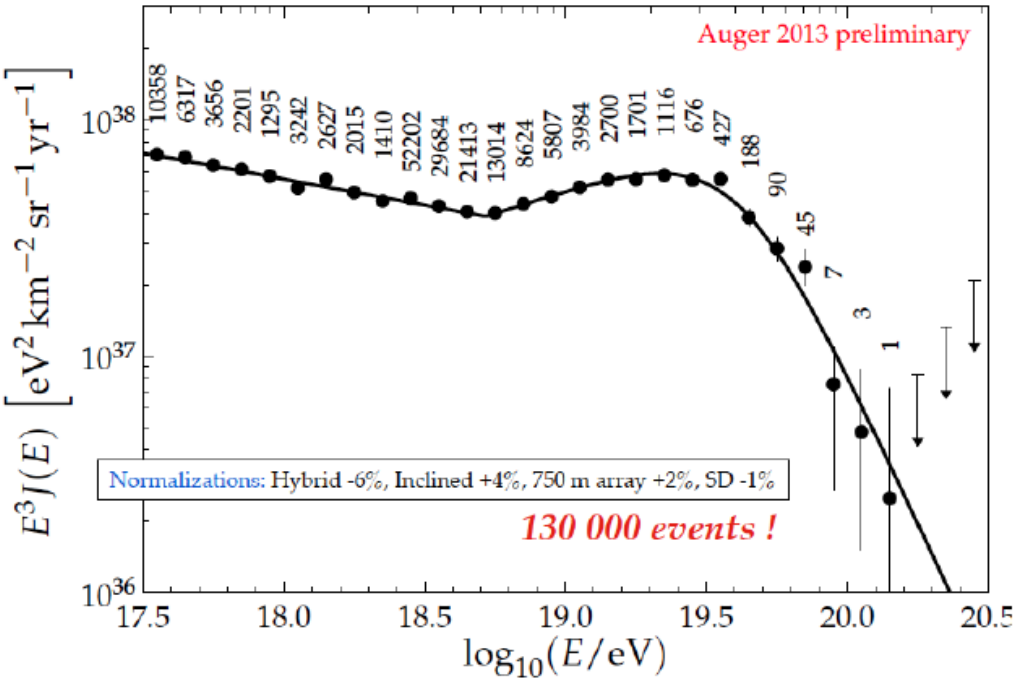

Number of black tanks typically lower than 20.

# Maintenance

- Failure rates are low, about 15 boards per year.
- About 3 maintenance trips per week (includes also batteries).
- All repair can be done in SDECo, Malargüe
- Test benches were moved to Malargüe.
- Local SDE staff: 3 technicians.



# Auger Upgrade




Auger has observed clearly both a strong cosmic-ray flux suppression above 50 EeV and a sharp spectral transition near 7 EeV (the ankle).

Presently it is not possible to determine whether the suppression is due to energy losses in transit (the GZK effect) or if it reveals the maximum energy of the source accelerators.

Goal:

Extend the existing measurements of composition-sensitive observables to higher energy to search for the rigidity-dependent suppression of the flux of individual mass groups.

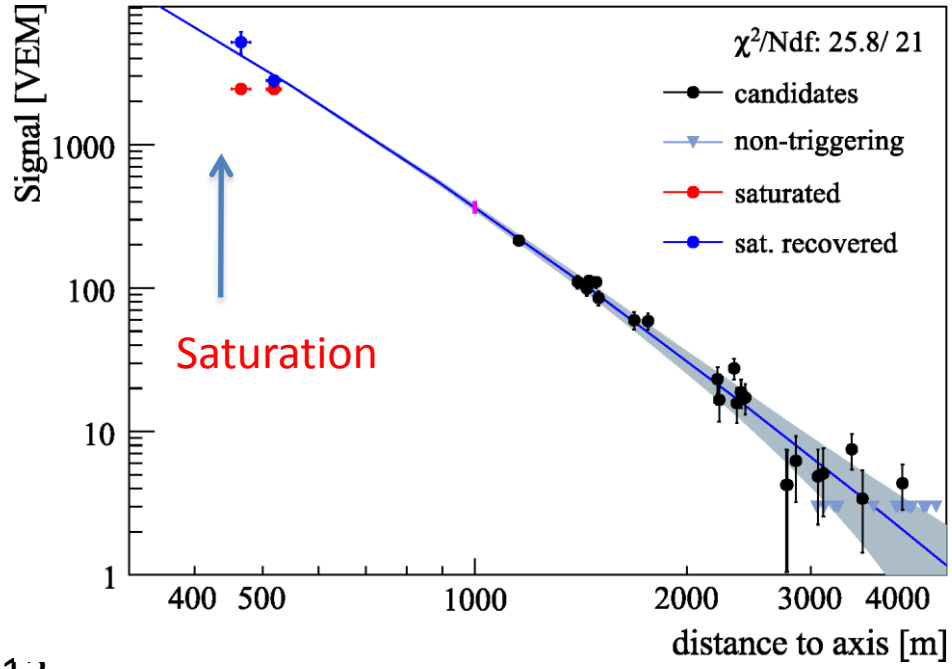
# Steps in SDE proposal construction

- Auger Beyond 2015 group suggests upgrade of SD/SDE
- Meeting in Orsay 8-9 October 2012
- Meeting in Orsay 21-22 January 2013
- Meeting in Lisbon 30-31 May 2013
- Meeting in Orsay 24-25 October 2013
- Meeting in Grenoble 30 January 2014
- Visio-meetings 7 May and 12 June 2014
- Meeting in Grenoble 15 October 2014
- Parallel sessions in Auger Collaboration meetings

- Documents circulated to the collaboration
- Mailing list: auger_sd_electronics
- Wiki page: https://www.auger.unam.mx/AugerWiki/SDE_Upgrade

# Requirements for new electronics

- Increased local processing and triggering capability by integrated, more powerful FPGA and microprocessor
  - ➔ Allows additional triggers and increases the processing power by > factor 10.
- Increased sampling rate from 40 MHz to 120 MHz:
  - ➔ Better resolving power for in-tank signal asymmetries




- Enhanced dynamic range (x32)
  - ➔ Allows to measure accurately showers up to about 250m from the shower core
  - ➔ Improve the geometric and energy reconstruction

# Requirements for new electronics

Increase the resolution of the station-to-station timing synchronization (from 10ns to 4ns).

Enhance calibration capabilities with a more flexible LED driver supporting additional calibration and test modes.

Enhance capabilities of the on board slow control system with additional sensors and functionalities

On prototypes:
Provides a flexible interface to allow the muon detectors upgrades prototypes and other enhancements co-located with the surface detector stations to make use of the data processing and communications infrastructure of the stations.

On final design:
Provide interface to the chosen muon detector solution.

# Status of Auger Upgrade

- The collaboration decided to upgrade the SD with Scintillator detector on top of the tank in November 2014.

Prototype scintillator detector ASCII.

- Muon component will be separated from the EM component by using additional information from scintillator installed on top of the water tank.
- Surface Detector electronics will be upgraded.
- Fluorescence Detector uptime will be increased from 14% to about 30%.
- Preliminary Design Report and final proposal in preparation (due to mid-April 2015).
- Engineering Array of 10 stations end 2015.
- Production and deployment 2016-17.

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# Development Plan & organization

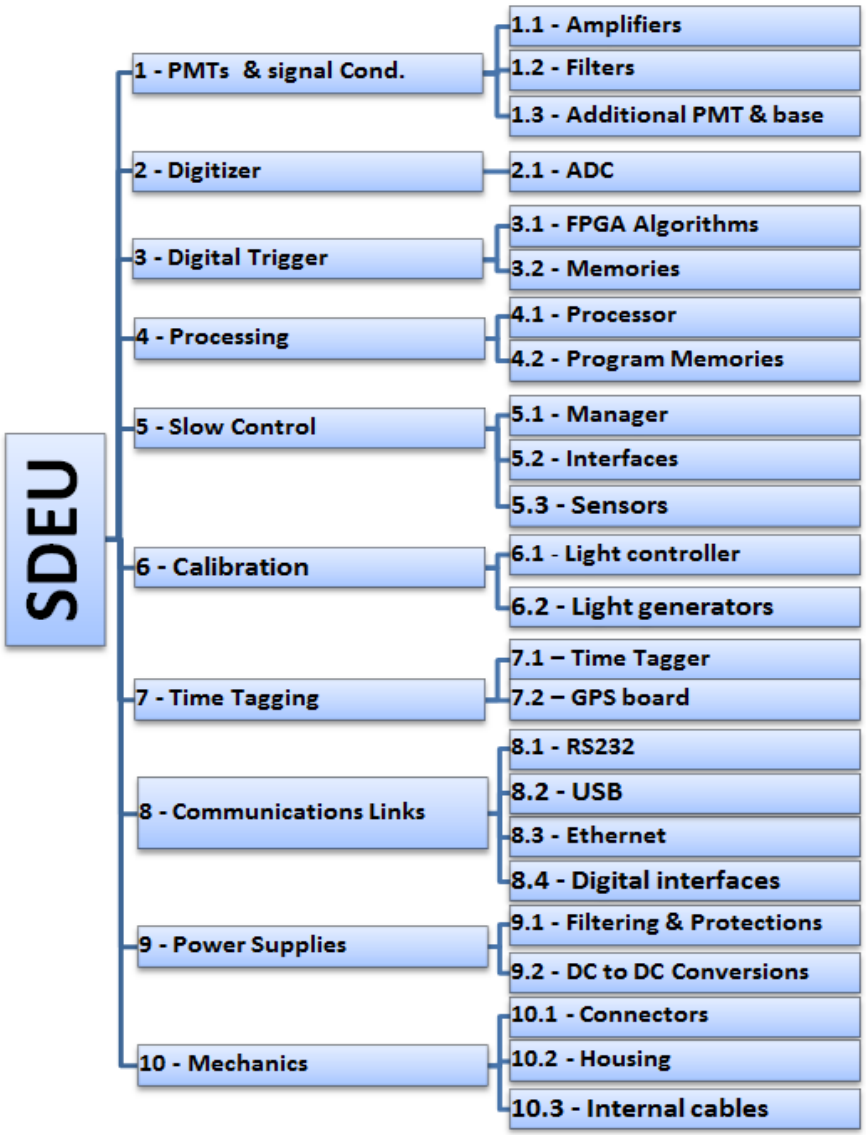
**WP10LPSC02J_SDEU_Dev_Plan_27nov14**

# SDE Task

- Task leaders: Tiina Suomijarvi and Jim Beatty
- System Engineer: Patrick Stassi
- Sub-tasks for maintenance
  - PMT-Base unit
  - Front End board
  - Trigger/memory circuitry
  - Time tagging and GPS
  - Unified Board
  - Tank Power Control Board
  - LED flasher

Maintenance activities continue in parallel with the upgrade activities.
Work Packages have been created for the upgrade activities.

# Development Plan - PBS




**1-The PMTs signal Conditioning**
- Amplifiers, filters, signal conditioning

**2-The PMTs signal Digitizing**
- ADCs

**3-The Storage and Trigger construction**
- Trigger algorithm in FPGA (firmware)

**4-Event Building and Processing**
- CPU, memories, OS and software

**5-The Slow Control management**
- Environmental sensors reading, PMTs high voltages control and voltage and current monitoring,
  solar power system monitoring. Dedicated software

**6-Calibration management**
- light generators and light generators management

**7-The Time Tagging**
- Commercial GPS and time tagger in FPGA (firmware)

**8-Communication links management**
- Serial, Ethernet, USB, external detectors digital interface

**9-Power supplies management**
- DC converters, filters and protections

**10-Mechanics**
- Housing, front panel, cables and connectors

# Work Packages definition

The Work Packages (WP) for the SDE Upgrade are:

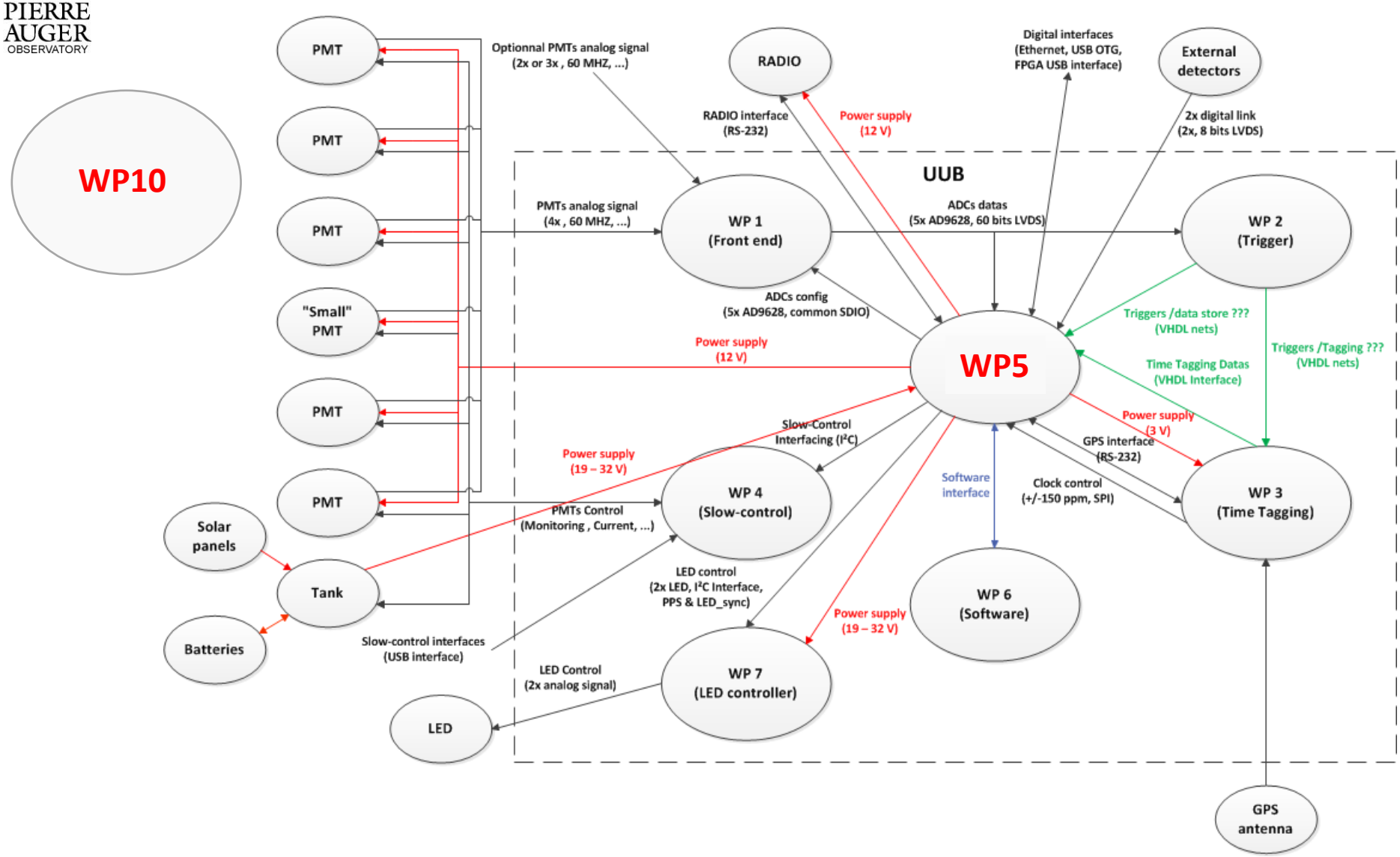
**WP1 Analog PMTs signal processing**
**WP2 Trigger development**
**WP3 Time Tagging development**
**WP4 Slow Control development**
**WP5 UUB Hardware Design & Integration**
**WP6 UUB Software development**
**WP7 Calibration & Control tools development**
**WP8 Assembly, Deployment and Validation**
**WP9 Simulation and Science Validation**
**WP10 Project Management**

# Work Packages responsibilities

| | WP1 | WP2 | WP3 | WP4 | WP5 | WP6 | WP7 | WP8 | WP9 | WP10 |
|---|---|---|---|---|---|---|---|---|---|---|
| BUW, Wuppertal - Germany | | | | Resp. | Part. | Part. | | | | |
| CNEA, Bariloche - Argentina | | | | | Part. | Part. | | Part. | | |
| ITEDA, Buenos Aires - Argentina | | | | | Part. | | | Part. | | |
| CWRU, Clevland - USA | | | Resp. | | Part. | Part. | | | | |
| FNAL, Chicago - USA | | | | | Part. | | | Part. | Part. | Part. |
| INFN, Lecce - Italy | Resp. | | | | Part. | Part. | | | | |
| INFN, Torino - Italy | Part. | | | | Part. | Part. | Resp. | | | |
| IPNO, Orsay - France | Part. | | | | Part. | | | Part. | | Resp. |
| KIT, Karlsruhe - Germany | | | | | Part. | | Part. | | Resp. | |
| LOD, Lodz - Poland | Part. | Part. | | | Part. | | | | | |
| LPNHE, Paris - France | Part. | | | | Part. | | Part. | | Part. | |
| LPSC, Grenoble - France | | | | Part. | Resp. | Part. | | Part. | | Part. |
| MTU, Houghton - USA | | Resp. | Part. | | Part. | Part. | Part. | | Part. | |
| OSU, Columbus - USA | Part. | Part. | | | Part. | Resp. | | Part. | | Part. |
| PAO, Malargue - Argentina | | | | | Part. | | | Resp. | Part. | |
| RU, Radboud University | Part. | | | | Part. | | | Part. | | |
| SU, Siegen University | | | | | Part. | | | Part. | | |

- Several laboratories from several countries participate to different WPs.
- All participate to WP5 (the integrated electronics board).
- Engineers for development have been identified.
- Most of the tools and facilities already available.

# Work Packages relations



# Project Documentation

| Designation | Reference | Revision |
|---|---|---|
| **Section 01: Development Plan** | | |
| SDEU Development Plan | WP10LPSC02 | J |
| | | |
| **Section 02: H/W Specifications** | | |
| SDEU Specifications | WP10LPSC03 | H |
| | | |
| **Section 03: S/W Specifications** | | |
| SDEU OBSW Specification | WP6LPSC13 | A |
| | | |
| **Section 04: Project Risks Analysis** | | |
| SDEU project Risks Analysis | WP10LPSC06 | C |
| | | |
| **Section 05: FMECA - FDIR** | | |
| SDEU FMECA-FDIR | WP10LPSC10 | C |
| | | |
| **Section 06: Tests Plan** | | |
| SDEU AIT-AIV Plan | WP10LPSC11 | D |
| | | |
| **Section 07: ICD** | | |
| SDEU Electrical Interfaces Control Document | WP10LPSC05 | E |
| SDEU Detectors Interfaces Control Document | WP10LPSC07 | F |
| **Section 08: WBS Cost estimate** | | |
| SDEU WBS | WP10LPSC08 | J |
| | | |
| **Section 09: Schedule** | | |
| SDEU Project General Schedule | WP10LPSC04 | K |
| | | |

Meeting minutes are on the SDE Upgrade wiki page.
Technical documents will be in the CERN EDMS.

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# Technical specifications

**WP10LPSC03H_SDEU_Specification_27Nov14**

# Requirements Classification

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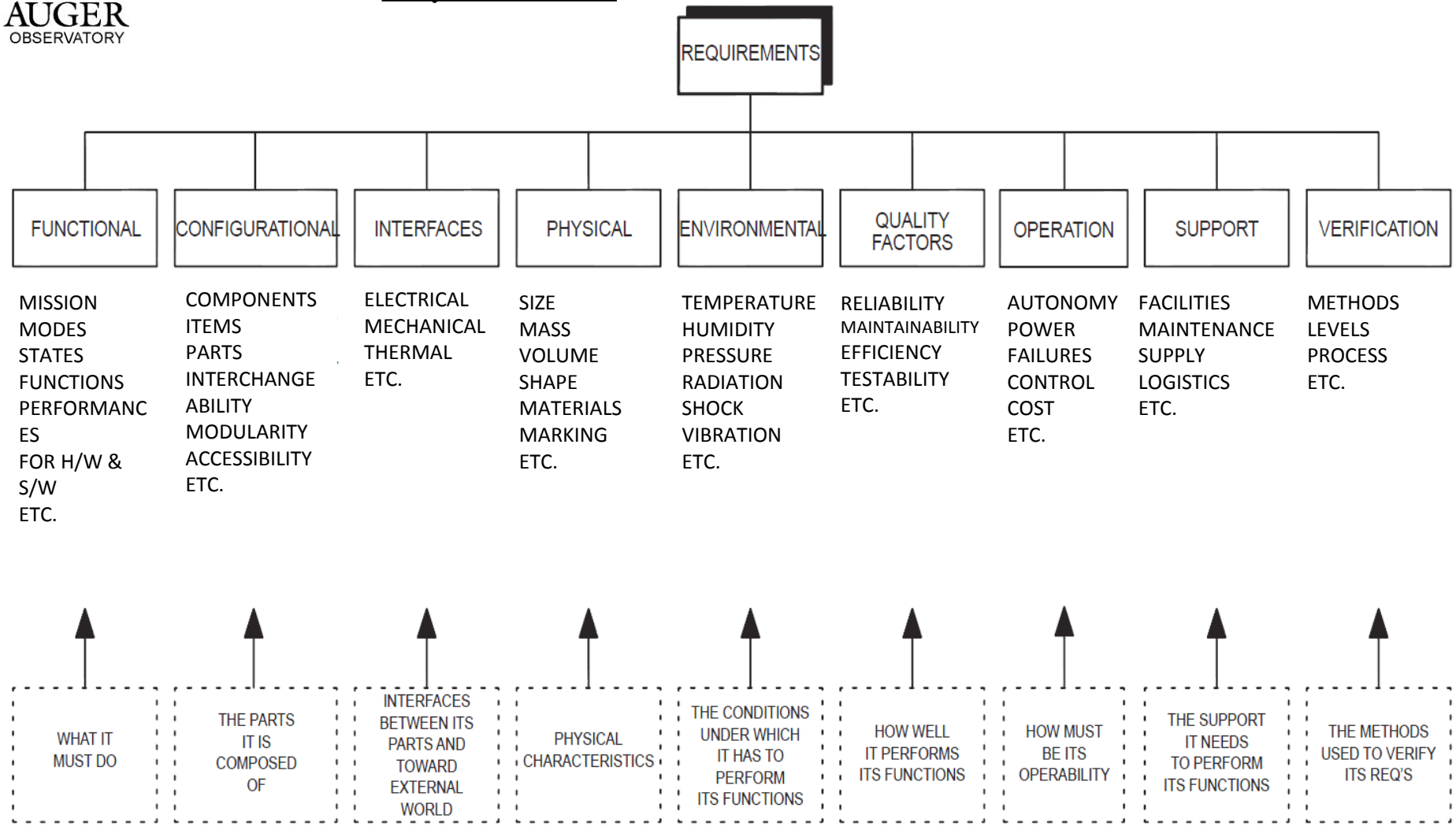
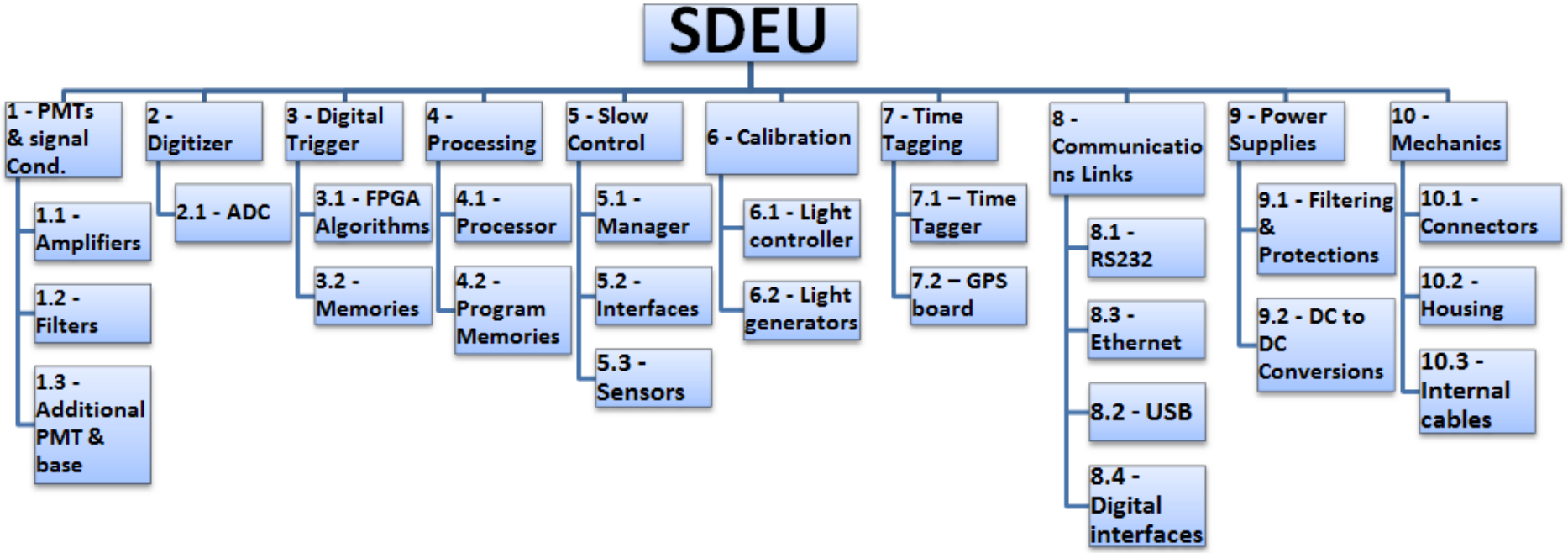
## 9 class of requirements:



# Product Breakdown Structure (PBS)

The requirements are defined in each class, accordingly to this PBS:

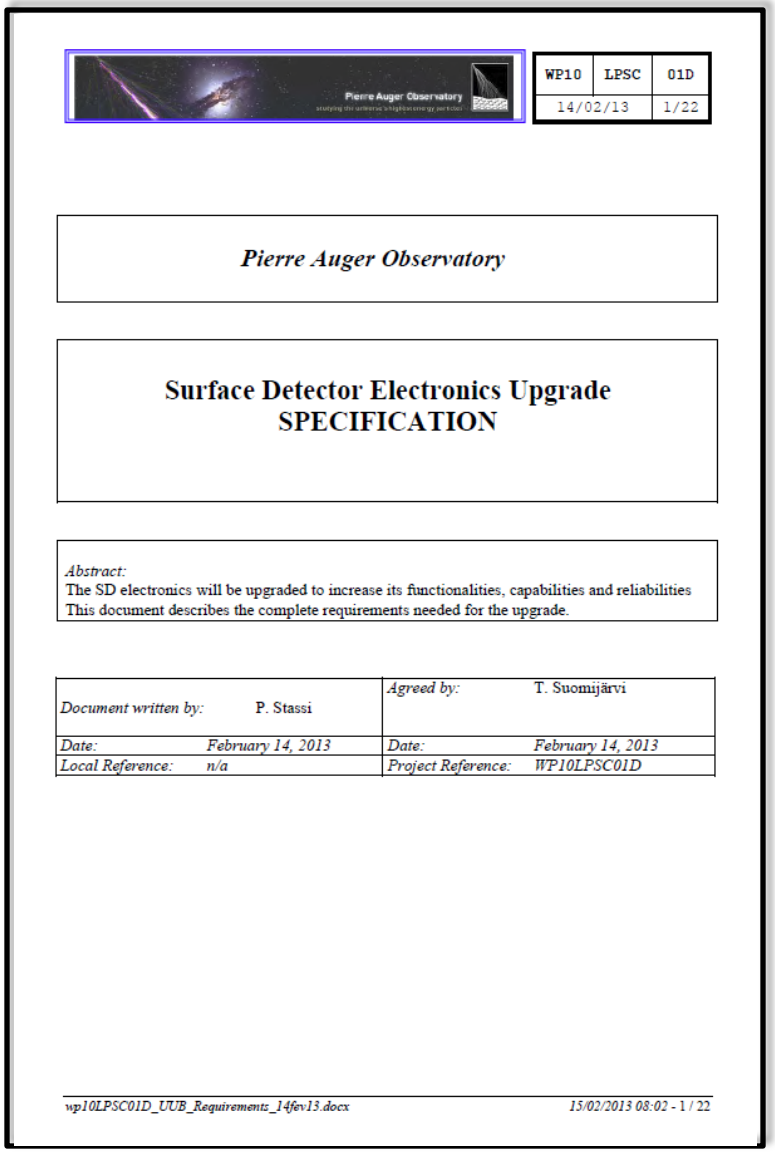


# Document Status

Version 03H – Nov. 27, 2014

- All Requirements class filled
- 87 Requirements defined
- 38 "old" Req.
- 49 "upgrade" Req.

Physics, user and technical req.



WP10 | LPSC | 01D
14/02/13 | 1/22

*Pierre Auger Observatory*

**Surface Detector Electronics Upgrade**
**SPECIFICATION**

*Abstract:*
The SD electronics will be upgraded to increase its functionalities, capabilities and reliabilities
This document describes the complete requirements needed for the upgrade.

| | | | |
|---|---|---|---|
| *Document written by:* | P. Stassi | *Agreed by:* | T. Suomijärvi |
| *Date:* | *February 14, 2013* | *Date:* | *February 14, 2013* |
| *Local Reference:* | *n/a* | *Project Reference:* | *WP10LPSC01D* |

*wp10LPSC01D_UUB_Requirements_14fev13.docx* *15/02/2013 08:02 - 1 / 22*

# Functional Requirements (FR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| FR11 | The UUB shall processes analog anode signals from the three PMTs. A low and high gain signal for each PMT shall be conditioned and digitized. |
| FR12 | The total RMS integrated noise at the ADC input shall not exceed 0.5 LSB. |
| FR13 | The UUB shall digitize the PMTs anode signals at a sampling frequency of 120 Msp/s with a resolution of 12 bits minimum with the adapted conditioning and gain circuitry. |
| FR14 | Adapted anti-aliasing filters shall be implemented for each PMT signal inputs (60Mhz at -3dB) (<5% single time bin aliasing noise) |
| FR15 | The UUB shall process analog signals from 2 additional PMTs from ASCII detector in 3 analog channels, one low gain for one of the 2 PMTs (or summation) and 2 high gains. |
| FR16 | The high gain/low gain ratio shall be of 32. |
| FR17 | The UUB shall processes analog anode signals from the fourth small additional PMT (RD6, the purpose is to increase the overall energy dynamic range). |
| FR21 | The trigger/memory circuitry shall evaluate the high-gain output of each PMT every 8.3 ns for interesting trigger patterns (see FR26), store the data in buffer and inform the micro-processor circuitry. |
| FR22 | The trigger/memory circuitry shall generate a first level trigger based upon hardware analysis of the high gain PMT channel waveforms. The UUB micro-processor software shall imposes additional constraints to generate a level 2 trigger signal. |
| FR23 | The goal of the first level trigger shall be to trigger efficiently on UHE cosmic ray air showers of energy >1019eV, while simultaneously rejecting lower energy showers and minimizing composition dependent trigger biases, within a rate constraint of 100 Hz. |
| FR24 | The level 1 trigger shall be designed to be flexible and eventually modifiable in the future |
| FR25 | The level 1 trigger shall start waveforms recording during 19.2 µs |
| FR26 | The triggers to be implemented are: etc.. |
| FR27 | The level 1 trigger shall provide signal to Time-Tagging circuitry allowing time step of trigger and determination of absolute time of each ADC bin. |
| FR31 | The UUB shall able to time tag each events, using the information given by a commercial GPS unit and a logic circuitry (in FPGA) based on the existing design, described in the RD1 document, point 2.2.3.4 |
| FR32 | The time tagging unit shall have a resolution of 4 ns or better, stable in temperature better than 5%. |
| FR41 | The UUB shall have a micro-processor able to perform the following tasks:<br>- Level 2 Trigger<br>- Data acquisition and event building with double buffering and recording<br>- Calibration process including analog inputs base line monitoring<br>- Data compression to fit the communication flux limit<br>- Communication with the slow control management unit. |
| FR51 | The UUB shall have a slow control unit, allowing measurement and monitoring of at least 64 x 0 to 5 Volts analog input signals coded over 12 bits (can be multiplexed) and 8 logic inputs. Number of channel shall accommodate the designs for additional ASCII detector. |

# Functional Requirements (FR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| FR52 | The UUB shall have a slow control unit able to generate at least 8 x 0 to 2.5 Volts analog buffered output signals coded from 12 bits and 8 logic buffered outputs. |
| FR53 | The UUB shall have a slow control unit able to monitor internal parameters to perform a failure detection, isolation and recovery (FDIR) process on onboard power supplies and batteries voltage protection over 35 V and under 22 V) |
| FR54 | The UUB slow control unit shall be able to manage all existing SDE environmental sensors (RD1) and additionally, a water temperature sensor and an atmospheric pressure sensor. |
| FR61 | The UUB shall have a light generator unit (LED controller) able to generate two adapted signals with at least an amplitude of 20 Volts towards the two foreseen light devices (LED driver). The signal shall be controlled in time with a resolution of 4 ns and shall be synchronized to the time tagging signal (1PPS) |
| FR62 | The light devices (LED driver) shall have at least the same specifications of the existing device |
| FR63 | The light generator unit (LED controller) and light devices (LED driver) shall measure the linearity of the SD photomultipliers (PMTs) over the full dynamic range of their acquisition channels, using the "two LEDs technique" |
| FR64 | The light generator unit (LED controller) and light devices (LED driver) shall measure the amplification ratio between overlapping acquisition channels, low and high gain of the SD PMT and the ASCII detector. |
| FR65 | The light generator unit (LED controller) and light devices (LED driver) shall be able to create artificial EAS events of different topology on the ground SD array in order to:<br>- check the ACQ response for different event pattern,<br>- check the event reconstruction |
| FR71 | The UUB shall include communication capabilities adapted to the existing unit (see Interfaces Requirements section) based on serial links |
| FR72 | The UUB shall include Ethernet communication capability. |
| FR73 | The UUB shall include USB and USB OTG communication capability. |
| FR74 | The UUB shall include digital communication capability for other detector systems, including synchronization signal. |
| FR81 | The UUB shall be able to produce all needed internal power supplies, regulated and stabilized, filtered and protected, from a single input of 24 Volts nominal but varying from 18 to 30 Volts. |
| FR82 | The UUB internal power supplies shall be voltage monitored by the slow control unit (FR53). |

# Configurational Requirements (CR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| CR01 | Each part of the UUB shall be contained in a single printed circuit board, excepted for the commercial GPS board, light generators (LED controller shall be on UUB PCB) and the mechanical housing. |
| CR02 | The SDEU shall be composed at the minimum of the following components: |
| CR11 | The PMTs signal conditioning unit shall be composed of analog discrete components to perform the low noise amplification and filtering functionalities from the actively split PMT anode signals. |
| CR21 | The Digitizer unit shall be composed of a number of commercial ADC equivalents to the number of analog inputs or split inputs (dual ADC chips with LVDS outputs are recommended). |
| CR31 | The Digital Trigger unit shall be implemented in the unique FPGA component, following the architecture described in *figure 2.2.4*.a below: |
| CR32 | External input and output Trigger signal shall be implemented (see Interfaces Requirements). |
| CR33 | Memory minimum size requirements shall follow the values described in the table *2.2.4.b* below: |
| CR41 | The Processing unit shall be composed of a hardcore processor in the unique FPGA component, with adapted circuitry and memories |
| CR42 | The Processing unit shall have an adapted random access memory size of 512 Mo at the minimum |
| CR43 | The Processing unit shall have an adapted flash memory |
| CR44 | The Processing unit shall works under a micro-Linux operating system |
| CR45 | The Processing unit shall have the adapted interfaces to be able to communicate with the other UUB units and the external world. |
| CR51 | The Slow Control unit shall be composed of separate (from the main processor) micro controller, ADCs, DACs and associated circuitry on the UUB board |
| CR52 | The Slow Control unit shall have analog inputs with 10 Kilo-Ohms impedance |
| CR53 | The Slow Control unit shall include the water temperature and atmospheric pressure sensors and all existing sensors (RD1). |
| CR54 | The Slow Control unit shall have a direct USB communication link (see Interface Requirements) |
| CR61 | The Calibration unit shall include a light generator unit (LED controller) implemented on the UUB PCB, able to provide 20 Volts amplitude pulses. Controlled directly by the processing unit (FPGA). |
| CR62 | The Calibration unit shall include an external dual light device adapted for SD PMT calibration purpose and ASCII detector (LED driver). |

# Configurational Requirements (CR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| CR71 | The Time Tagging unit shall be composed of a commercial, timing dedicated, GPS board and a time tagging algorithm implemented in the unique FPGA. |
| CR81 | The UUB shall be able to manage at least 1 serial connection RS-232 type to communicate with the BSRU (radio). |
| CR82 | The UUB shall be able to manage one Ethernet connection. |
| CR83 | The UUB shall be able to manage 2 USB (2.0) and one USB-OTG connection. |
| CR84 | The UUB shall be able to manage 2 digital connections for other detector systems, including synchronization signal, slow control and 24V power supply (CR93) |
| CR91 | The power supplies unit shall be composed of adapted to design DC to DC converters with the following requirements:<br>- Efficiency better than 80% (90% recommended)<br>- Large input range, from 18 to 30 Volts (24V nominal)<br>- Low ripple noise, less than 20mV |
| CR92 | The 12V power supplies for PMTs bases and BSRU (radio) shall be separated (to avoid eventual failure propagation). |
| CR93 | 24 Volts, filtered, non-regulated and controlled shall be provided on the extensions connectors |
| CR101 | The mechanical housing shall be composed of an aluminum extruded RF proof box, identical to the existing design (the existing box can be reused) and a metallic front panel, adapted to the new connectors type and their disposition. |

# Interface Requirements (IR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| IR11 | All the electrical interfaces between the UUB and the PMTs shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2 (excepted for the dynode connectors). |
| IR12 | All the electrical interfaces between the UUB and the Radio module shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2. |
| IR13 | All the electrical interfaces between the UUB and GPS antenna and the tank control (from TPCB) shall be identical to the electrical interfaces of the existing UB, as described in the RD1 document, chapter 2.2. |
| IR14 | All additional the electrical interfaces between the UUB and external world are described in the following *2.3.1.a* table: |
| IR15 | The UUB shall provide external LVDS connection (EXT 1 and EXT 2) for other detector systems, including synchronization signal. The front panel connectors pin out for those extension connections, are described in the table 2.3.1.b below. |
| IR21 | The UUB mechanical interfaces shall be identical to the mechanical interfaces of the existing UB (RD5). |
| IR22 | The UUB mechanical front panel shall have the same external dimensions of the existing UB front panel. |
| IR23 | All UUB new electrical connection toward the inner tank shall use the existing feed through (RD7, hatch cover design document). |

# Physical and Environmental Requirements (PR# ER#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| PR1 | The cabled PCB of the UUB shall be within the following dimensions: |
| PR2 | The complete mass of the UUB shall not exceed 10 Kg. |
| PR3 | The UUB PCB shall have at least six layers minimum, with one layer for ground plane and one layer for power supplies. Class VI, minimum isolation distances 0.12mm |
| | |
| ER1 | The UUB shall be able to resist in operation to a temperature range from -20 to +70 degrees Celsius and in storage from -40 to +80 degrees Celsius. Other parts of the SDEU (located in the tank) shall be able to resist to a lower temperature range, -50 degrees Celsius |
| ER2 | The UUB shall be able to resist in operation to an average hygrometry between 30 and 80% |
| ER3 | The UUB system shall include all necessary electrical protection for internal (over current) and external surges. |
| ER4 | The UUB shall be able to resist in operation to storm lightning occurring at a distance of 1 km. |
| ER5 | The UUB shall not exhibit any malfunction, degradation of performance or deviation from specified indications when test spikes are applied to the dc power input leads or electromagnetically coupled into the equipment wiring. |
| ER6 | The UUB shall resist, out of operation, to long distance cargo flight and dirty road transportation, with an adapted packaging. |

# Quality and Operation Requirements (QR# OR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| QR1 | The UUB system shall be included in the overall Pierre Auger Observatory Quality Assurance Plan, (RD3). |
| QR2 | The UUB system shall follow policies and procedure described in the Pierre Auger Observatory Surface Detector Electronics Quality Management Plan, (RD4) |
| | |
| OR1 | The UUB system shall be entirely autonomously powered through the existing power system. In the scope of a further extension, the total consumption shall not exceed 10W, including existing BSRU (radio, 1.1W average, 3.6W peak) and PMT Bases (1.5W) |
| OR2 | The UUB system shall be entirely controlled and monitored through the main radio communication system (BSRU). |
| OR3 | The UUB system shall be able to detect major failure and send alarm and/or initiate a recovery process with an internal monitoring system |
| OR4 | The software used in the UUB system shall be written in a standard language and widely documented to allow modification by people not involved in the primary design phase |
| OR5 | The software used in the UUB system shall be easily downloadable through the main radio communication system and from maintenance device (computer) connected on site |
| OR6 | The UUB shall be able to be in operation 24 hours over 24 hours, during 15 years. |

# Support Requirements (SR#)

| Requirements | |
|---|---|
| **ID** | **Text** |
| SR1 | The UUB system shall be designed to limit onsite maintenance at the maximum |
| SR2 | Hardware and software tools and test benches shall be developed and provided to facilitate the onsite support of the UUB system |
| SR3 | Adequate quantity (15%) of spare of the major elements of the SDEU (UUB, light generators, GPS boards, small PMT & bases, sensors) shall be procured and stored to facilitate onsite maintenance, in addition of the attrition (2 to 3%) for the part procurement |
| SR4 | The UUB system design shall allow people not involved in the design performing general maintenance operations, after a short training |
| SR5 | All support operation on the UUB system shall be completely documented, traced and recorded |

# Verification Requirements (VR#)

| |
|---|
| **VR1:** The UUB system requirements listed in the present document shall be verified following the verification matrix |

**The verification can be performed with four methods, at system or sub system level:**

- **Inspection**
  - *The requirement implementations are verified by a visual inspection of the system and its sub systems.*
- **Review of Design**
  - *The requirement implementations are verified by a review of the design documents (schematics, reports, pictures, etc.) of the system and its sub systems.*
- **Analysis (simulations)**
  - *The requirement implementations are verify through analysis reports, showing result on mathematical or software models of the sub system concerned.*
- **Test**
  - *The requirement implementations are verified through test reports showing results on test procedures applied on the system and its sub systems.*

| |
|---|
| **VR2:** The test plan for the integrated SDEU shall be performed according to the RD3 document. |

RD3 Pierre Auger Observatory Quality Assurance Plan, October 2000, V1

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# Design Implementation

- Upgraded Unified Board – WP5
- Analog PMT signal processing – WP1
- Time Tagging - WP3
- Slow Control - WP4
- Calibration Tools – WP7

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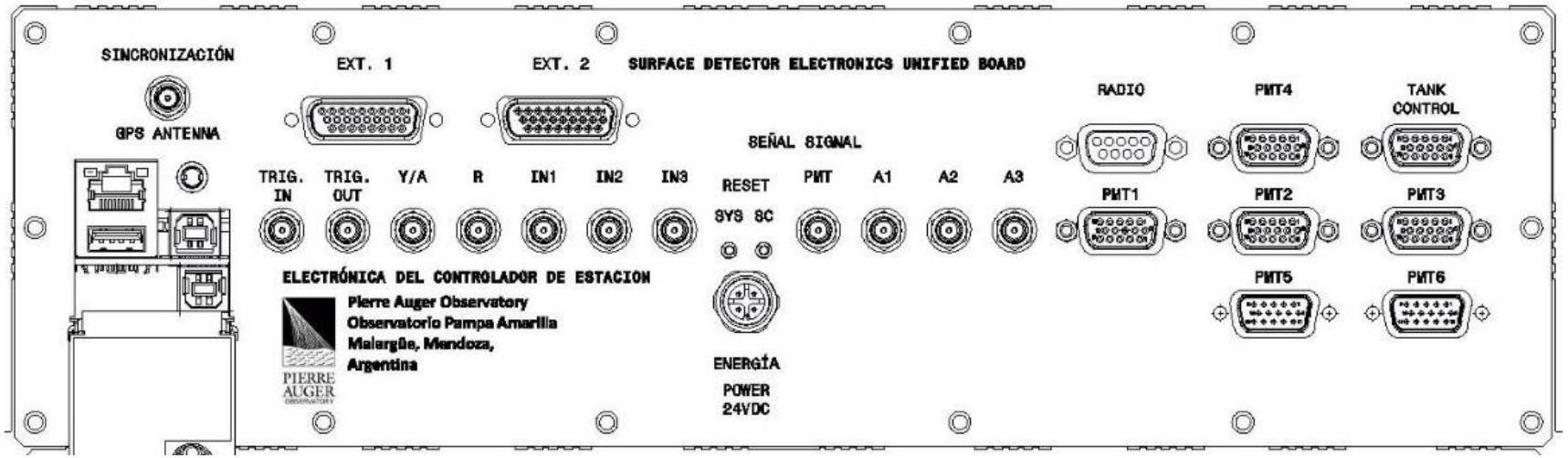
# Interfaces

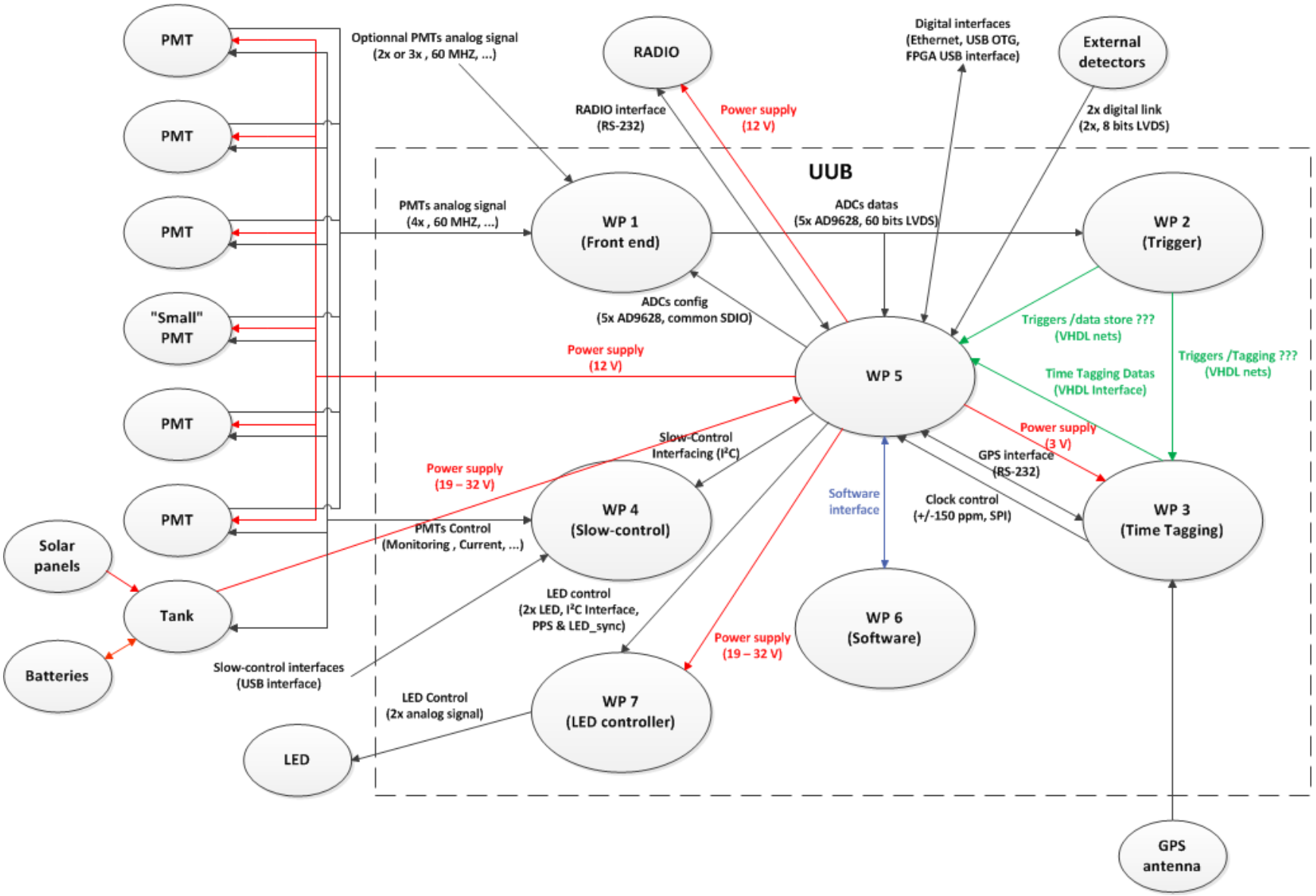
**WP10LPSC05E_SDEU_EICD_28Nov14**

**WP10LPSC07F_SDEU_DICD_29Jan14**

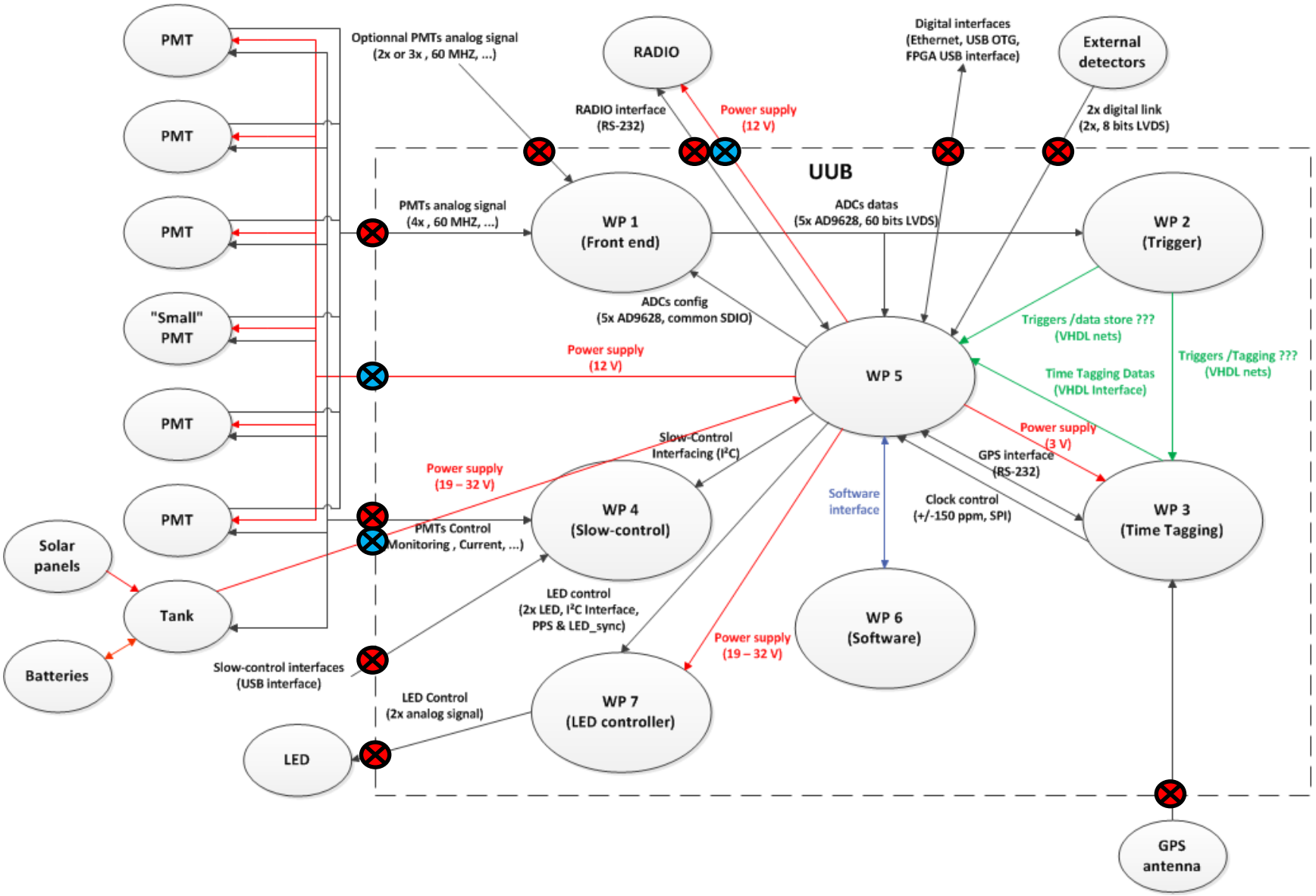
# UUB mechanical interface



# UUB electrical interface



# UUB electrical interface



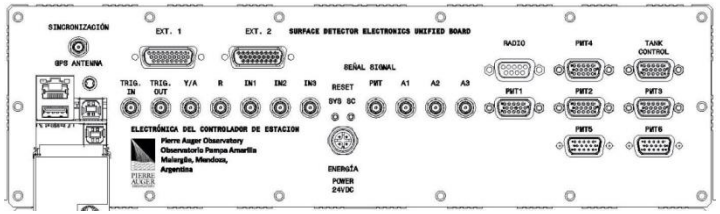
# Power consumption

| | Work Package | Power (W) |
|---|---|---|
| UUB | WP1 - Front-end | 4.5 |
| | WP2 - Trigger | 0.06 |
| | WP3 - Time Tagging | 0.3 |
| | WP4 - Slow Control | 0.07 |
| | WP5 - FPGA, Processor | 4.8 |
| | PMTs & Radio | 5.7 |
| | TOTAL with DC/DC at 97% of efficiency | 16.5 |

The total **peak** power estimate is 14.5W.
This is compatible with the current power consumption.

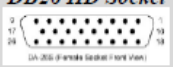
# UUB Connectors

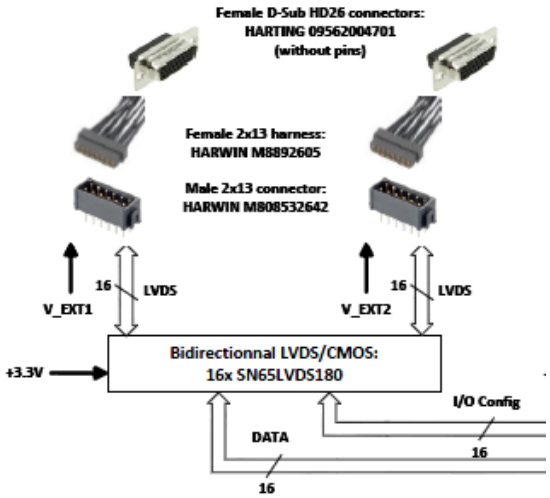
| Connector Ref. | Connector Type | Connector Function | Connected to | Comment |
|---|---|---|---|---|
| J11 | SMA, socket  | In, Anode PMT1 | PMT Anode 1 | On front panel |
| J12 | | In, Anode PMT1 | PMT Anode 2 | On front panel |
| J13 | | In, Anode PMT1 | PMT Anode 3 | On front panel |
| J14 | | In, Anode Small PMT | Small PMT An. | On front panel |
| J15 | | In, Analog 1 | Ext. detector 1 | On front panel<br>TBD |
| J16 | | In, Analog 2 | Ext. detector 2 | On front panel<br>TBD |
| J17 | | In, Analog 3 | Ext. detector 3 | On front panel<br>TBD |
| J21 | DB15HD socket  | In/Out, PMT1 monitoring | PMT base 1 | On front panel |
| J22 | | In/Out, PMT2 monitoring | PMT base 2 | On front panel |
| J23 | | In/Out, PMT3 monitoring | PMT base 3 | On front panel |
| J24 | | In/Out, Small PMT monitoring | Small PMT base | On front panel |
| J25 | | In/Out, PMT I monitoring | PMT base I | On front panel |
| J26 | | In/Out, PMT II monitoring | PMT base II | On front panel |
| J31 | | In, Slow control sensors reading | TPCB | On front panel |
| J41 | 10 pin (2x5) socket  | In/Out, GPS power and com. | GPS board | Internal |
| J51 | Binder 99-3431-202-04  | In, 24V power supply | TPCB | On front panel |
| J61 | SMA, socket  | Out, LED Flasher 1 cde. | LED Flasher 1 | On front panel |
| J62 | | Out, LED Flasher 2 cde. | LED Flasher 2 | On front panel |
| J71 | | In, External trigger input | TBD | On front panel |
| J72 | | Out, Internal trigger output | TBD | On front panel |
| J81 | USB Type B, Socket  | In/Out, System com. | Maintenance | On front panel |
| J82 | | In/Out, Slow Control com. | Maintenance | On front panel |
| J83 | USB Type A, Socket  | In/Out, maintenance | Maintenance | On front panel<br>100 mA maxi |
| J84 | RJ45, Socket  | In/Out, Ethernet | Maintenance | On front panel |
| J85 | SUBD9, socket  | In/Out, Radio interface | BSRU (radio) | On front panel |
| J91 | HARWIN M808542642 , socket  | In/Out, and out power supply | TBD | Internal, connected to DB26 HD on front panel |
| J92 | | In/Out, and out power supply | TBD | |
| J93 | HE14 2x7 pin  | In/Out, Jtag system | Maintenance | Internal |
| J94 | | In/Out, Jtag system | Maintenance | Internal |

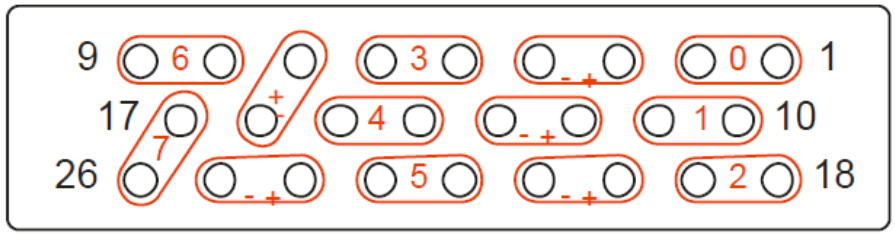


# Interface to additional detectors

Two connectors are provided with 8 differential lines individually defined as input or output which can be allocated in the FPGA, with switched 24V power supplies.

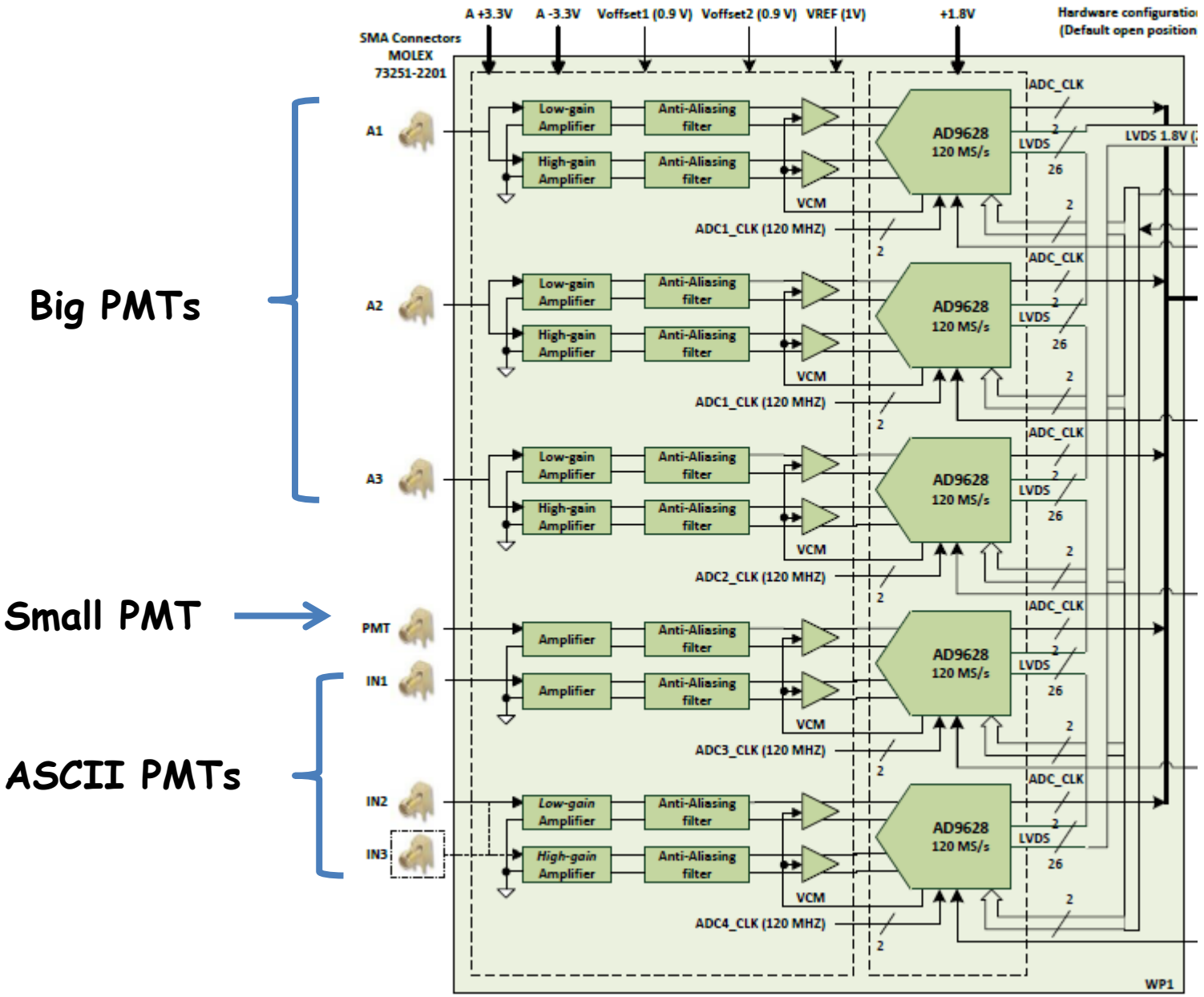
| *UUB Conn. ID* | *Name* | *Signal Name* | *UUB connector HE26, 2x13 Socket*  *Pin#* | *Front Panel connector DB26 HD Socket*  *Pin#* | *Signal description* |
|---|---|---|---|---|---|
| J91<br>J92 | EXT 1<br>EXT 2 | D1+ | 1 | 10 | Configurable |
| | | D1- | 2 | 11 | Configurable |
| | | VCC | 3 | 3 | +24V, unregulated, switchable |
| | | GND | 4 | 4 | Ground |
| | | D0+ | 5 | 1 | Configurable |
| | | D0- | 6 | 2 | Configurable |
| | | D2+ | 7 | 18 | Configurable |
| | | D2- | 8 | 19 | Configurable |
| | | VCC | 9 | 12 | +24V, unregulated, switchable |
| | | GND | 10 | 13 | Ground |
| | | D4+ | 11 | 14 | Configurable |
| | | D4- | 12 | 15 | Configurable |
| | | D3+ | 13 | 5 | Configurable |
| | | D3- | 14 | 6 | Configurable |
| | | VCC | 15 | 20 | +24V, unregulated, switchable |
| | | GND | 16 | 21 | Ground |
| | | D5+ | 17 | 22 | Configurable |
| | | D5- | 18 | 23 | Configurable |
| | | D6+ | 19 | 8 | Configurable |
| | | D6- | 20 | 9 | Configurable |
| | | VCC | 21 | 7 | +24V, unregulated, switchable |
| | | GND | 22 | 16 | Ground |
| | | D7+ | 23 | 17 | Configurable |
| | | D7- | 24 | 26 | Configurable |
| | | VCC | 25 | 24 | +24V, unregulated, switchable |
| | | GND | 26 | 25 | Ground |



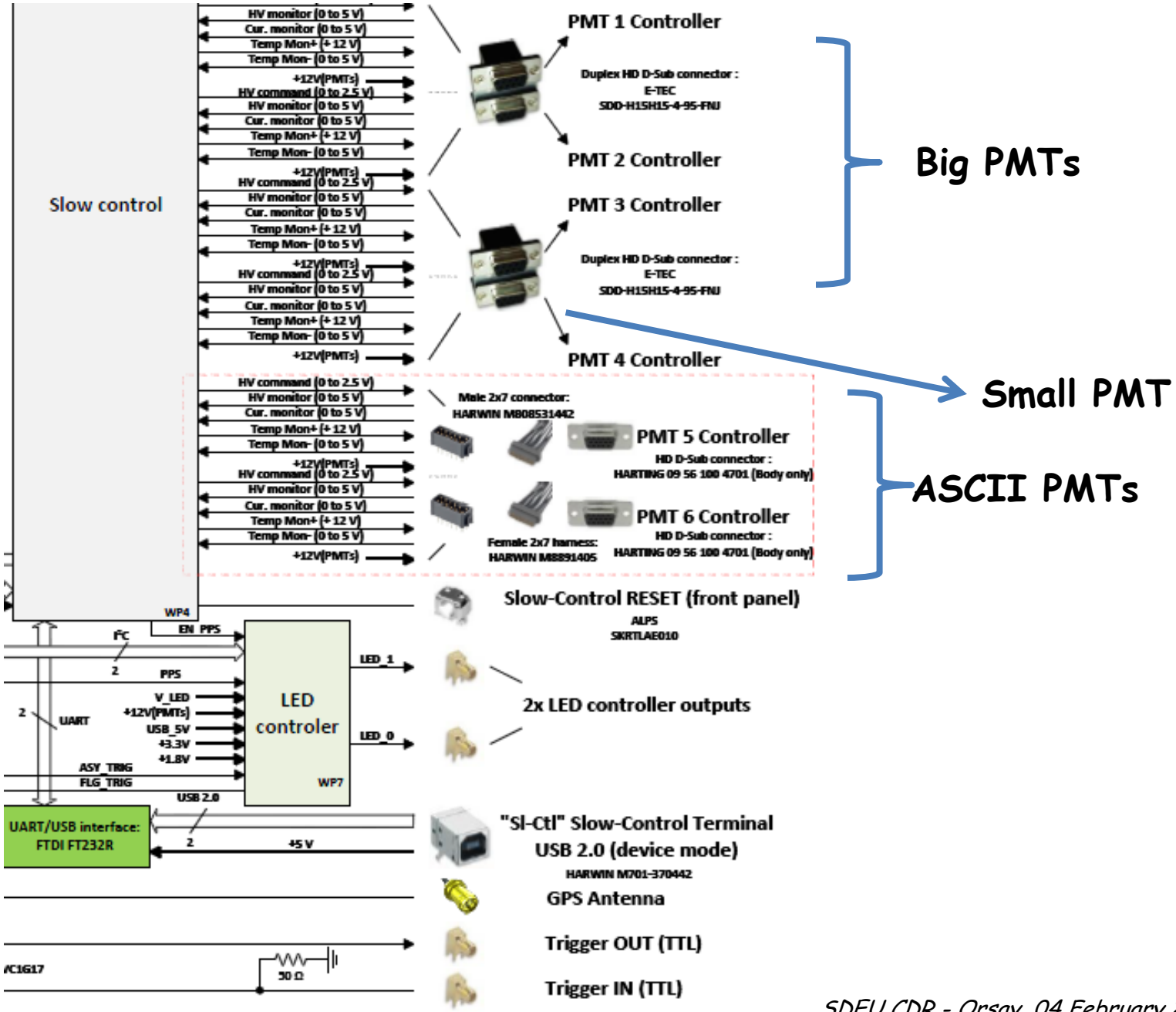




Front panel view

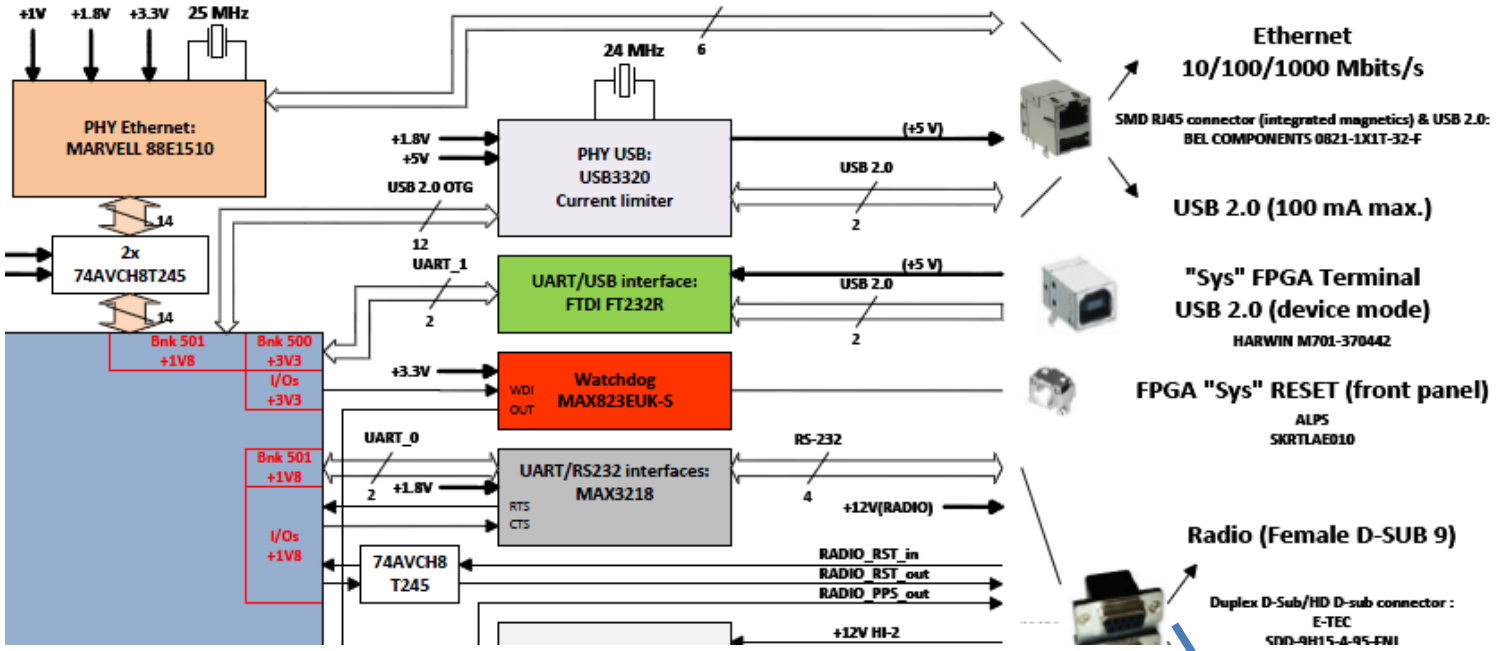
# UUB – PMTs analog inputs



# UUB – Slow Control I/Os, Trigger, GPS



# UUB – Communications




Radio

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# Risks & FMECA-FDIR

**WP10LPSC06C_SDEU_Project_Risk_Analysis_28Nov14**

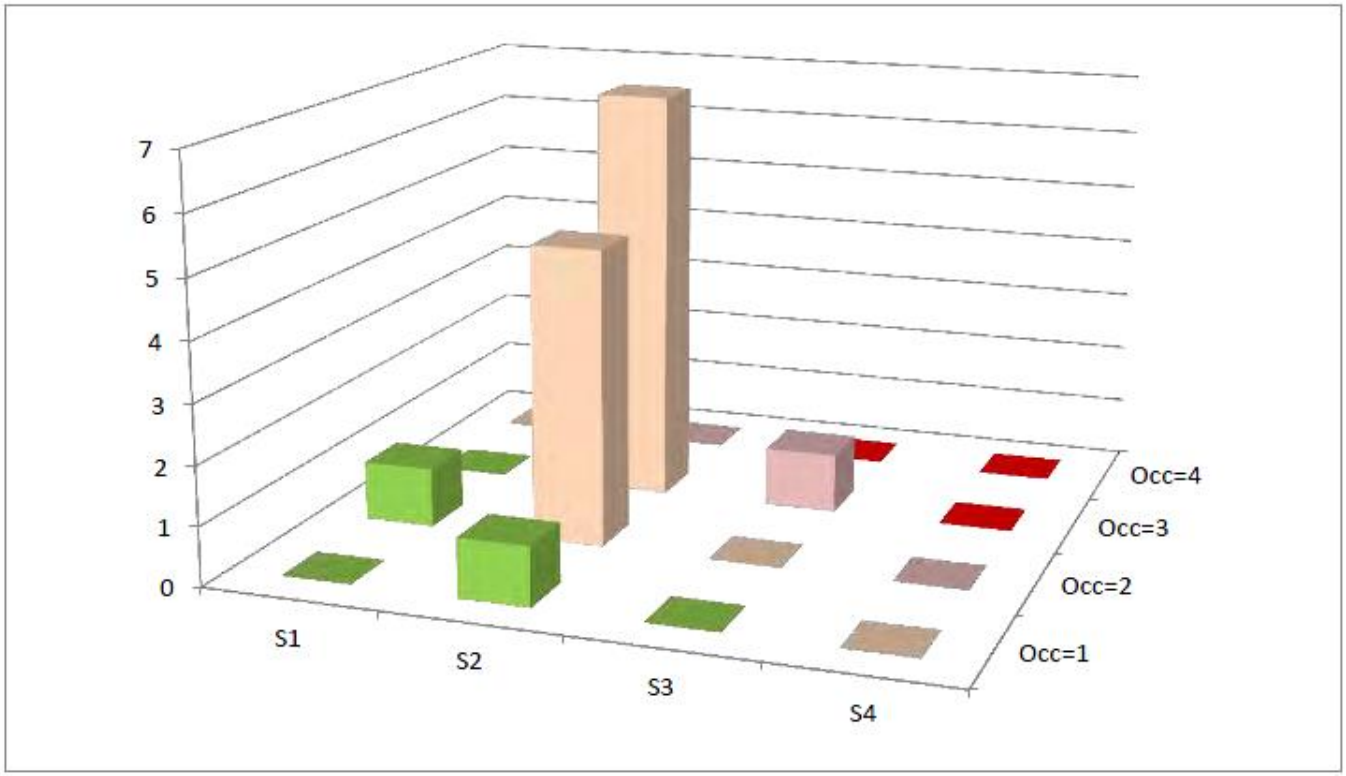
**WP10LPSC10C _SDEU_FMECA _FDIR_28Nov14**

# Project risks analysis

| N# | Risk Description | Mitigation | Reduction verification criteria |
|---|---|---|---|
| 1 | Risk of instability of the need for the project: (Change of priorities, instability of demand, insufficient strategic analysis). | Organize regular meetings and communication within the Pierre Auger Observatory community. | Reduction of the engineering change requests. |
| 2 | Risk of problems associated with the project partners (abandonment, non-priority project, regulations and different standards, economic and social situation, political instability, fiscal instability). | Organize work packages with multiple partners, with overlapped competences. | Multiple solutions are proposed for each design issue. |
| 3 | Funding risk: change of research policy medium/long term, alternative funding, unfavorable budgetary arbitration, absence or discount in question of multi-year funding. | Organize work packages with multiple partners, with different funding possibilities. | Funding easily available. |
| 4 | Risk of poor expression or lack of understanding of the scientific need. | Organize regular meetings and communication between scientists and designers and propose a accurate TDR. | TDR accurate and quickly available. |
| 5 | Risk of evolution of the scientific need after the start of the project. | Avoid too early specific design, leave margin in functionalities and allow design adjustment possibilities, especially for detector upgrade. Use engineering change request process. | Several key-point meetings and reviews organized every year. |
| 6 | Risk of missing, incomplete, insufficiently accurate specifications. | Spend time to produce a unique and stable specification document in collaboration with all people of the project. | Specification document accurate and quickly available. |
| 7 | Risk of innovative technical solutions, not validated in the laboratory or industrial. | Avoid as much as possible too much innovative design | Time reduction for R&D phases. |
| 8 | Risk of technical solutions used to boundaries (insufficient margins), or non-mature (no feedback) or exotic. | Reuse inheritage of recent designs like, Northern Auger, AERA, etc. | Time reduction for design phases. |
| 9 | Risk of uncontrolled material production, reception, testing, maintenance. | Have a strong, agreed and applied production and validation plan. Apply QAM plan. | Clear tracking documentation. |
| 10 | Risk associated with the transport of components, subsystems or system. | Use sure and safe proven transportation procedures, domestic and international. | Reduction of the casualties |
| 11 | Risk of non-implementation of the quality assurance by the manufacturer (traceability, monitoring, non-conformity management, change management). | Include quality assurance criteria in the selection process of the manufacturers. | Manufacturer quality assurance plan available. |
| 12 | Risks related to the internal interfaces of the project: lack of definition, requirements volatility, poor or no coordination.. | Organize regular internal meetings and communication between WP and system engineering. | Delay reduction in the global schedule. |
| 13 | Risk of wrong announced date of one or more phases of the project, consequences:<br>a) Interference between several phases of the project (e.g. R & D and production).<br>b) Interference with other projects. | Establish a realistic schedule, frequently updated, agreed by all people involved in the project realizations. | Delay reduction in the global schedule. |
| 14 | Risk on the sustainability of human resources: retirement, mobility project of people having knowledge not easily replaceable. | Organize work packages with multiple partners, working in team with overlapped competences. | Increase of the number of persons involved in the WPs. |

# Project risks analysis

| Likelihood | | | | | Color = Risk Index |
|---|---|---|---|---|---|
| Occ=4 | | *CP* | *CP* | *CP* | High |
| Occ=3 | | 7 risks | 1 risk | *CP* | Medium |
| Occ=2 | 1 risk | 5 risks | | *CP* | Low |
| Occ=1 | | 1 risks | | | Very Low |
| | S1 | S2 | S3 | S4 | Global Severity |



# Technical risks - FMECA

PIERRE AUGER OBSERVATORY

| ID # | ITEM (component) | Function | Failure Mode ID# | Severity | Failure Effect Probability (β) | Failure Mode Ratio (α) | Failure Rate (λp) | Operating Time (t, hours) | Failure Mode Criticality (Cm) | Item Criticality (Cr) | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ADA4927 | Amplifier | 1.2 | IV. Minor | 0.1 | 0.5 | 0.039 | | 256.23 | 512.46 | |
| | | | 1.3 | IV. Minor | 0.1 | 0.5 | | | 256.23 | | |
| 2 | Discrete SMD | Filter | 1.4 | IV. Minor | 0.1 | 1 | 0.720 | | 9460.80 | 9460.80 | |
| 3 | SMA socket conn. | I/O connection | 1.1 | IV. Minor | 0.1 | 0.7 | 0.011 | | 101.18 | 144.54 | |
| | | | 5.2 | IV. Minor | 0.1 | 0.3 | | | 43.36 | | |
| 4 | AD9628 | FADC | 2.1 | IV. Minor | 0.5 | 01 | 0.065 | | 4270.50 | 4270.50 | |
| 5 | ZINQ 7020 | FPGA | 3.3 | II Critical | 0.5 | 0.1 | 0.530 | | 3482.10 | 34821.00 | |
| | | | 3.9 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 3.11 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 5.3 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 6.2 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 6.5 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 6.8 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 6.11 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 6.14 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| | | | 6.17 | II Critical | 0.5 | 0.1 | | | 3482.10 | | |
| 6 | MT42L128M32D | Memories | 3.4 | II Critical | 0.5 | 1 | 0.140 | | 9198.00 | 9198.00 | |
| 7 | N25Q00AA13GSF40 | Memories | 3.4 | II Critical | 0.5 | 1 | 0.071 | | 4664.70 | 4664.70 | |
| 8 | M12M I-Lotus | GPS board | 3.12 | III. Marginal | 0.5 | 0.5 | 0.030 | | 985.50 | 1971.00 | |
| | | | 5.5 | III. Marginal | 0.5 | 0.5 | | | 985.50 | | |
| 9 | T2000 Motorola | GPS Antenna | 3.14 | III. Marginal | 0.1 | 0.5 | 0.011 | 131400 (15 years) | 72.27 | 144.54 | |
| | | | 5.5 | III. Marginal | 0.1 | 0.5 | | | 72.27 | | |
| 10 | N Socket Conn | Antenna conn. | 3.13 | III. Marginal | 0.1 | 0.5 | 0.011 | | 72.27 | 144.54 | |
| | | | 5.5 | III. Marginal | 0.1 | 0.5 | | | 72.27 | | |
| 11 | MPS430F2618 | Micro controller | 4.1 | II Critical | 0.3 | 0.5 | 0.490 | | 9657.90 | 19315.80 | |
| | | | 4.10 | II Critical | 0.3 | 0.5 | | | 9657.90 | | |
| 12 | ADG608 | Multiplexor | 4.5 | III. Marginal | 0.5 | 0.5 | 0.066 | | 2168.10 | 4336.20 | |
| | | | 4.8 | II Critical | 0.5 | 0.5 | | | 2168.10 | | |
| 13 | LTC2637 | DAC | 4.8 | II Critical | 0.3 | 1 | 0.066 | | 2601.72 | 2601.72 | |
| 14 | BMP085 | Pressure sensor | 4.4 | III. Marginal | 0.1 | 1 | 0.020 | | 262.80 | 262.80 | |
| 15 | LM224D | Amplifier | 5.1-5.7 | IV. Minor | 0.5 | 1 | 0.039 | | 2562.30 | 2562.30 | |
| 16 | AD5316 | DAC | 5.1-5.7 | IV. Minor | 0.5 | 1 | 0.066 | | 4336.20 | 4336.20 | |
| 17 | MMBT3904LT1 | Transistor | 5.1-5.7 | IV. Minor | 0.3 | 1 | 0.160 | | 6307.20 | 6307.20 | |
| 18 | Marvell 88E1518 | ETH Interface | 6.1 | IV. Minor | 0.7 | 1 | 0.080 | | 7358.40 | 7358.40 | |
| 19 | USB 3320 | USB OTG Interface | 6.4 | IV. Minor | 0.7 | 1 | 0.080 | | 7358.40 | 7358.40 | |
| 20 | FTDIFT32232R | USB Interface | 6.7 | IV. Minor | 0.7 | 0.5 | 0.080 | | 3679.20 | 7358.40 | |
| | | | 6.10 | IV. Minor | 0.7 | 0.5 | | | 3679.20 | | |
| 21 | MAX3218 | Serial interface | 6.13 | IV. Minor | 0.7 | 1 | 0.080 | | 7358.40 | 7358.40 | |
| 22 | DS90LV047ATM | Buffers drivers | 6.16 | IV. Minor | 0.7 | 1 | 0.080 | | 7358.40 | 7358.40 | |
| 23 | LM3150 | DC/DC converter | 7.1 | III. Marginal | 0.5 | 0.25 | 0.065 | 131400 | 533.81 | 2135.25 | |

# Technical risks - FMECA

| Part Reference | Part ID # | Part Criticality (Cr) | Number of Failure Mode | | | |
|---|---|---|---|---|---|---|
| ZINQ 7020 | 5 | 34821.00 | | | 10 | |
| ? FUSE | 32 | 22075.20 | 1 | | | |
| MPS430F2618 | 11 | 19315.80 | | | 2 | |
| BSS138P | 29 | 10512.00 | | 1 | 1 | |
| Discrete SMD | 2 | 9460.80 | 1 | | | |
| MT42L128M32D | 6 | 9198.00 | | | 1 | |
| Marvell 88E1518 | 18 | 7358.40 | 1 | | | |
| USB 3320 | 19 | 7358.40 | 1 | | | |
| FTDIFT32232R | 20 | 7358.40 | 2 | | | |
| MAX3218 | 21 | 7358.40 | 1 | | | |
| DS90LV047ATM | 22 | 7358.40 | 1 | | | |
| MMBT3904LT1 | 17 | 6307.20 | 2 | | | |
| BC846B | 30 | 6307.20 | 1 | | | |
| FDN358P | 31 | 6307.20 | 1 | | | |
| N25Q00AA13GSF40 | 7 | 4664.70 | | | 1 | |
| ADG608 | 12 | 4336.20 | | 1 | 1 | |
| AD5316 | 16 | 4336.20 | 2 | | | |
| AD9628 | 4 | 4270.50 | 1 | | | |
| LM3150 | 23 | 4270.50 | | 2 | 2 | |
| TPS54020 | 26 | 4270.50 | | | 1 | |
| TPS40170 | 28 | 4270.50 | | | 1 | |
| TPS62125 | 25 | 4266.23 | | 1 | 2 | |
| LMR24220 | 27 | 4266.23 | 1 | 1 | 1 | |
| LTC2637 | 13 | 2601.72 | | | 1 | |
| LM224D | 15 | 2562.30 | 2 | | | |
| LTC1174 | 24 | 2299.50 | | 1 | | |
| M12M I-Lotus | 8 | 1971.00 | | 2 | | |
| ADA4927 | 1 | 512.46 | 2 | | | |
| BMP085 | 14 | 262.80 | | 1 | | |
| T2000 Motorola | 9 | 144.54 | | 2 | | |
| N Socket Conn | 10 | 144.54 | | 2 | | |
| SMA socket conn. | 3 | 144.54 | 2 | | | |
| | | | IV | III | II | I |

Increasing level of Item Criticality →

Increasing level of Severity →

- Separate power supplies between FPGA and micro controller
- Do not provide voltage to all DC/DC with only one DC/DC converter avoiding to create a single point failure (SPF) on the power supply unit
- Implement internal voltage and current monitoring, in addition to an internal failure detection, isolation and recovery (FDIR) mechanism performed by the Slow Control micro controller (WP7).
- Implement DC/DC protections and technics to improve their reliability.
- Use secure mechanisms in the S/W to read and write memories to be able to detect memory failure.
- Use gold plated connectors and keep a high level on cleanliness.
- Use high reliability cabling and soldering process to avoid bad connections and contacts.
- Use inverted logic for on board switches (normal state in open circuit)

# Technical risks - FDIR

All the failure described here will trigger action only from the Slow Control, Unit.

| ID# | Failure Mode | Detection Method | Symptom Trigger | Isolation | Recovery | Slow Control Actions |
|---|---|---|---|---|---|---|
| 1 | FPGA S/W failure a loading | An acknowledge message is send by the FPGA to signal a good S/W loading | No acknowledge message received | Yes | Yes | - Load a mirrored version of the S/W sited in in another part of the memory<br>- Write a message in the non-volatile Slow Control memory |
| 2 | FPGA core voltage failure | The core voltage is monitored every second | The core voltage is below 0.9 Volts | Yes | No | - Shut down all the FPGA power supplies in a delay below one second<br>- Write a message in the non-volatile Slow Control memory |
| 3 | Symmetric voltage failure | The symmetric power supply is monitored every second | One of the polarity voltage values of the symmetric power supply is different with more than 10 % of the other, regardless of the polarity. | Yes | No | - Shut down the symmetric power supply in a delay below one second<br>- Write a message in the non-volatile Slow Control memory |
| 4 | External 24V failure | The voltage and the current on the +24V provided on the 2 extension connectors are monitored every second | - The voltage value after the switch is below 17 Volts<br>- The current value on each line is over 100 mA per line | Yes | No | - Shut down the considered +24V line on the extension connector<br>- Write a message in the non-volatile Slow Control memory<br>- Send an alarm on the telemetry for the monitoring S/W (TBC) |

PIERRE AUGER OBSERVATORY

# AIT – AIV Plan

**WP10LPSC11D_SDEU_AIT_AIV_Plan_28Nov14**

# UUB Models philosophy

***Prototype Boards (PrtB)***

This model is needed to test and validate the design of the SDEU. 5 plus 20 units of PrtB will be realized and tested at various plants. 10 units will be shipped to PAO site to be tested on the engineering array.

***Pre-production Boards (PpB)***

The PpB model is needed for manufacturer qualification. 100 units are foreseen for this purpose. If more than one manufacturing site will be identifier the numbers of PpB will be adapted.

***Production Boards (PB)***

From 1900 to 2000 units or the PB model will be manufactured on one or more production sites.

# UUB Verification Tools

***Tank Simulator (TS)***

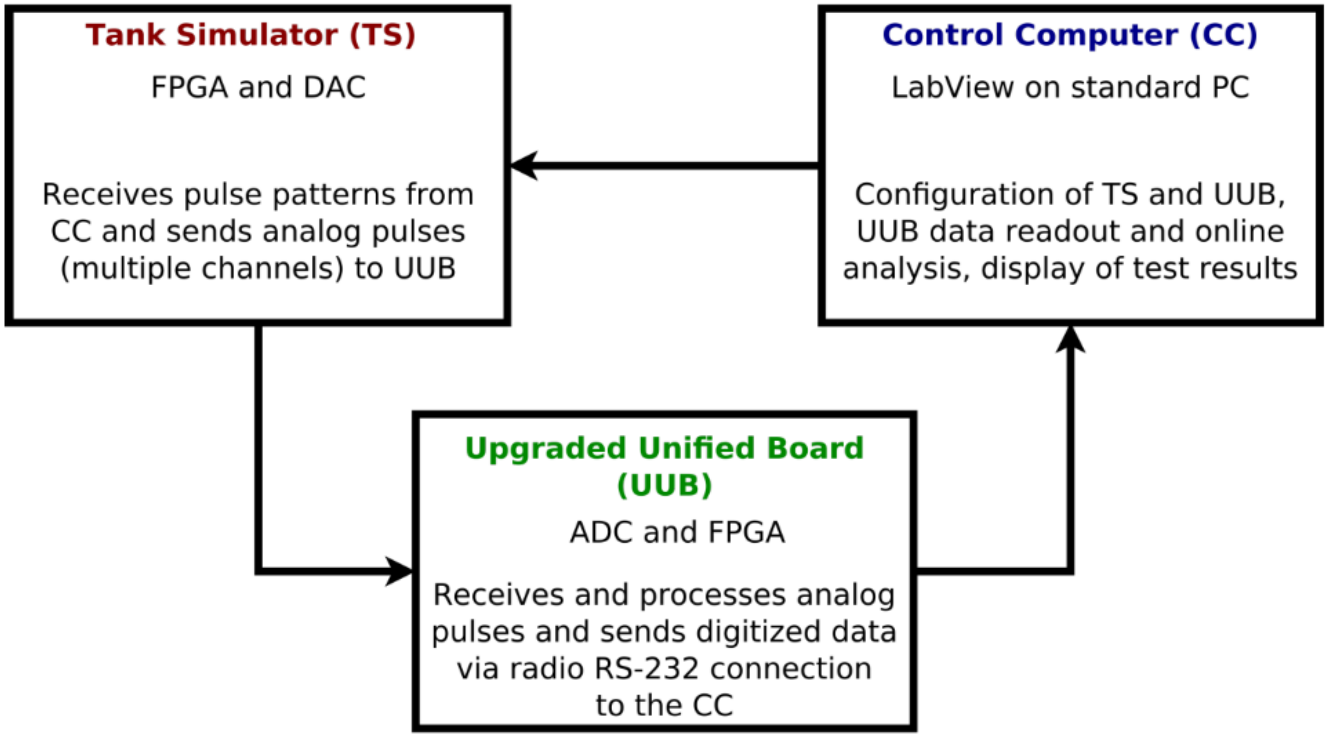
To verify all the requirements of the SDEU and also to be able to operate it at the various test plant, a "Tank Simulator" will be built, not only able to generate or receive and monitor signals to and from the UUB under test, but also able to have the basic behavior of the real tank and devices around.
Additionally, this kind of simulator can be easily reproduced and spread through the different partners, allowing sharing test and validation activities.

The "Tank Simulator" should be able to be used for the specification validation of the UUB but also for the functional verification, fabrication and production validation and reception, maintenance and failure detection and recovery.

***Engineering Array (EA)***

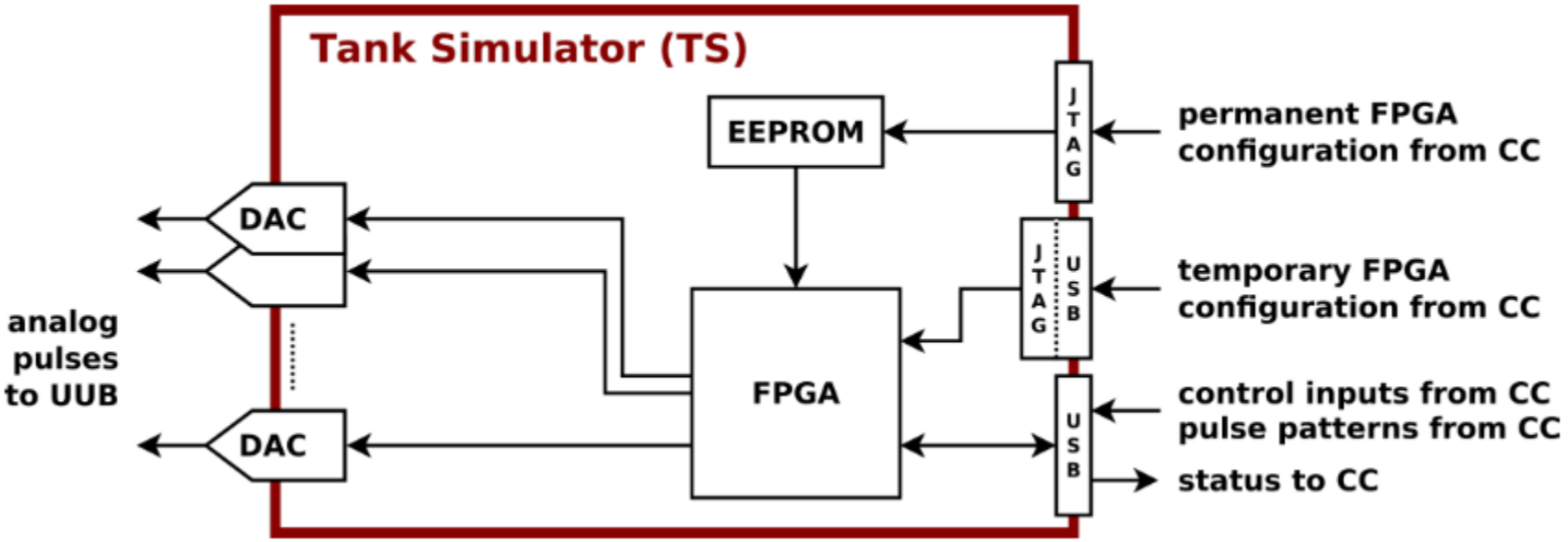
A small area, including a set of an array of 7 Water Cerenkov Tanks (WCT), dedicated for test and validation will be setup in a TBD place of the SD area.
These Engineering Array (EA) WCT will be equipped with the power supply system, and the whole communication setup. Large and small PMTs and LED flasher will be also installed.
The EA purpose is complete the validation of the UUB design verify the performances of the SD equipped with the UUB, in situ.

# Tank simulator – Test Set Up



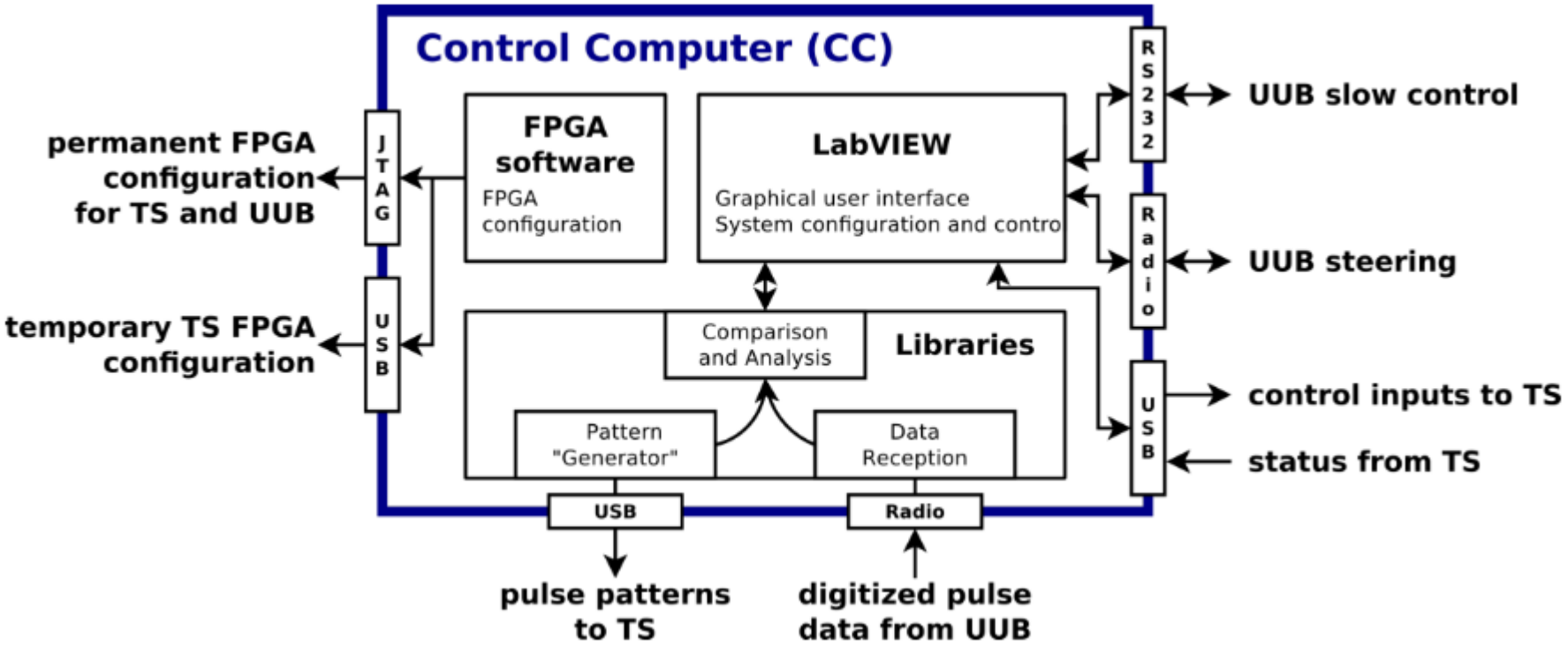

- It consist of two parts, a control computer (CC) with the user interface and a tank simulator (TS).
- The TS is an FPGA-driven device, which will provide analog data for the UUB which processes it and transmits the processed digital data to the CC.
- The received data in the CC is then compared with the expected answer of the UUB to the given analog input.

# Tank simulator – Block diagram



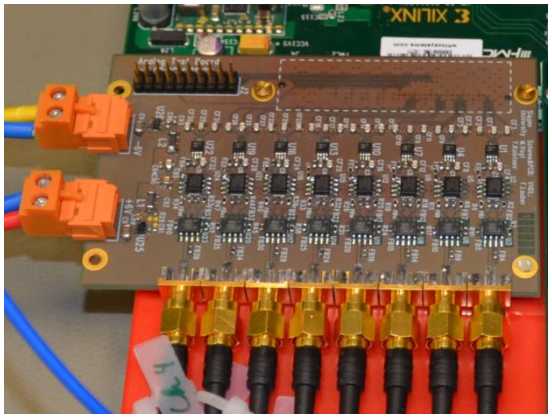

- The input signals are generated with help of an FPGA (Xilinx Zynq).
- Fast and/or complicated analog signals (for UUB ADC inputs) are produced by a FPGA-controlled signal generator.
- Current setup: Zynq FPGA on ZC702 evaluation board.
  Later: Custom FPGA board.

# Control Computer – Block diagram

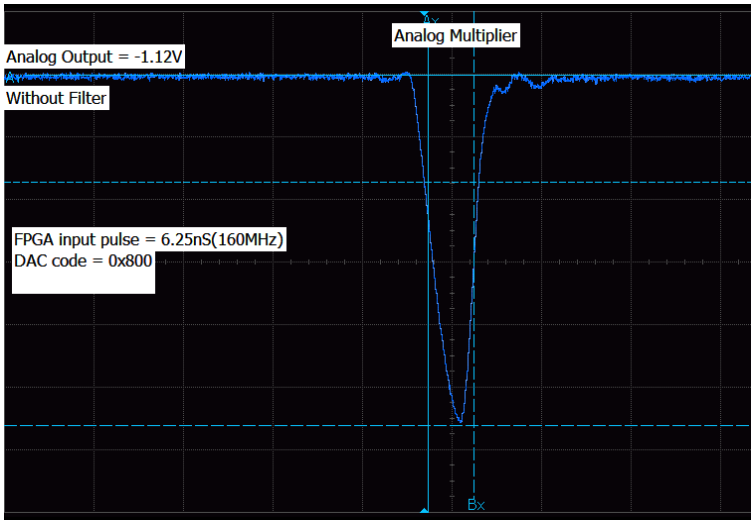


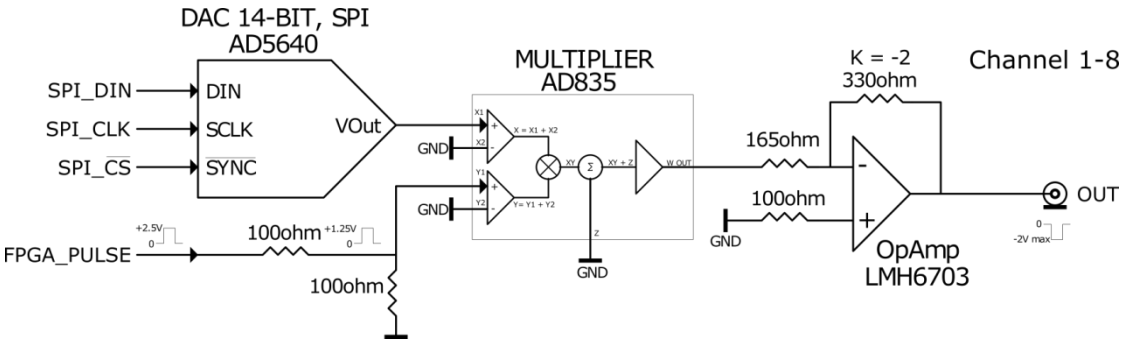

- The UUB receives signals at its inputs and provides output data via the "RS232" radio interface.
- From the LabVIEW interface, all configurations for the TS can be loaded and transmitted.
- The GUI will provide status output on the performed measurements. This includes an online comparison between the expected digitization result and the digital data returned.

# Tank simulator – Analog signal



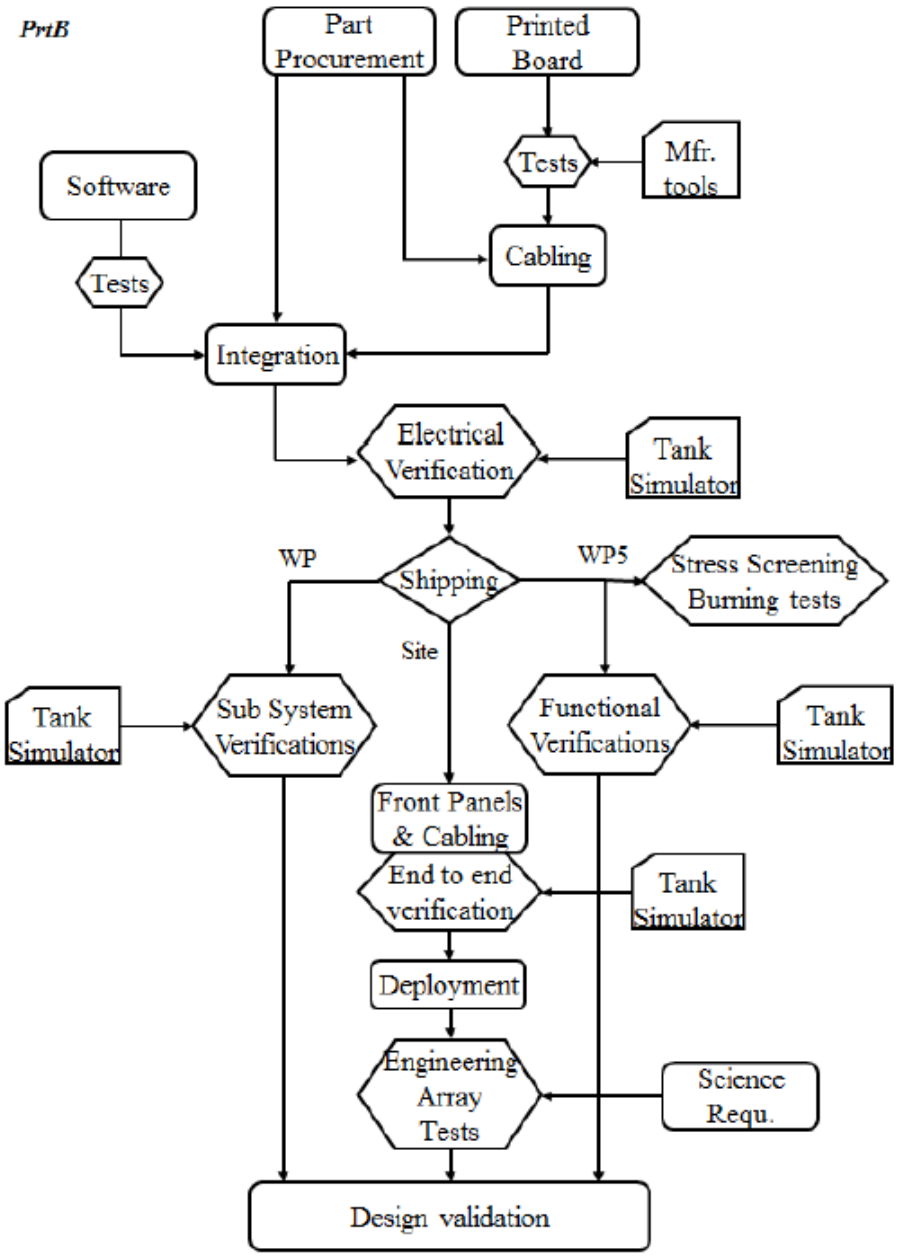
- 8 channel board for use with Xilinx ZC702 evaluation board already produced and evaluated.
- Currently implementing serial communication for dynamic generation of pulse patterns.



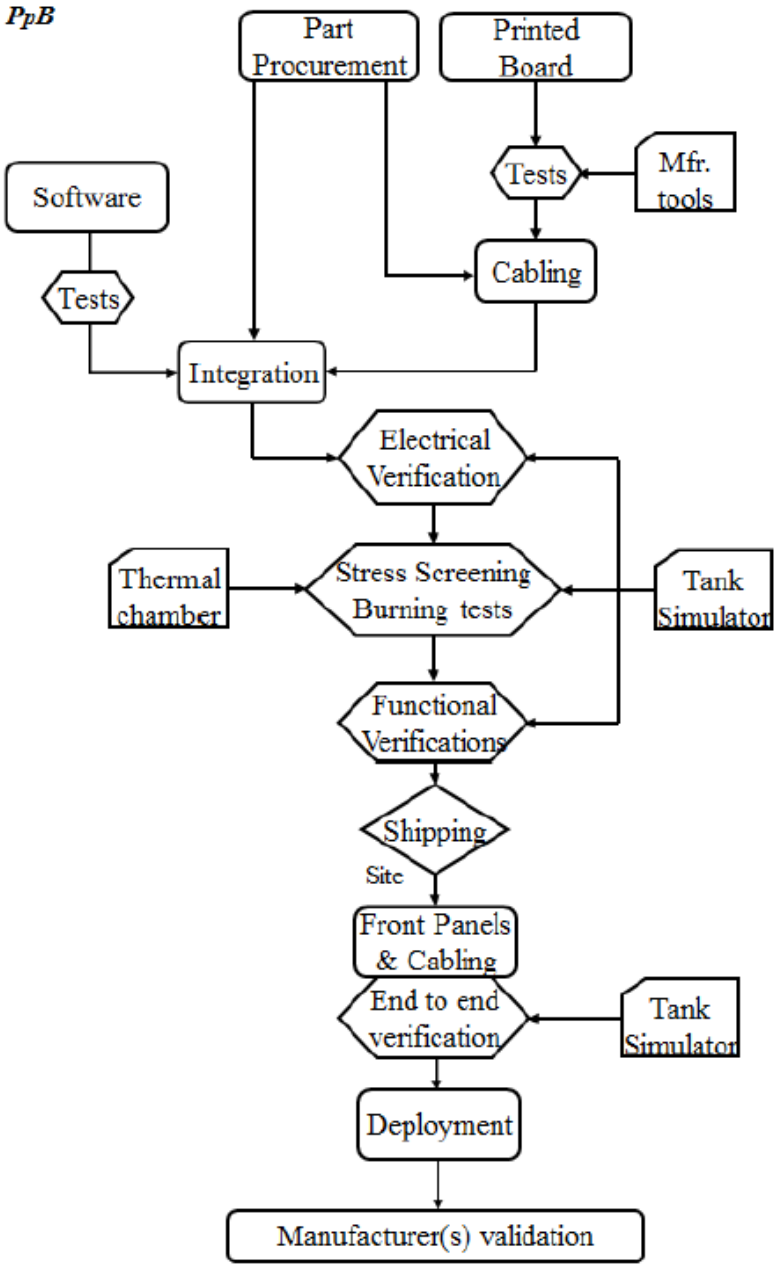




**Shaped pulses with arbitrary length and amplitude.**

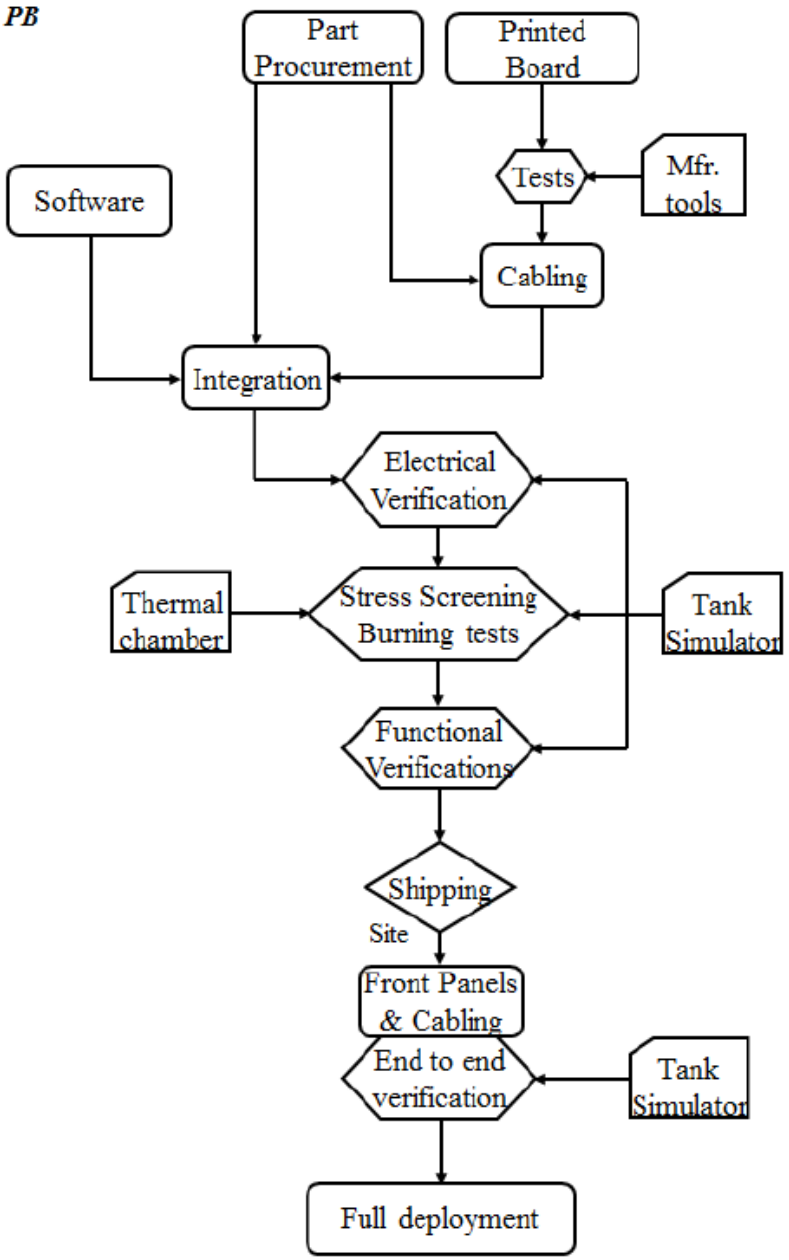
# Prototype Board Verification flow



# Pre-production Board Verification flow



# Production Board Verification flow



# Assembly and tests


- Process in Malargüe (SDECo)
- Receiving inspection
- Functionality test
- Assembly to Ekit
- End-to end-test

The SDE Upgrade process follow the QMP of the current SDE and the QA of the Pierre Auger Observatory.

PIERRE AUGER OBSERVATORY

# Small PMT Design

# Cost & Schedule

**WP10-LPSC-08J-SDEU_WBS_24Jun14**

**WP10LPSC04K_SDEU_Project_28Nov14**

# Cost – WBS SDEU & SPMT

PIERRE AUGER OBSERVATORY

Pierre Auger Observatory - Cost Estimate - Surface Detector Electronics Upgrade — 24 June 2014

| WBS | | Activity | Total Cost with Cont. | | Material, Service & Labor costs paid by the Project | | Infrastructure Labor Cost (not paid by the project) | |
|---|---|---|---|---|---|---|---|---|
| | | | € | $ | € | $ | € | $ |
| 1 | WP | SDEU | 2 614 720 | 3 399 136 | 1 988 468 | 2 585 008 | 626 252 | 814 128 |
| 1.1 | WP1 | PMTs signal Conditioning | 81 410.00 | 105 833.00 | 21 000.00 | 27 300.00 | 60 410.00 | 78 533.00 |
| 1.2 | WP2 | Trigger | 20 570.00 | 26 741.00 | 20 570.00 | 26 741.00 | 0.00 | 0.00 |
| 1.3 | WP3 | Time Tagging | 163 807.50 | 212 949.75 | 163 807.50 | 212 949.75 | 0.00 | 0.00 |
| 1.4 | WP4 | Slow Control | 85 700.50 | 111 410.65 | 27 968.00 | 36 358.40 | 57 732.50 | 75 052.25 |
| 1.5 | WP5 | Upgraded Unified Board | 1 806 214.50 | 2 348 078.85 | 1 577 232.50 | 2 050 402.25 | 228 982.00 | 297 676.60 |
| *1.5.1* | *WP5* | *Upgraded Unified Board (Prototype)* | *174 482.50* | *226 827.25* | *46 400.00* | *60 320.00* | *128 082.50* | *166 507.25* |
| *1.5.2* | *WP5* | *Upgraded Unified Board (Pre-Production)* | *207 542.00* | *269 804.60* | *118 700.00* | *154 310.00* | *88 842.00* | *115 494.60* |
| *1.5.3* | *WP5* | *Upgraded Unified Board (Production)* | *1 370 740.00* | *1 781 962.00* | *1 358 682.50* | *1 766 287.25* | *12 057.50* | *15 674.75* |
| *1.5.4* | *WP5* | *Upgraded Unified Board test benches* | *53 450.00* | *69 485.00* | *53 450.00* | *69 485.00* | *0.00* | *0.00* |
| 1.6 | WP6 | Software | 103 967.50 | 135 157.75 | 20 475.00 | 26 617.50 | 83 492.50 | 108 540.25 |
| 1.7 | WP7 | Calibration and control tools | 30 292.50 | 39 380.25 | 6 160.00 | 8 008.00 | 24 132.50 | 31 372.25 |
| 1.8 | WP8 | Assembly and deployment | 145 697.50 | 189 406.75 | 79 755.00 | 103 681.50 | 65 942.50 | 85 725.25 |
| 1.9 | WP9 | Simulation and science validation | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 1.10 | WP10 | Project management | 177 060.00 | 230 178.00 | 71 500.00 | 92 950.00 | 105 560.00 | 137 228.00 |

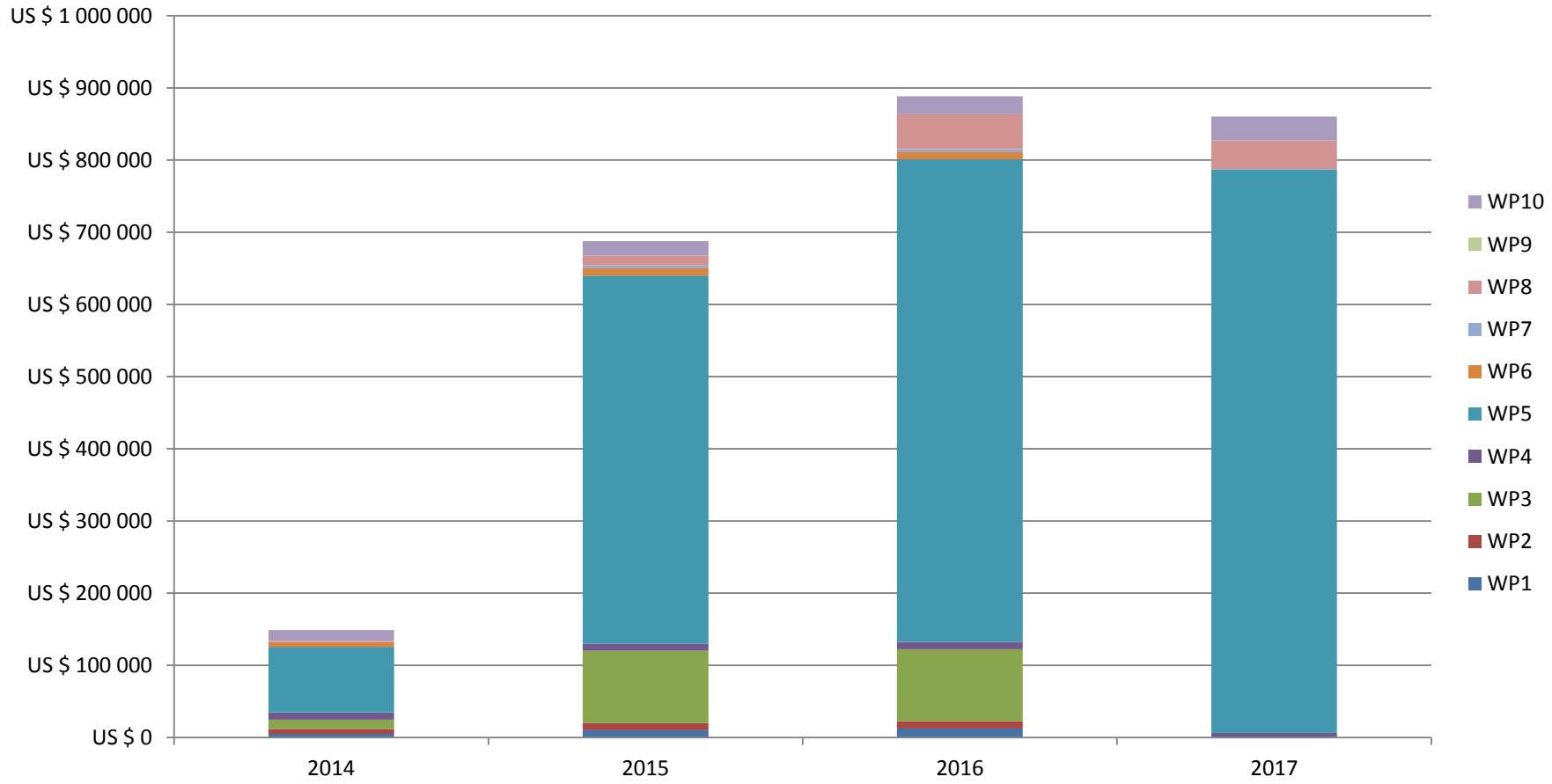
Pierre Auger Observatory - Cost Estimate - Small Photomultiplier Tube

| | | | | | | |
|---|---|---|---|---|---|---|
| 2 | WP | SPMT | | | 896 500 | 1 165 450 |
| | | | | Total | 2 884 968 | 3 750 458 |

25 prototypes boards (UUB) 60 320,00 US$ (~2500$/unit)

Production: 2000 boards (UUB) 1 766 287,00 US$ (~900$/unit)

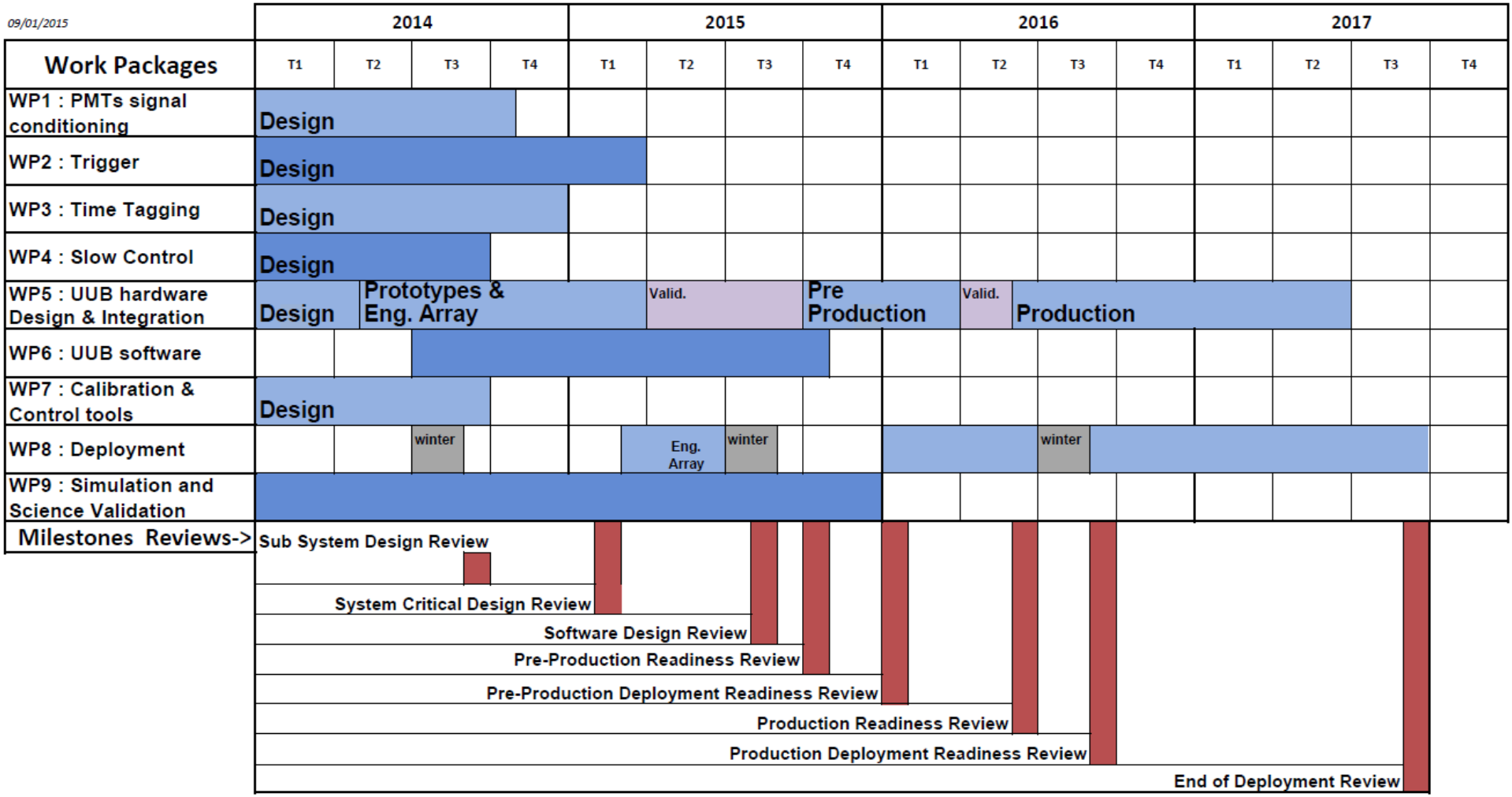
# Cost - Funding profile



# Schedule

PIERRE AUGER OBSERVATORY

09/01/2015



# Schedule

PIERRE AUGER OBSERVATORY

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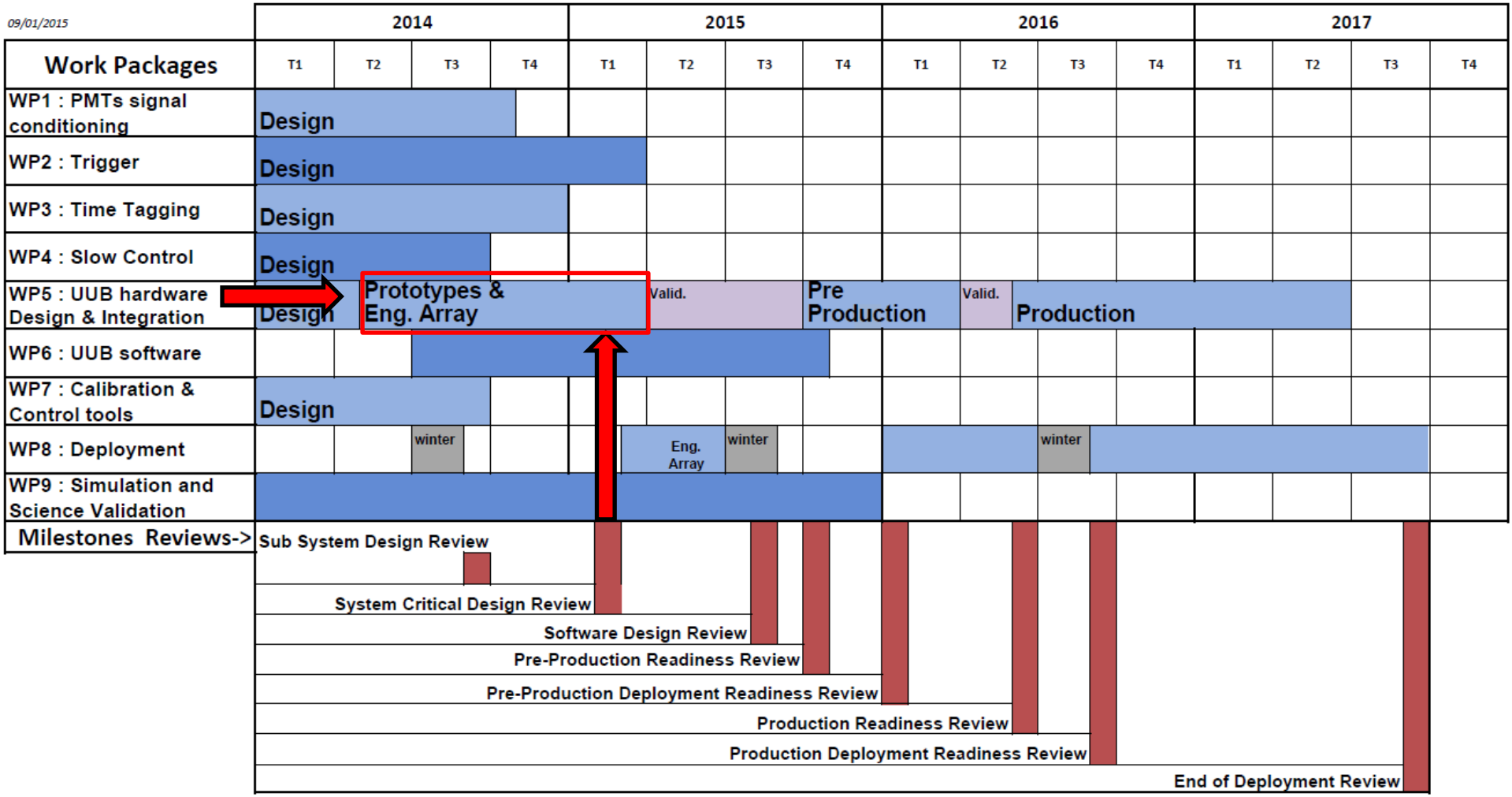
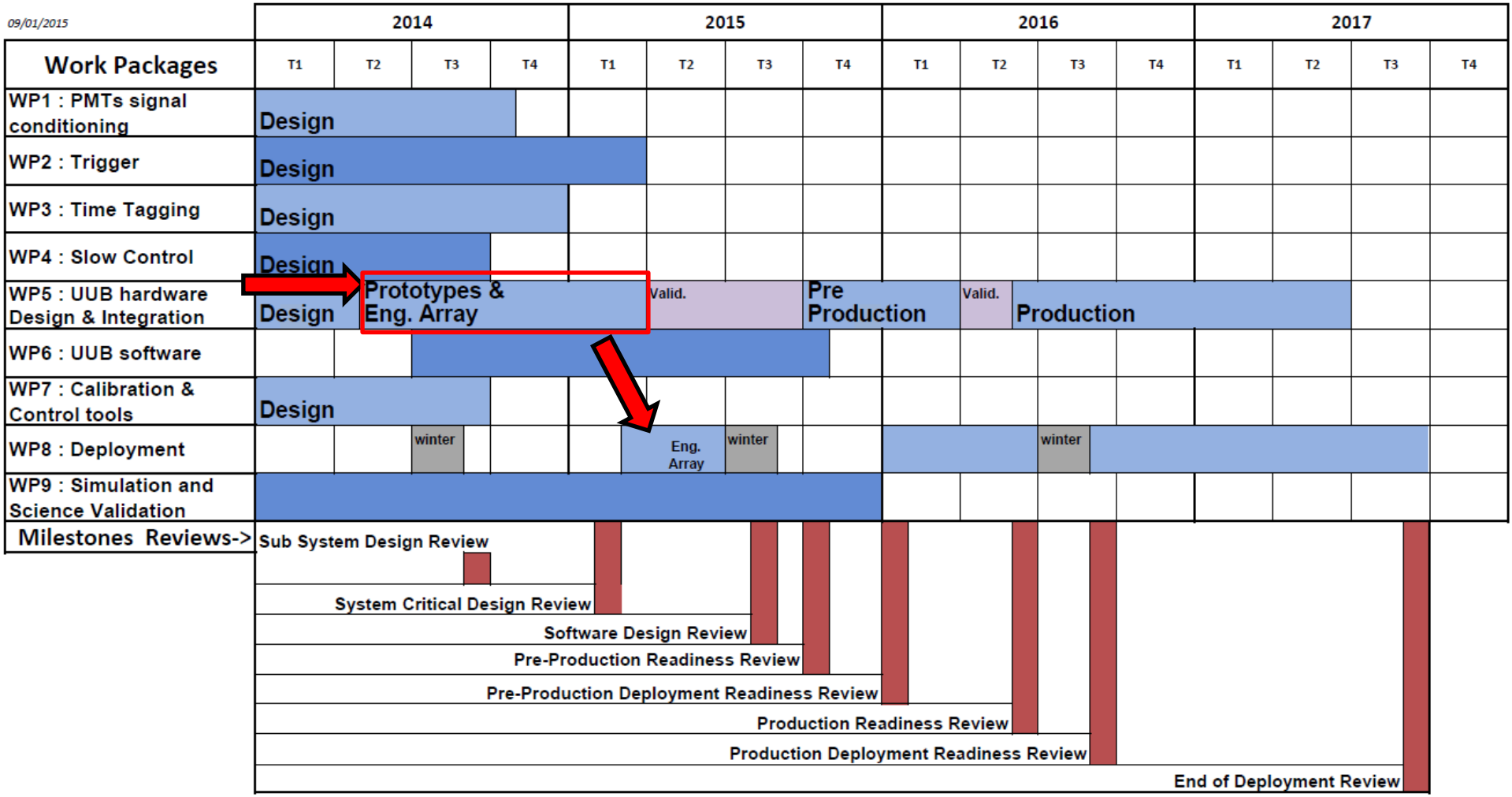


# Schedule

PIERRE AUGER OBSERVATORY

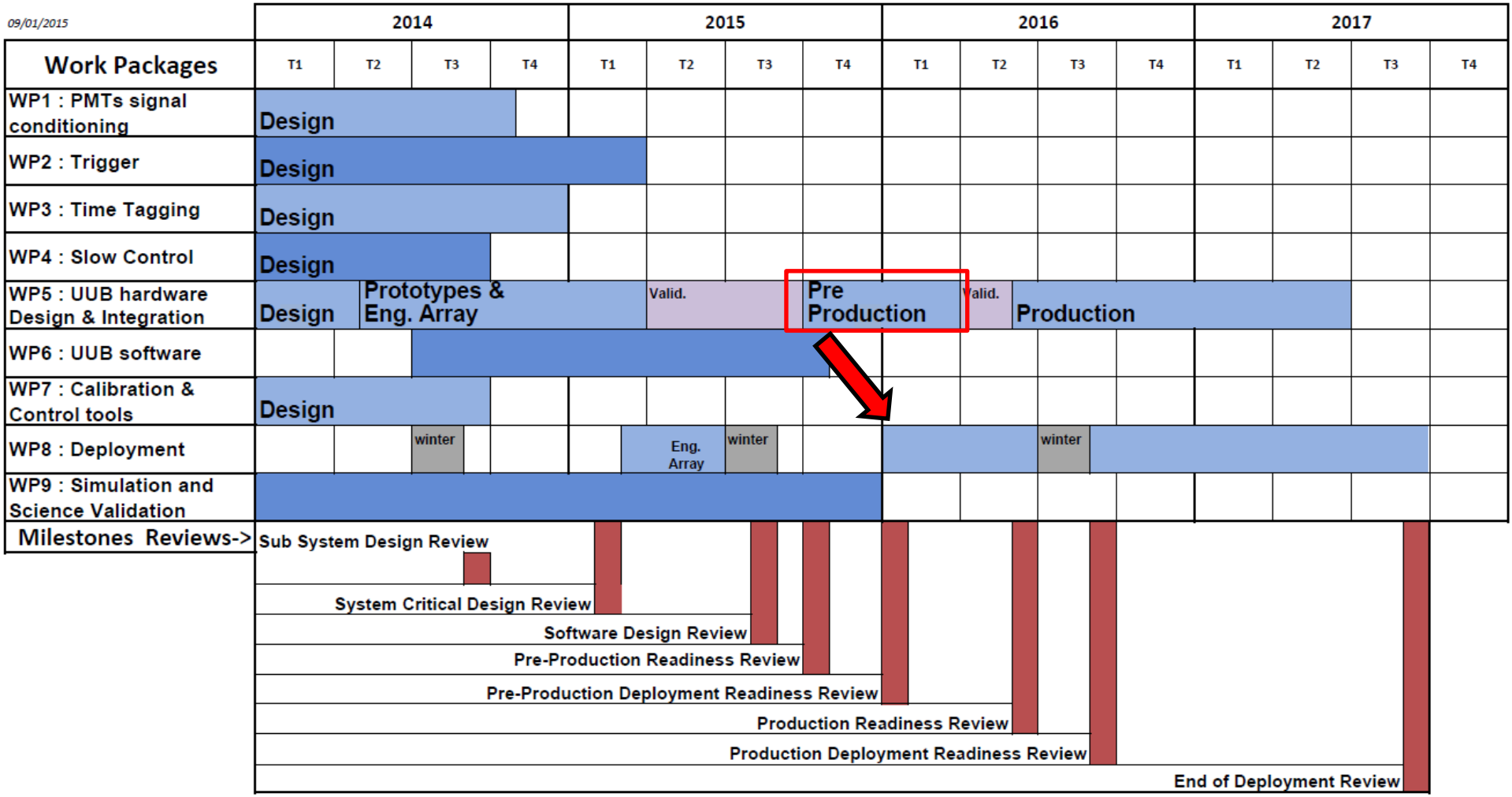
09/01/2015



# Schedule

PIERRE AUGER OBSERVATORY

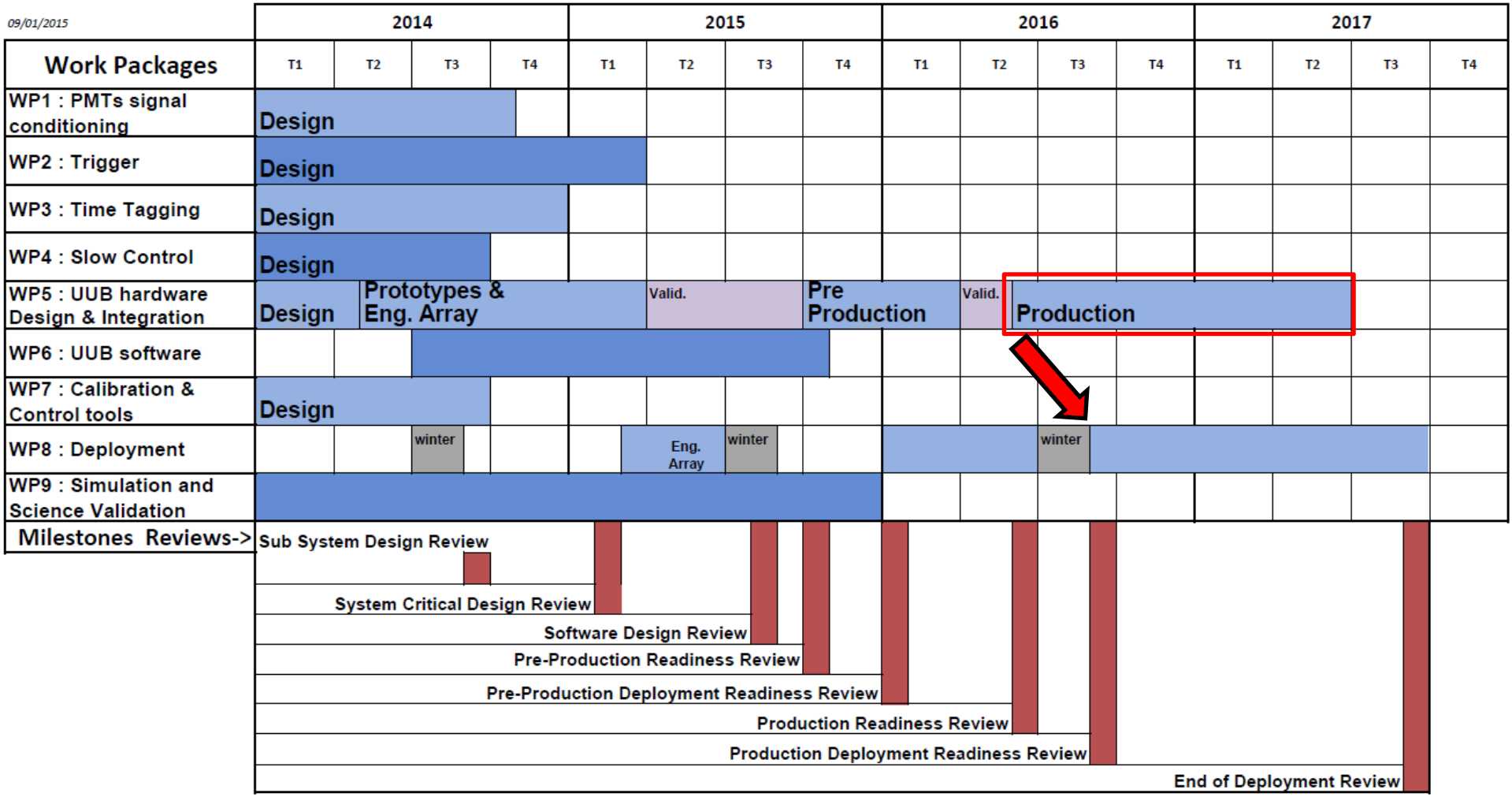
09/01/2015



# Schedule

PIERRE AUGER OBSERVATORY

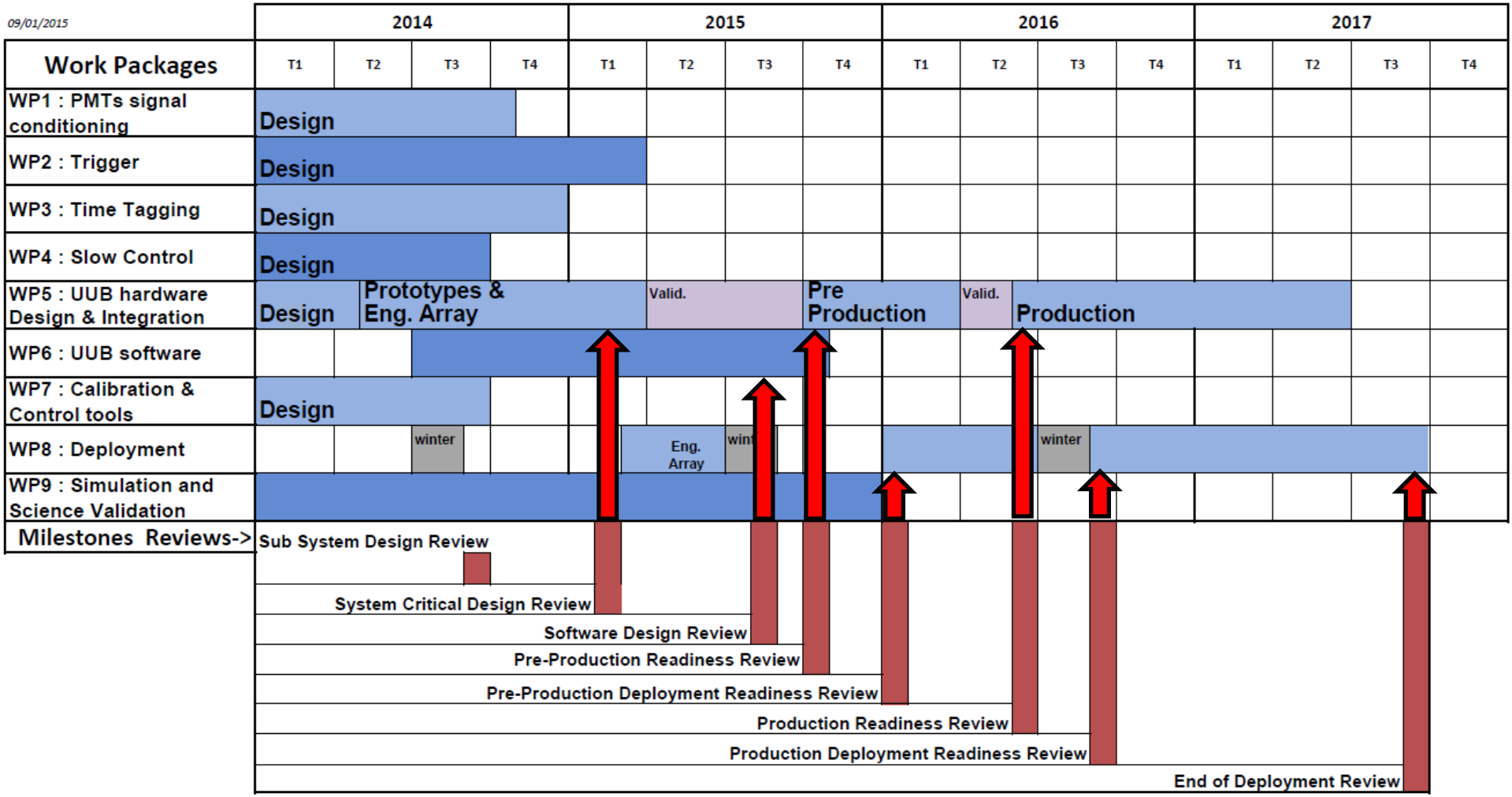
09/01/2015



# Schedule

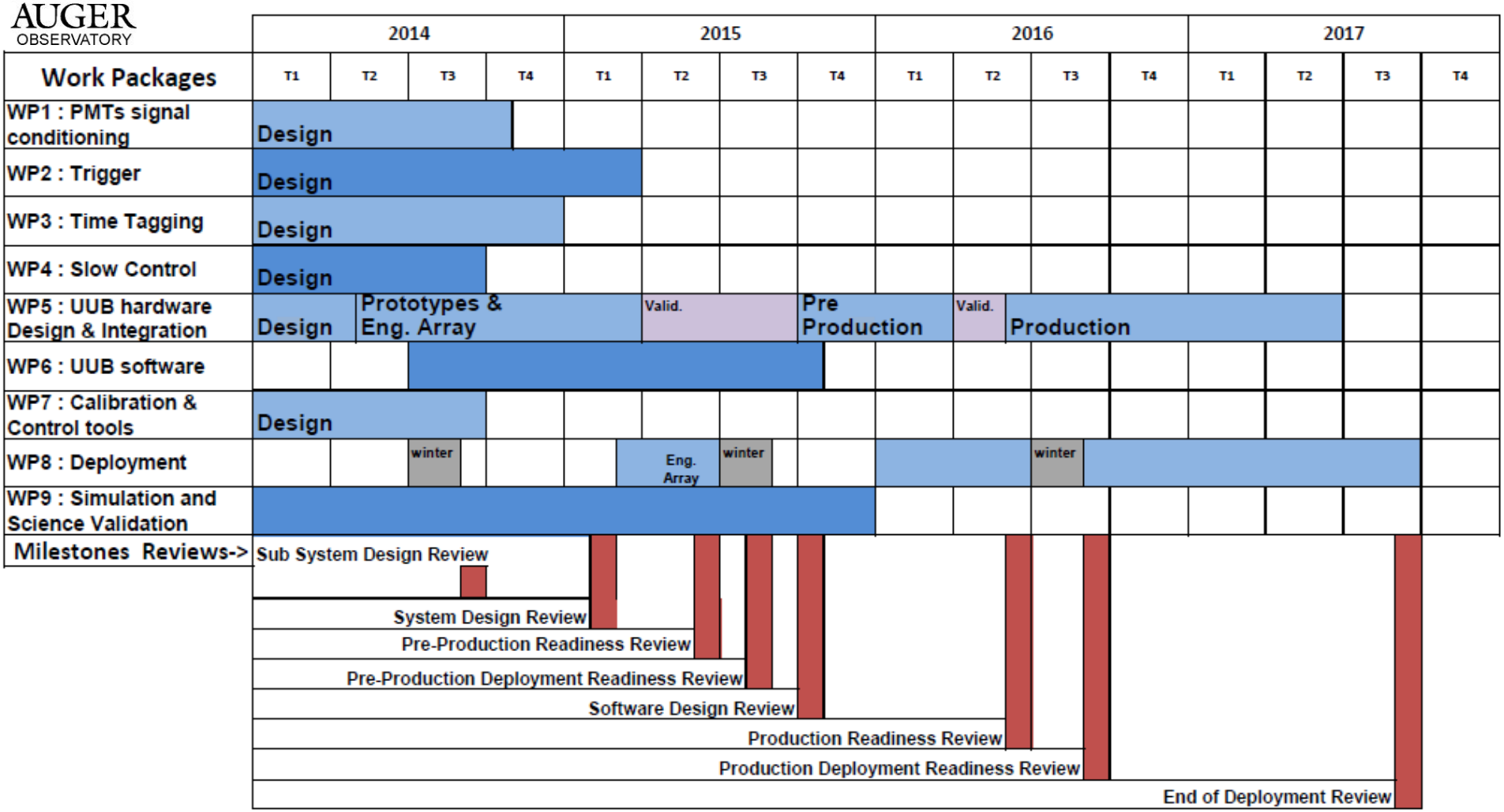
PIERRE AUGER OBSERVATORY

09/01/2015



# Schedule

PIERRE AUGER OBSERVATORY



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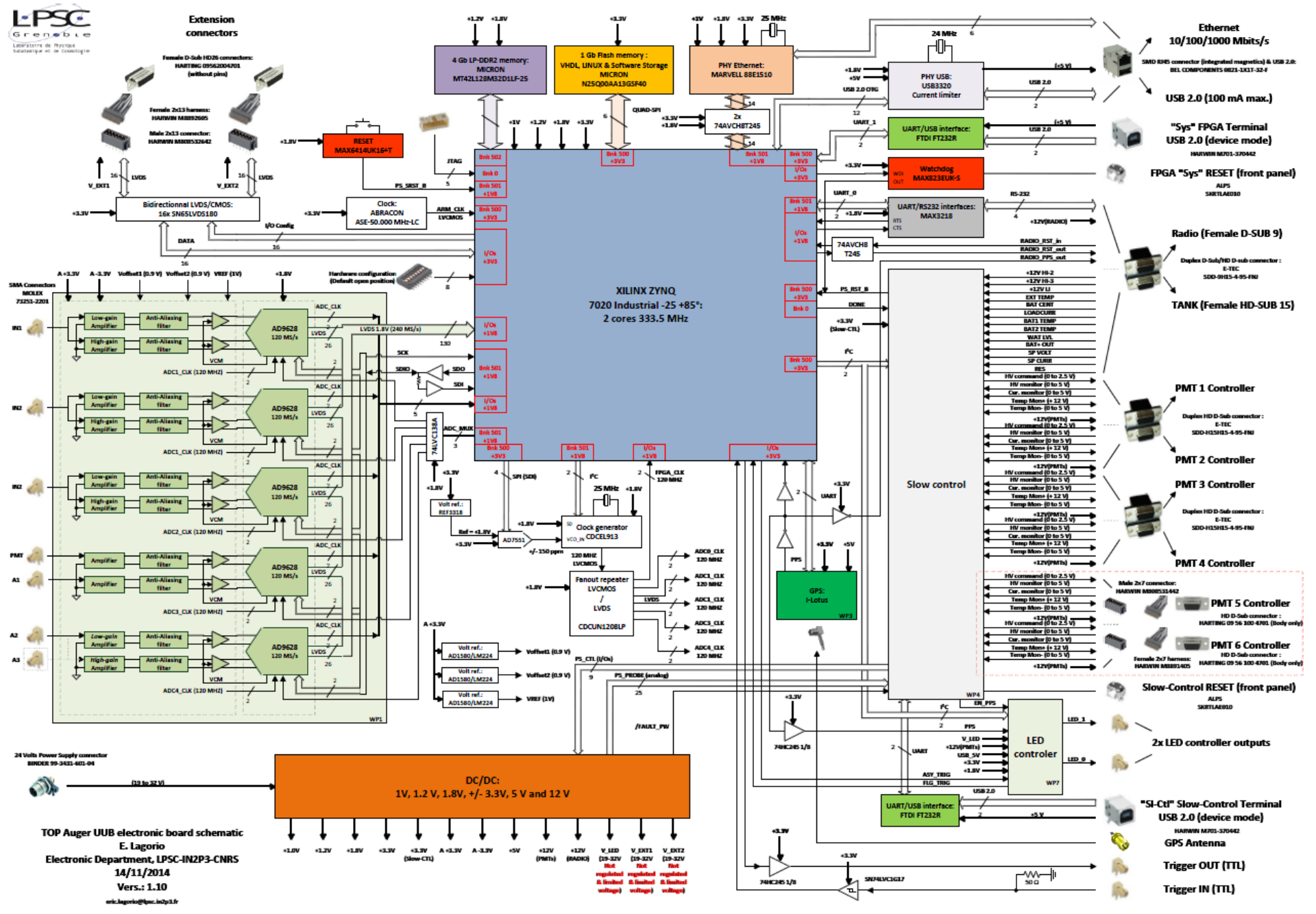
# Backup Slides

# Upgraded Unified Board UUB

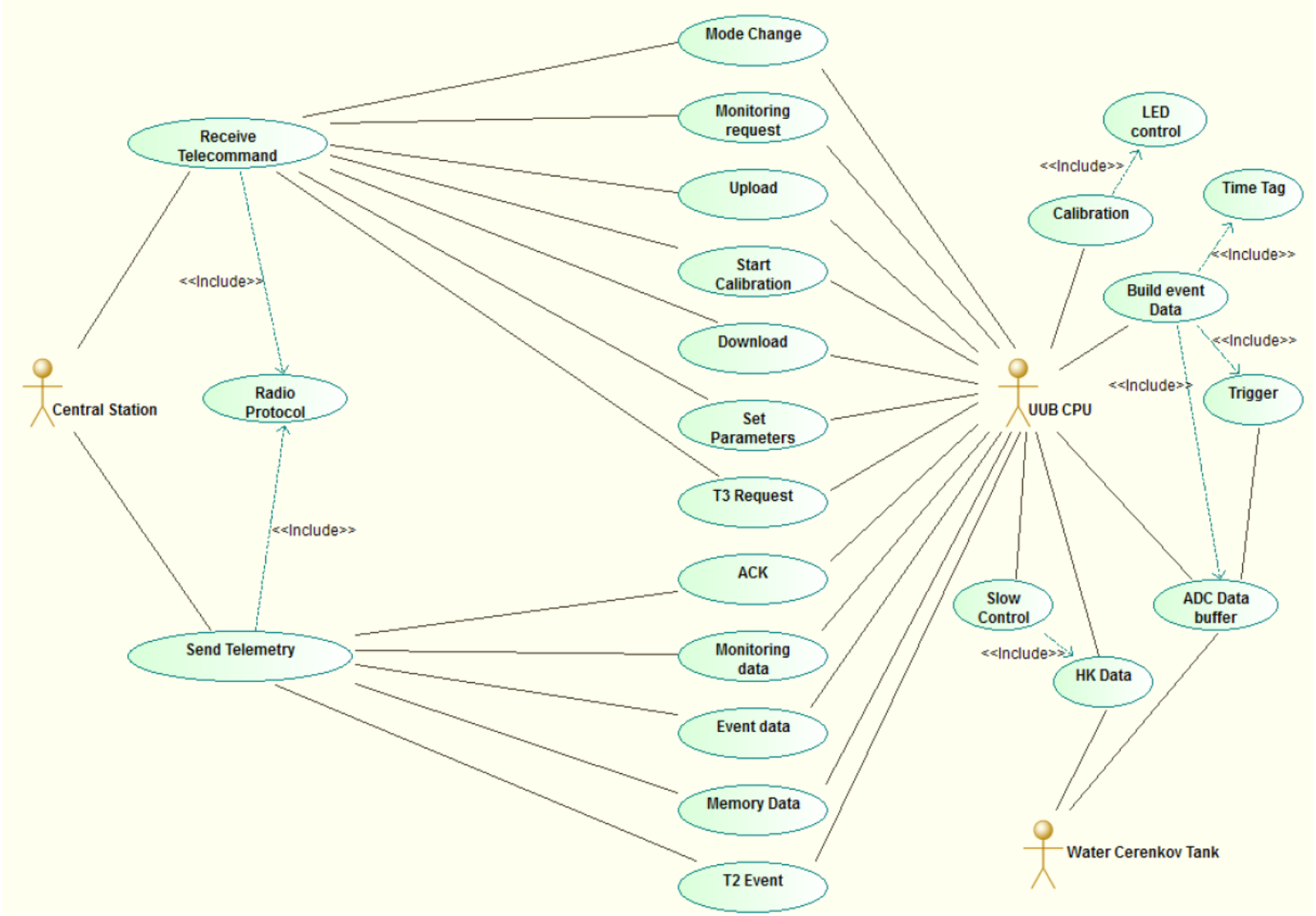


# Software and data transmission

The existing Auger-UB software will be ported to Linux.
The software will involve greater use of FPGA firmware to simplify data acquisition.

The 900MHz COMMS transmission is 150 bytes/s/station.
The bandwidth is divided into 50% T2 (3 bytes), 40% T3 (events, 7 kbytes) and 10% fixed overhead.
It is best to keep readout rate < 0.1 per station per min, the readout time is currently about 2min.
The estimated increase of the event size for Auger upgrade is about 5.
Possible solution:
Decrease T2 rate from 20 to 10Hz (will not affect shower triggers ToT etc.).
Would require slightly higher threshold trigger, but could be compensated for horizontal showers by a smarter trigger.
Event compression currently uses « Zip » algorithm.
Better algorithms (Fobbonazi compression etc.) produce compressed sizes
between 1/2 and 2/3 of « Zip ».
Intelligent suppression of low gain channels can reduce size about a factor of 2 for the 3 PMTs.
Total relative effective decrease is therefore a factor 4-5 and compensates the increase of event size.

# Software: Use Case diagram



# Software: Operating Modes diagram