Pierre Auger Observatory

Surface Detector Electronics Upgrade
List of ECR

Abstract:
This document is the list of the UUB ECR defined before, during and after the AE set up.

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Table of Content

ACRONYMS

ADC	Analog to Digital Converter
BGA	Ball Grid Array
BSRU	Base Station Radio Unit
CR	Configurational Requirement
DAC	Digital to Analog Converter
DC	Direct Current
EA	Engineering Array
EAS	Extensive Air Shower
ECR	Engineering Change Request
ER	Environmental Requirement
FDIR	Failure Detection, Isolation and Recovery
FPGA	Field Programmable Gate Array
FR	Functional Requirements
Fs	Full scale
GPS	Global Positioning System
ICD	Interfaces Control Document
IR	Interface Requirements
LED	Light Emitting Diode
LSB	Low Significant Bit
LVDS	Low Voltage Differential Signaling
Msp/s	Mega samples per second
n/a	non applicable
OR	Operational Requirements
OS	Operating System
PAO	Pierre Auger Observatory
PBS	Product Breakdown Structure
PCB	Printed Circuit Board
PMT	PhotoMultiplier Tube
PR	Physical Requirements
QR	Quality Requirements
RD	Reference Document
RDA	Research and Development Array
RF	Radio Frequency
RMS	Root Mean Square
SD	Surface Detector
SDE	Surface Detector Electronics
SDEU	Surface Detector Electronics Upgrade
SR	Support Requirements
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TPCB	Tank Power Control Board
UB	Unified Board
UC	Upgrade Committee
USB	Universal Serial Bus
USB OTG	USB On-The-Go
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VM	Verification Matrix
WBS	Work Breakdown Structure
WP	Work Package

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
19	A	25/11/16	P. Stassi	1st DRAFT for approbation
19	B	29/11/16	P. Stassi	ECRs added after WPs feed backs. All ECRs need to be discussed and accepted before next revision.
19	C	09/12/16	SDEU Team	Updated during the 8-9/12 Orsay meeting
19	D	12/12/16	P. Stassi	More details added, annex added.
19	E	16/12/16	SDEU Team	SDEU team feed backs on previous revision

1 INTRODUCTION

The document defines the complete list of the UUB ECR, decided in February 2016 for the pre-prototypes implemented in the EA. Additionally, since October 2016, new ECR has been raised, learned from the EA experience. These ECR are also reported in the list.

The status of all the UUB ECR is defined in the list, their acceptation and their implementation for the next production phase.

1.1. Reference Documents

RD1 UUB Pre prototype cabling Report, WP05-LPSC-20D – ATR 120770

2. ECR FROM 26FEB 2016 – ALL ACCEPTED

#	WP1 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
1.1	Replace type 3 FE design by Type 1 or 2 (2 last channels)	- Simplification and SSD adaptation	YES	☒ YES ☐ NO	☒ YES ☐ NO
1.2	Low gain on type 1 FE design at -12 dB	- SSD PMT adaptation	YES	☒ YES ☐ NO	☒ YES ☐ NO
1.3	Gain optimization on 3 last ADC chan. (on type 1 & 2, 3 boards only) ***Replaced by the ECR 11.6***	- Adaptation to SiPM	YES	☒ YES ☐ NO for 2 boards	☒ YES ☐ NO
1.4	Remove zero resistors as jumper to exclude external VREF on ADCs (use of ADC ref) ***Replaced by the ECR 11.8***	- To allow more measurements	YES	☒ YES ☐ NO	☒ YES ☐ NO
~~**1.5**~~	~~Siegen solution for enable of - 3.3 V problem~~ ***Canceled by the ECR 15.1***	~~- NCR~~	~~YES~~	~~☒ YES ☐ NO~~	~~☐ YES ☐ NO~~
1.6	Add tantalum capacitors on offset output	- Stabilization & filtering - Noise reduction	YES	☒ YES ☐ NO	☒ YES ☐ NO
1.7	Use precision & quality resistors for offset and VREF generators ***See the ECR 11.8***	- Optimization - Noise reduction	YES	☐ YES ☒ NO	☐ YES ☒ NO

#	WP1 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
1.8	Passive components final values on filter and amplifiers and capacitors position	- Optimization - Noise reduction and - NCR	YES	☒ YES ☐ NO	☒ YES ☐ NO
1.9	Remove last SMA connector ***The decision is to keep it only on the layout***	- Design Simplification - Cost saving	YES Exc. SiPM	☐ YES ☒ NO	☐ YES ☒ NO

#	WP2 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
2.1	Remove the ADC overflow bits ***The decision is to not implement it because there is no need of the saved I/O***	- Useless and save 10 FPGA I/O	YES	☐ YES ☒ NO	☐ YES ☒ NO

#	WP4 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
4.1	Add 10uF capacitors filter on microcontroller Vref+	- Noise reduction on SC ADCs	YES	☒ YES ☐ NO	☒ YES ☐ NO
4.2	~~Change SC ADC impedances on PMT_TMon lines to 1 kΩ~~ ***Actually it is 10kΩ on old UB***	- ~~Conformance to old UB~~	YES	☒ YES ☐ NO	☐ YES ☒ NO
4.3	3.3 to 1.8V conversion for microcontroller NMI-FPGA line ***The H/W solution is more safe than the S/W one, more inputs needed here.***	- Safety. Can be done by S/W (microcontroller configuration)	YES	☐ YES ☒ NO	☐ YES ☐ NO
4.4	Connect microcontroller PS_SRST_B line to 3.3V	- Non conformance	YES	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
5.1	Ethernet LED connections to be changed	- NCR	YES	☐ YES ☒ NO	☒ YES ☐ NO
5.2	Radio reset routed to micro-controller ***See the ECRs 14.4, 14.9 & 14.10***	- Design consistency - Safety of operation	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.3	Replace Jitter cleaner with fan-out and new VXO to go to 1ps jitter, 3.3V on DAC	- Save power (Layout modifications mandatory)	YES	☐ YES ☒ NO	☒ YES ☐ NO
	The jitter on ADC clock is estimated to 100 fs (RMS) with the Jitter-Cleaner and 300 fs with a fan out circuit which is fully acceptable from the point of view ADC resolution degradation and SNR. The power consumption decrease from 700 to 252 mW per UUB. There is no initial configuration required. (see Annex)				
5.4	Replace QSPI flash memory with faster one ***See ECR 15.31***	- Speed of upload	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.5	Remove LVDS buffers on EXT I/O and on board connectors. ***See ECR 15.5***	- Save power	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.6	Replace Power supply connector with ref: BINDER 86 0531 1121 00004	- Robustness - Simplification (only one piece)	YES	☐ YES ☒ NO	☒ YES ☐ NO
	This connector is much more robust, especially when it is tight hard during the mounting phase, putting less mechanical constraints on the plastic part. There is only one part, soldered on the PCB, reducing the risk of losing part (barrel) during integration. There is no risk of shift of the front panel due to thermal stress because the panel is hard tight with the SMA screws. (see annex)				

#	WP5 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
5.7	Modify bad footprints found on the prototype design	- NCR	YES	☐ YES ☒ NO	☒ YES ☐ NO
5.8	Use adapted size stencil sheet for PCB ***This is not an ECR but a fabrication specification for the manufacturer***	- NCR	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.9	Update the BOM ***Obvious action for the new design***	- Production Simplification	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.10	Additional ground plane on top and bottom of the PCB	- Reduce conducted noise	YES	☐ YES ☒ NO	☒ YES ☐ NO
	This **not** mean adding new layers on the PCB but only filling the blank area on the top and bottom layers with copper connected to GND. This was foreseen form the beginning in the layout design but discarded for the prototypes to ease test and adjustment work on the PCB during prototype phase.				
5.11	Change holes position on PCB ***No need to keep the historical positions of the holes on the PCB, used only for holding during test phase***	- Layout simplification	YES	☐ YES ☒ NO	☒ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
5.12	Remove stiffener	- Useless excepted for horizontal transportation	YES	☒ YES ☐ NO	☐ YES ☒ NO
	The decision is to keep the stiffener in aluminum (other material can also be tested, like FR4) at the back position, with standard circular holes and screws in the middle and slots and screws on the edges, to release the mechanical stress on the PCB during thermal deformation. ***See ECR 15.23***				
5.13	DC/DC ramp capacitor value optimization	- Faster start up	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.14	Design correction on USB PHY component	- NCR	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.15	Correction on clock DAC voltage	- NCR	YES	☒ YES ☐ NO	☒ YES ☐ NO
5.16	Optimized ADCs SDIO Configuration ***Allow a safe configuration of the ADCs at power up. (see annex)***	- Optimization and safety	YES	☐ YES ☒ NO	☒ YES ☐ NO
5.17	Optimize passive components values and sizes (for production) ***See ECR 15.14***	- Manufacturing simplification - QA	YES	☐ YES ☒ NO	☒ YES ☐ NO
5.18	Replace through-hole connectors by SMT models (for production) for J4, J5, J7 & J9	- Manufacturing simplification - QA	YES	☐ YES ☒ NO	☐ YES ☒ NO
	These connectors got hard mechanical constraints due to flat cables attached on it. The through-hole version is more robust and can be equipped with metallic or plastic locks to maintain the flat cable. More over the SMT model require the usage of glue to maintain it on the PCB during fabrication representing an additional work from the manufacturer.				

#	WP7 Modification	Motivation	Accepted ?	Implemented on the EA ? (retrofit)	To be implemented on the new design ?
7.1	LED controller logic integration into FPGA firmware.	- Save power & components	YES	☒ YES ☐ NO	☒ YES ☐ NO

2. ECR DEFINED FOR RETROFIT (FOR RECORD ONLY, CAN BE REDUNDANT WITH THE ABOVE LIST)

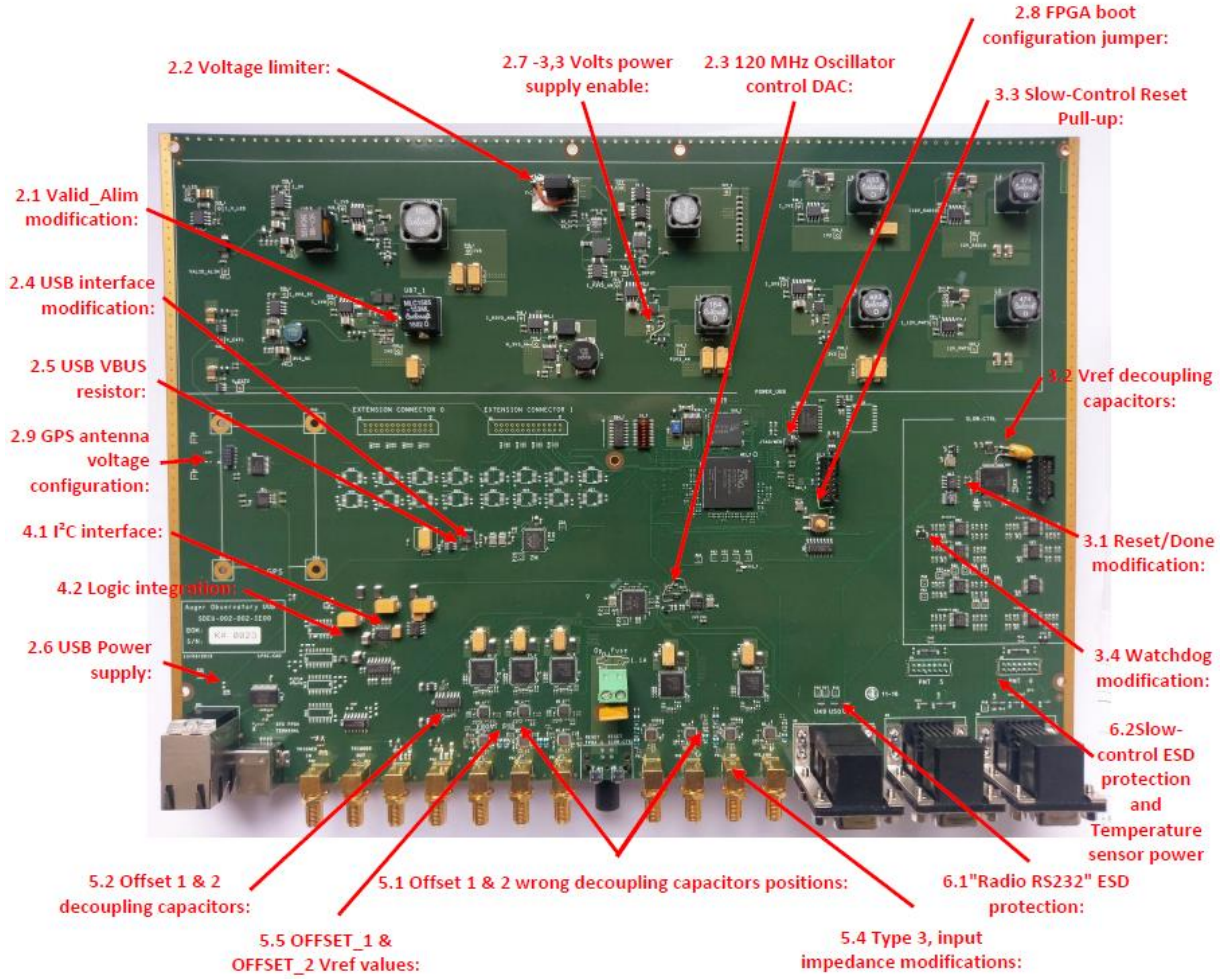
This ECR list is established in reference of the Retrofit document (RD1).

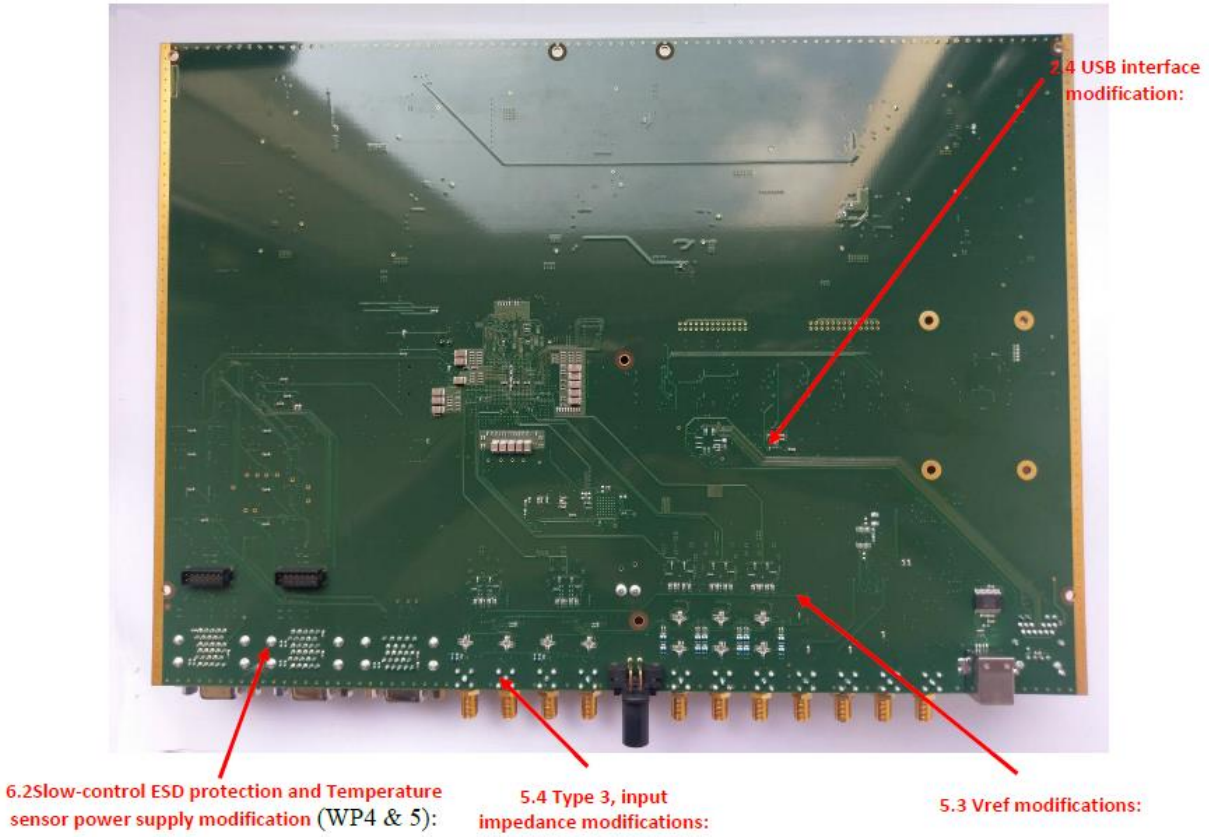
#	WP1 Retrofit Modification	Motivation	Accepted ?	To be implemented on the new design ?
R1.1	Offset 1 & 2, decoupling & capacitors positions: - Move C5_1, C8_1, C5_2, C8_2, C5_3, C8_3, C5_4, C8_4, C5_5 & C8_5 capacitors to be connected on Offset In signal (see schematics). - Add 4 Tantalum or ceramic decoupling capacitors on each OFFSET signal. 2 on amplifier Offset outputs. The 2 others must be close the ADCs.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R1.2	Vref: - Disconnect output of M1 amplifier	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R1.3	input impedance: - Add 91 and 200 Ohms resistor on PX1_1	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R1.4	OFFSET_1 & OFFSET_2 Vref values: The Reference Voltage value must be changed. R91 resistor value must be 2,4 kOhms and R92 1,3 kOhms in 0402 1%	- NCR	☒ YES ☐ NO	☒ YES ☐ NO

#	WP4 Retrofit Modification	Motivation	Accepted ?	To be implemented on the new design ?
R4.1	Reset/Done: - Add 4.7kOhms resistor between 3V3_SLOW_CTRL and U20 pin 23	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R4.2	Vref decoupling capacitors: - Add a 10 µF 25 Volts and 100nF capacitors in parallel to U20 pin 7 and C138	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R4.3	Slow-Control Reset Pull-up: - Connect R297_7 resistor pull up pin to 3.3 Volts power supply.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R4.4	Watchdog: - Add a 10 kOhms resistor between pins 1 and 5 of M34.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R4.5	LED logic integration: A short-cut must be made between M14 pins 2 and 3.	- LED logic integration	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Retrofit Modification	Motivation	Accepted ?	To be implemented on the new design ?
R5.1	Valid_Alim modification: - Remove R100_1 - Add 1.5kOhms resistor on U86_1	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.2	Voltage limiter: - Modify the foot print of the Q4_1 transistor	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.3	120 MHz Oscillator control DAC: - Connect DAC7551 IOVDD to 3.3 Volt (1,8 volt previously) power supply. - Connect pull-up resistors R382, R383, R384, R385 & R386 to 3.3 Volt.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.4	USB interface: - Connect U36 pin 20 to U36 pin 23. - Connect U36 pin 23 to 3.3 Volts.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.5	USB VBUS resistor: The VBUS R343 resistor value is wrong in the Bill Of Material. It must be 1 kOhms	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.6	USB power supply: The FE5 coil has been forgotten. A 0 Ohm resistor or a short-cut should be added.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Retrofit Modification	Motivation	Accepted ?	To be implemented on the new design ?
R5.7	-3,3 Volts power supply enable: - Connect the +/- 3.3 Volts Enable from the Slow-Control micro-controller (3,3Volts) to U97_1 +3.3V DC/DC pin15 (EN) and U18_1 -3.3V DC/DC pin 15 (/SHDN). The +3.3V DC/DC output will enable the -3.3V DC/DC enable. - Add two 10kOhms resistor	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.8	FPGA boot configuration jumper: The boot configuration jumper (S2_7) has been forgotten in the BOM. It must be added.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.9	GPS antenna voltage configuration: The GPS antenna could be powered by 2 types of voltages, 3 Volts or 5 Volts. On the board this choice is made by R1 and R2, 0 Ohm resistors. Presently, the 2 resistors are soldered on board, R2 resistor must be removed.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
R5.10	I²C interface: - Swap SCL & SDA pins on AD5316 (M11, pins 2 & 3).	- NCR	☒ YES ☐ NO	☒ YES ☐ NO


2.8 FPGA boot configuration jumper:
2.2 Voltage limiter:
2.7 -3,3 Volts power supply enable:
2.3 120 MHz Oscillator control DAC:
3.3 Slow-Control Reset Pull-up:
2.1 Valid_Alim modification:
2.4 USB interface modification:
2.5 USB VBUS resistor:
3.2 Vref decoupling capacitors:
2.9 GPS antenna voltage configuration:
4.1 I²C interface:
3.1 Reset/Done modification:
4.2 Logic integration:
2.6 USB Power supply:
3.4 Watchdog modification:
6.2Slow-control ESD protection and Temperature sensor power
5.2 Offset 1 & 2 decoupling capacitors:
5.1 Offset 1 & 2 wrong decoupling capacitors positions:
6.1"Radio RS232" ESD protection:
5.5 OFFSET_1 & OFFSET_2 Vref values:
5.4 Type 3, input impedance modifications:


2.4 USB interface modification:
6.2Slow-control ESD protection and Temperature sensor power supply modification (WP4 & 5):
5.4 Type 3, input impedance modifications:
5.3 Vref modifications:

3. ECR DEFINED FROM EA SETUP ACTIVITIES

#	WP1 Modification	Motivation	Accepted ?	To be implemented on the new design ?
11.1	Add LC filters on analog amplifiers power supplies (Front End)	- Reduce conducted noise	☒ YES ☐ NO	☒ YES ☐ NO
	As it has been done on the design of the old Front End, LC filters with high level of rejection should be added closely to the chips, on the power supplies lines of the Front End amplifiers, calculated to take into account the switching frequency of the DC/DC converters.			
11.2	Modify decoupling capacitors value on filter outputs. Value = 470 nF or 1 uF	- Suppress excessive undershoot on PMT signals	☒ YES ☐ NO	☒ YES ☐ NO
	Three capacitors values are under test in the EA: 100 nF (original value) 470 nF and 1000 nF. The tests are already conclusive at a first approach with the 470 nF value. If some reason leads to modify this value, it can be done even after fabrication.			
11.3	Modify offset circuit and resistor values on front end inputs channels.	- Optimization	☒ YES ☐ NO	☒ YES ☐ NO
11.4	Layout modification on analog channels	- Reduce channels cross talk under saturation.	☒ YES ☐ NO	☒ YES ☐ NO
11.5	Filter layout modification	- Reduce inductive cross talk between high gain and low gain next channel.	☒ YES ☐ NO	☒ YES ☐ NO
	The filters inductors of each high gain channels are placed too much close to the ones of the next channel low gain. This will generate inductive cross talk between channels. These components should be placed at a bigger distance from each other or on other side of the PCB alternatively. (see annex).			

#	WP1 Modification	Motivation	Accepted ?	To be implemented on the new design ?
11.6	Design a unique layout solution valid for both SSD PMT and SiPM on the SSD channels	- Design simplification	☒ YES ☐ NO	☒ YES ☐ NO
	A unique layout configuration can be design, valid for both SiPM and standard PMT on the SSD channels. This assuming that the signal split between high and low gain for the SiPM is made inside the UUB front end circuitry like it is made for the SSD PMT. The same layout PCB can be used for both solution, only the resistors values determining the gain and the offset need to be adjusted to adapt the design to SiPM or standard PMT.			
11.7	Offset adjustment by S/W ***Rejected due to the risk of unwanted modification***	- To compensate the variation of the tolerance of the resistor values	☐ YES ☒ NO	☐ YES ☒ NO
11.8	Using individual internal references for each ADC rather than tying all ADCs to a single reference. ***Some tests will be conducted before integration to the next design***	- To avoid a possible single point failure	☒ YES ☐ NO	☐ YES ☐ NO
	It does not guarantee that all the ADC references are identical but there is no physics reason why this is essential since this difference would be absorbed into the MIP calibration. Note that low gain and high gain channels would share a common reference for each pair of channels since there is one reference per dual ADC. The specification gives the range of internal reference voltages as ± 2% which I don't think presents a problem			

#	WP2-WP6 Modification	Motivation	Accepted ?	To be implemented on the new design ?
12.1	Optimization of the Firmware	- Decrease power consumption	☒ YES ☐ NO	☒ YES ☐ NO
12.2	Change the flash memory mapping (see annex)	- Optimization - Maintenance simplification	☒ YES ☐ NO	☒ YES ☐ NO
12.3	Extend Muon buffer length	- To add more bins before the SSD signal	☒ YES ☐ NO	☒ YES ☐ NO
12.4	Include internal self-test program in the F/W	- Maintenance and tests simplification	☒ YES ☐ NO	☒ YES ☐ NO
12.5	Implement new patching procedure for S/W (see annex)	- Optimization - Maintenance simplification	☒ YES ☐ NO	☒ YES ☐ NO

All these 12.n ECRs had no impact on the hardware design.

#	WP4 Modification	Motivation	Accepted ?	To be implemented on the new design ?
14.1	Reverse resistor bridge and values for -3.3V value reading	- NCR, error in schematics	☒ YES ☐ NO	☒ YES ☐ NO
14.2	Replace on board temperature sensor BMP 180 with ref: BME280 (with additional humidity sensor) This require S/W modification. (see annex)	- Component obsolete	☒ YES ☐ NO	☒ YES ☐ NO
14.3	Remove ESD protection on temperature sensor inputs, U11, U12, U13. ***The ESD protection is kept, the transfer function and/or the resistive bridge is adjusted.***	- NCR	☐ YES ☒ NO	☐ YES ☒ NO
14.4	Change Watchdog logic (H/W and/or S/W) **See 5.2, 14.8, 14.9**	NCR	☒ YES ☐ NO	☒ YES ☐ NO
	There is proposition (from WP1, WP4 and WP5) to re design the Watchdog and reset circuitry learning from the results of the EA. This conduct to integrate part of the logic into the FPGA firmware. A merged and optimized solution should be proposed to be implemented for the next design. (see annex)			
14.5	Change values of R173 and R178 resistors from 8k2 Ohms to 820 Ohms	NCR	☒ YES ☐ NO	☒ YES ☐ NO
14.6	Change values of R194 and R199 resistors from 2k ohms to 200 Ohms	NCR	☒ YES ☐ NO	☒ YES ☐ NO

#	WP4 Modification	Motivation	Accepted ?	To be implemented on the new design ?
14.7	Use reference voltage (1V) for the SC ADC	- Increase SC measurements accuracy	☒ YES ☐ NO	☒ YES ☐ NO
	This will be realized by an additional voltage reference component: TBD			
14.8	Add Failure Detection (FDIR) actions related to Power management into the SC software.	- Battery protection	☒ YES ☐ NO	☒ YES ☐ NO
	The idea is to detect the batteries lower voltage limit form the Slow Control voltage measurement and to raise an alarm toward the Monitoring and then take the action of switching off all the powers supplies (SC excepted). Same mechanism can be applied in case of over-voltage. (see annex)			
14.9	Modify S/W for FPGA reset **See ECR 14.4**	- Design consistency	☒ YES ☐ NO	☒ YES ☐ NO
14.10	Reverse the logic of the UUB radio reset to be compatible with the Radio Unit.	- Design consistency, NCR	☒ YES ☐ NO	☒ YES ☐ NO
14.11	Modify resistors bridge values for the large PMTs temperature sensors reading	- Design consistency	☒ YES ☐ NO	☒ YES ☐ NO
14.12	Fix battery voltage measurement discrepancy (-3.3V reading error). ***R240, 241 & 242 values modified***	- NCR	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	To be implemented on the new design ?
15.1	Replace -3,3V LT3431 DC/DC converter ***Replaced with ref: LT3704with no charge pump technology: less noisy (see annex)***	- ECR #1.5 (-3.3V enable, NCR 2-40) - Conducted noise reduction	☒ YES ☐ NO	☒ YES ☐ NO
15.2	Modify RAM layout ***See ECR 15.19***	- NCR on decoupling capacitors - Conducted noise reduction	☒ YES ☐ NO	☒ YES ☐ NO
15.3	Add GND ring on analog channels on layout ***On each channel if possible or each ADC***	- Conducted noise reduction	☒ YES ☐ NO	☒ YES ☐ NO
15.4	Optimize all DC/DC converter layout and grounding. (see annex)	- Layout NCR - Conducted noise reduction	☒ YES ☐ NO	☒ YES ☐ NO
15.5	Remove one of the two digital extension interface blocs ***Decision is to keep it on the layout***	- Useless	☐ YES ☒ NO	☐ YES ☒ NO
15.6	Remove PMT6 slow control connector ***Decision is to keep it on the layout***	- Useless	☐ YES ☒ NO	☐ YES ☒ NO
15.7	Change reference of PMT5 & 6 and EXT 1 &2 connectors and cables (loose parts)	- Robustness	☒ YES ☐ NO	☒ YES ☐ NO
	Learning from the EA integration experience, the EXT1 and 2, PMT5 et 6 extension cables (from the board to the front panel) defined in the loose parts specification document, are very weak regarding the mechanical constraints with a big risk of unwanted disconnection or break. New references, more robust, are under study for direct replacement.			

#	WP5 Modification	Motivation	Accepted ?	To be implemented on the new design ?
15.8	Change Slow Control JTAG connector to 2x7 2.54 mm.	- SC Probe compatibility - Suppress the small connector adaptor PCB	☒ YES ☐ NO	☒ YES ☐ NO
15.9	Remove BP1_7 FPGA reset switch on front panel and on board also ***Not used by anyone***	- Useless	☒ YES ☐ NO	☒ YES ☐ NO
15.10	~~Replace FPGA &~~ Slow Control reset switch with the ref: C&K KT11B1SAM34LFS ***Destroyed by the PCB washing process in the previous fabrication***	- Robustness (IP58) - NCR	☒ YES ☐ NO	☒ YES ☐ NO
15.12	Move position of the main power connector (and fuse) on the right side of the board (from the front view of the front panel) ***Compliant with the existing cable length. (see annex)***	- Reduce conducted noise from outside (shorter cable) and inside (power wires far from analog area)	☒ YES ☐ NO	☒ YES ☐ NO
15.13	Move Slow Control layout bloc far from the edge of the PCB ***Few mm displacement, no big impact on layout***	- Reduce risk of components damage during integration	☒ YES ☐ NO	☒ YES ☐ NO
15.14	Use 0402 packages type only for passive components on the ADCs and FPGA blocs layouts (see ECR #5.17)	- Simplification	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	To be implemented on the new design ?
15.15	Replace S1_7, 8 x multi-switches with a new reference (TBD). ***Keep 8 channels. Foot print can be***	- Problem of procurement - Design simplification	☒ YES ☐ NO	☒ YES ☐ NO
15.16	Rotate position of 180 deg. of screw connector B1_1 (fuse connection)	- NCR - Integration simplification	☒ YES ☐ NO	☒ YES ☐ NO
15.17	Replace 12V DC/DC converter for big PMT bases and Radio power supplies	- NCR, reduce failure propagation on 12V	☒ YES ☐ NO	☒ YES ☐ NO
	The LMR24220 component does not have output short-cut protection (NCR n°2-59). Changed by TPS54A20, but the estimated efficiency is only 80% (instead of 90%).			
15.18	Replace all tantalum capacitors with ceramic ones.	- Reduce intrinsic noise - Reduce blast risks	☒ YES ☐ NO	☒ YES ☐ NO
15.19	Replace U32_7 2 Gbits LP-DDR RAM	- Component obsolete	☒ YES ☐ NO	☒ YES ☐ NO
	This component is obsolete since Dec. 21, 2016. Replacement can be made with the reference: EDB4432BBPA-1D-F-R (Micron) but this component is not pin to pin compliant and it is not (yet) certified by Xilinx. ECR is accepted but some test must be made.			
15.20	Remove RS232 Comms ESD protection, U49 and U50. ***The MAX3218 RS232 interface has already an inside ESD protection.***	- NCR, useless	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	To be implemented on the new design ?
15.21	Reverse function of the S2_7 jumper to: open= normal mode	- Maintenance simplification	☒ YES ☐ NO	☒ YES ☐ NO
15.22	Replace Ethernet connector with PoE Ethernet connector.	- For Bullet radio	☐ YES ☒ NO	☐ YES ☒ NO
	This connector is a part of a combo connector gathering the ETH and the USB connections. This kind of combo connector does not exist with the PoE option. The mechanical configuration of the front panel does not allow other connectors than a combo. The usage an external bias-tee power supply is recommended where the Bullet radio are needed.			
15.23	Increase PCB thickness.	- Reduce mechanical constraints on PCB	☒ YES ☐ NO	☒ YES ☐ NO
	The present PCB thickness is 1.52 mm, due to layout constraints. It could be increased up to 1.8 mm at the maximum, if it is compliant with the constraints of the next layout. Note that the final PCB thickness is manufacturer dependent, related to the type of material used.			
15.24	Add buffers on RX/TX line for USB Slow Control connection. ***Also on the FPGA UART (see annex)***	- NCR - To solve start-up failures on the MSP430	☒ YES ☐ NO	☒ YES ☐ NO
15.25	Change Slow Control reset label position on PCB	- NCR, wrong position	☒ YES ☐ NO	☒ YES ☐ NO
15.26	To provide a new design for the dust cover of the ETH and USB front panel connectors. ***A slot must be foreseen on the USB connection in case of SiPM use. (see annex)***	- Present proposed design not implemented - No satisfying design available	☐ YES ☐ NO	☐ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	To be implemented on the new design ?
15.27	Replace 10 V DC/DC converter	- Reduce conducted noise	☐ YES ☒ NO	☐ YES ☒ NO
	The actual 10V DC/DC converter (LMR3150) has very good performances in terms of noise, efficiency, protection and transient response. The decision is to keep this component and to improve the layout for an optimized grounding, and the filtering with values more adapted to the UUB behavior than the data sheet standard configuration. (see annex)			
15.28	Add buffer on Trigger OUT signal to be able to drive 50 Ohms impedance.	- NCR	☒ YES ☐ NO	☒ YES ☐ NO
15.29	Increase low voltage switch off threshold value to 22 Volts (specs.) ***The H/W under voltage protection component is for electronics protection (DC/DC) and not for batteries protection. See ECR 14.8***	~~- Battery protection~~	☐ YES ☒ NO	☐ YES ☒ NO
15.30	Modify the pinout of the COMS connector allowing use a straight pin to pin cable for radio (loose parts).	- Design simplification, cost saving.	☒ YES ☐ NO	☒ YES ☐ NO
	The 9 pin to 9 pin connector cable used for the COMS is a pinout customized item, defined in the Loose parts specification document, due to the fact that the former cable cannot be re-used because of the too short length. The decision is to modify the pinout of the COMS connector on the UUB PCB, allowing using a standard straight pin to pin cable.			
15.31	Suppression of the second flash memory chip. **Decision is to keep it on the layout.**	- Design simplification, cost saving.	☒ YES ☐ NO	☒ YES ☐ NO

#	WP5 Modification	Motivation	Accepted ?	To be implemented on the new design ?
15.32	Add test point for power supplies verification	- Maintenance simplification	☒ YES ☐ NO	☒ YES ☐ NO
15.33	Add a Zener protection after a fuse on each power supply outputs as an additional overvoltage protection. ***The decision is to not implement this useless and too much noisy configuration***	~~- UUB protection~~	☐ YES ☒ NO	☐ YES ☒ NO
15.34	To provide a definition of the FPGA heat sink to allow commercial procurement.	- No definition on actual design	☒ YES ☐ NO	☒ YES ☐ NO
15.35	Request that the silkscreen be modified to include reference designator for all components	- Maintenance simplification	☒ YES ☐ NO	☒ YES ☐ NO
15.36	To find a way to identify easily SMA connectors on front panel ***The decision is to use colored or half tone labels***	- To avoid confusion and misconnecting on SMA connectors	☒ YES ☐ NO	☒ YES ☐ NO
15.37	Add electrical protection on the USB (not USB SYS) connector	- To protect the interface from incorrect connections or disconnections	☒ YES ☐ NO	☒ YES ☐ NO

2. ANNEX - VIEWGRAPHS

The following viewgraph add more information about some critical ECRs.

ECR (Feb 2016) not integrated for EA

ECR 5-3, Jitter Cleaner replacement by Fanout:

WHAT DO WE NEED: Acceptable SNR (noise) MUST BE define before the choice. MORE JITTER = MORE NOISE

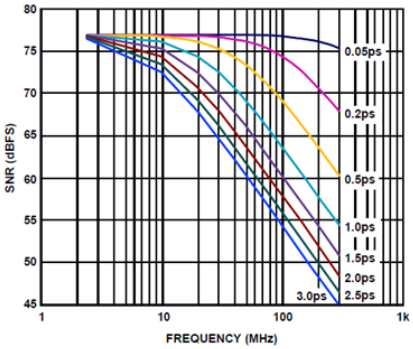
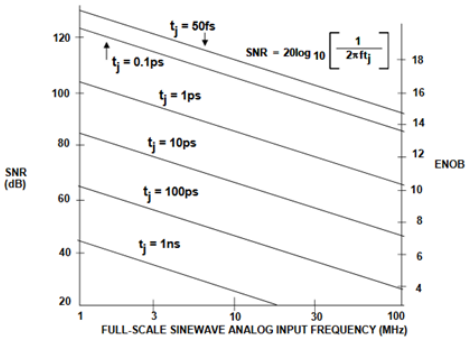


Figure 58. SNR vs. Input Frequency and Jitter

Analog Devices AD9628 datasheet rev. C



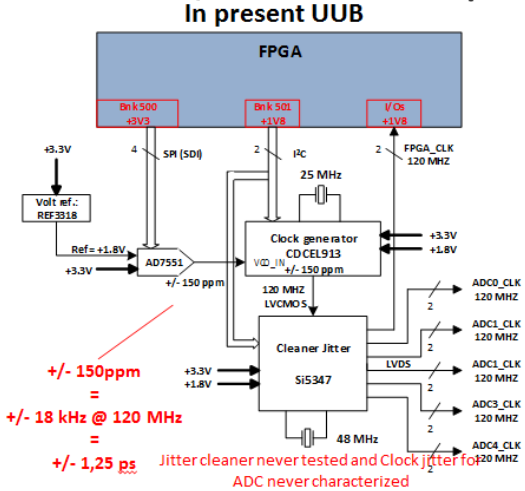
Lower power consumption OR Lower noise

To remove Jitter cleaner -> risk of increase of noise

ECR (Feb 2016) not integrated for EA

ECR 5-3, Jitter Cleaner replacement by Fanout:

In present UUB

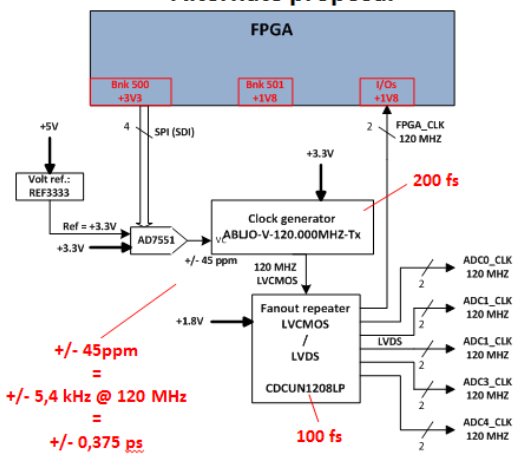


+/- 150ppm = +/- 18 kHz @ 120 MHz = +/- 1,25 ps

Jitter cleaner never tested and Clock jitter for ADC never characterized

Compliant with ADCs 100fs specs
Clocks Jitter Estimate : 0,1 ps Max
+/- 150 ppm frequency control (+/- 18 kHz)
Configurable
Power: 700mW

Alternate proposal



+/- 45ppm = +/- 5,4 kHz @ 120 MHz = +/- 0,375 ps

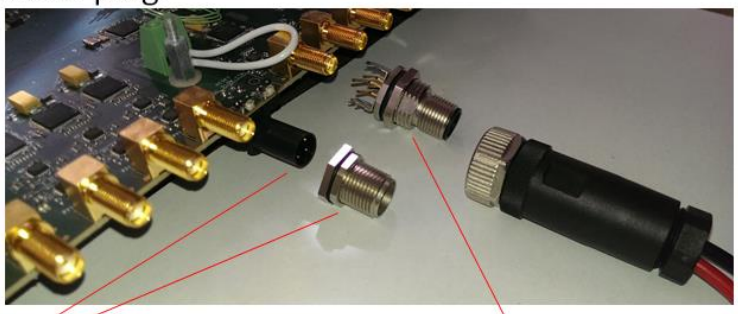
Outside ADCs specs.
Clocks Jitter estimate : 0,3 ps RMS
+/- 45 ppm frequency control (+/- 5,4 kHz)
No configuration
Power: 252 mW

ECR (Dec 2016)

ECR 5.6, Change Power supply connector:

only one part and more robust. Less mechanical constraints.

Same plug.



Present version: 2 parts

next version: 1 parts

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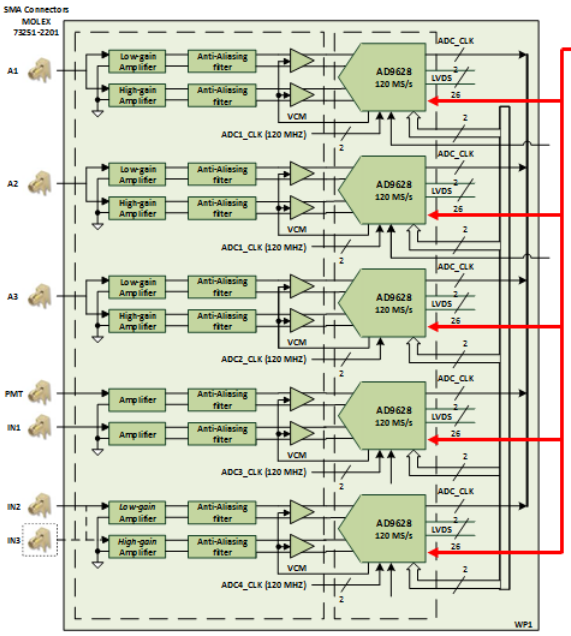
ECR (Feb 2016) not integrated for EA

ECR 5-16, Optimized ADCs SDIO configuration:



Power_down (1 FPGA pin)

ADCs power down enable from FPGA:

- ADCs initialization.
- Low power when UUB starts.
- Better component's life time.

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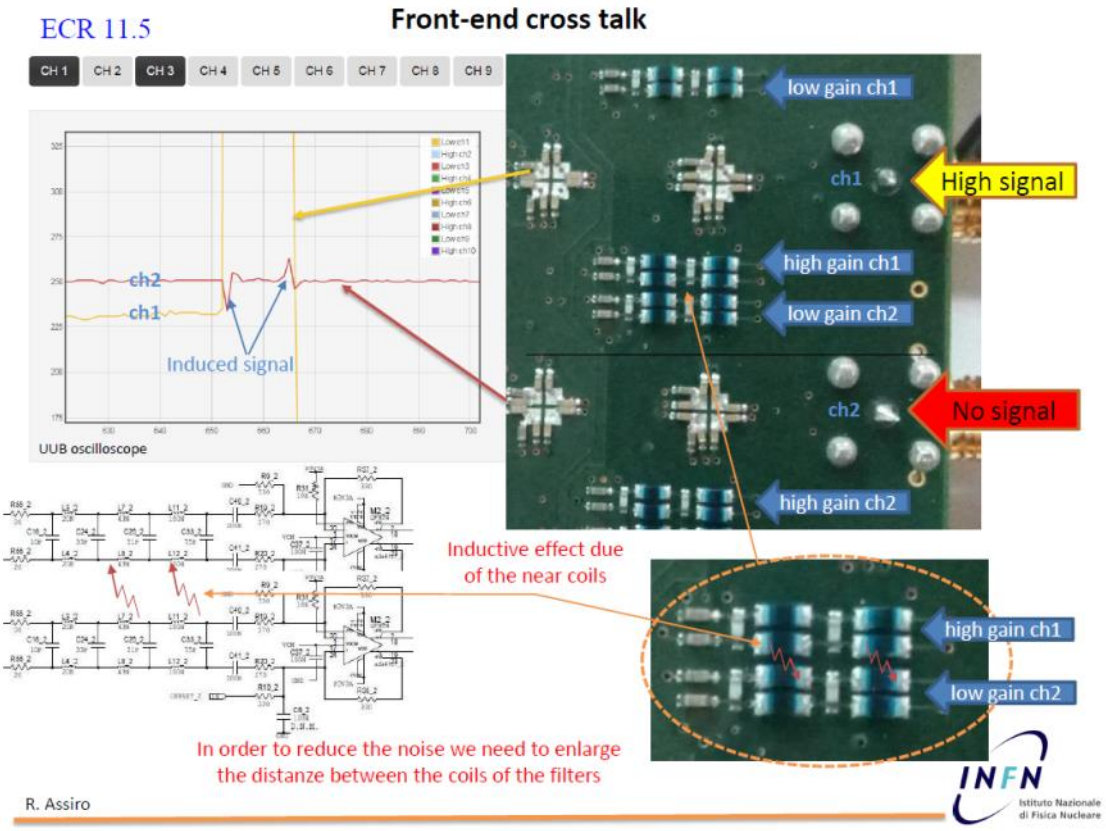
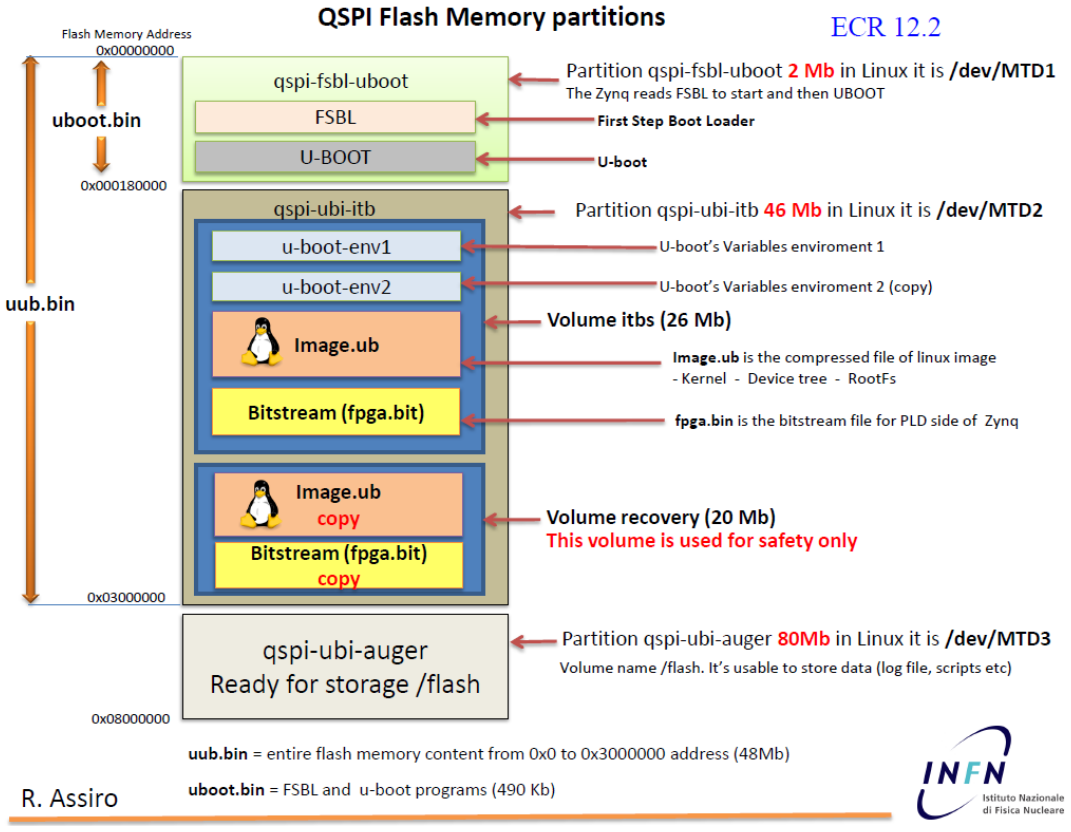

ECR 11.5
Front-end cross talk
CH 1
CH 2
CH 3
CH 4
CH 5
CH 6
CH 7
CH 8
CH 9
ch2
ch1
Induced signal
UUB oscilloscope
low gain ch1
ch1
High signal
high gain ch1
low gain ch2
ch2
No signal
high gain ch2
Inductive effect due
of the near coils
high gain ch1
low gain ch2
In order to reduce the noise we need to enlarge
the distanze between the coils of the filters
R. Assiro
INFN
Istituto Nazionale
di Fisica Nucleare


QSPI Flash Memory partitions
ECR 12.2
Flash Memory Address
0x00000000
uboot.bin
0x000180000
uub.bin
0x03000000
0x08000000
qspi-fsbl-uboot
FSBL
U-BOOT
Partition qspi-fsbl-uboot 2 Mb in Linux it is /dev/MTD1
The Zynq reads FSBL to start and then UBOOT
First Step Boot Loader
U-boot
qspi-ubi-itb
Partition qspi-ubi-itb 46 Mb in Linux it is /dev/MTD2
u-boot-env1
u-boot-env2
U-boot's Variables enviroment 1
U-boot's Variables enviroment 2 (copy)
Volume itbs (26 Mb)
Image.ub
Image.ub is the compressed file of linux image
- Kernel - Device tree - RootFs
Bitstream (fpga.bit)
fpga.bin is the bitstream file for PLD side of Zynq
Image.ub
copy
Bitstream (fpga.bit)
copy
Volume recovery (20 Mb)
This volume is used for safety only
qspi-ubi-auger
Ready for storage /flash
Partition qspi-ubi-auger 80Mb in Linux it is /dev/MTD3
Volume name /flash. It's usable to store data (log file, scripts etc)
uub.bin = entire flash memory content from 0x0 to 0x3000000 address (48Mb)
uboot.bin = FSBL and u-boot programs (490 Kb)
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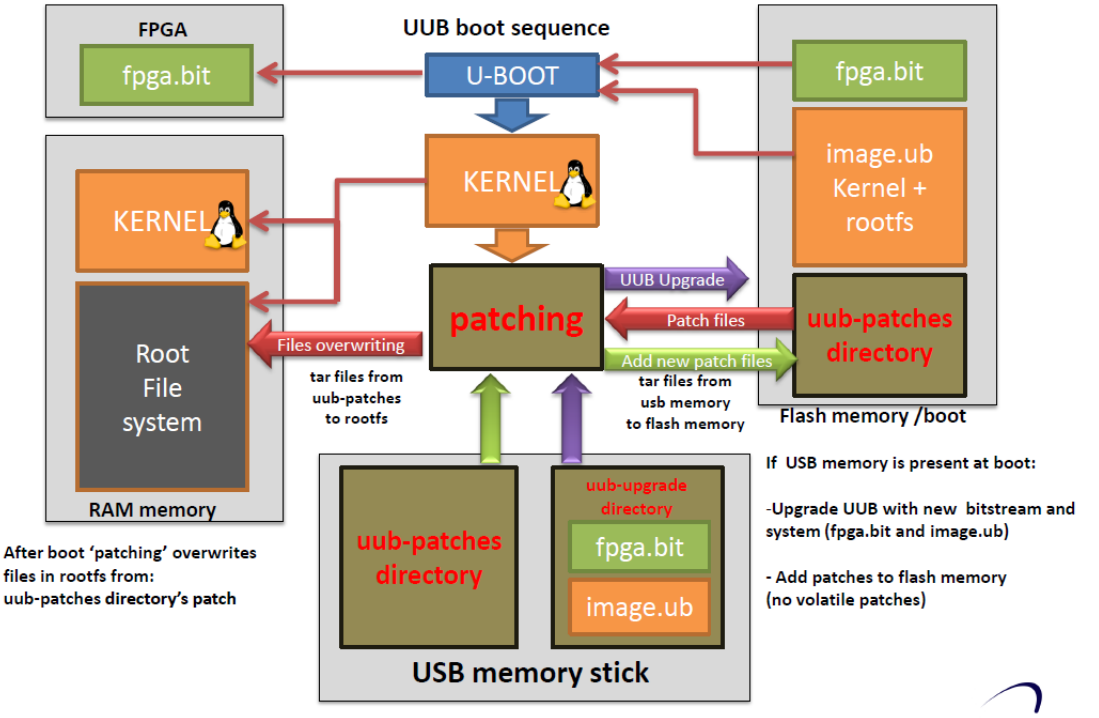
di Fisica Nucleare

ECR 12.5

How patching works



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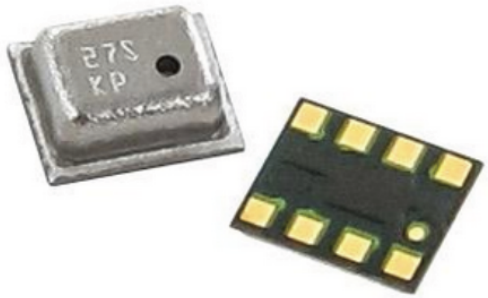
ECRs Slow Control (WP4) ECR 14.2

Pressure Sensor BMP180 discontinued

- BMP180 -> BMP280
- Different footprint
- Different Software
- Price 1.39 € @1000



Alternative BME280

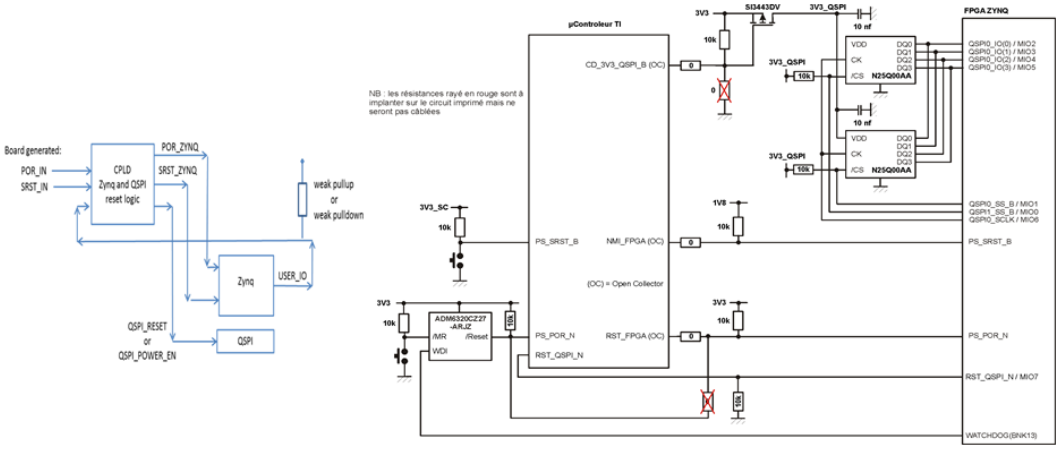
- Additional humidity Sensor
- Price 4.59 @ 1000

ECR (Dec 2016)

ECRs 14.4, 14.9 & 14.10, Resets specifications:

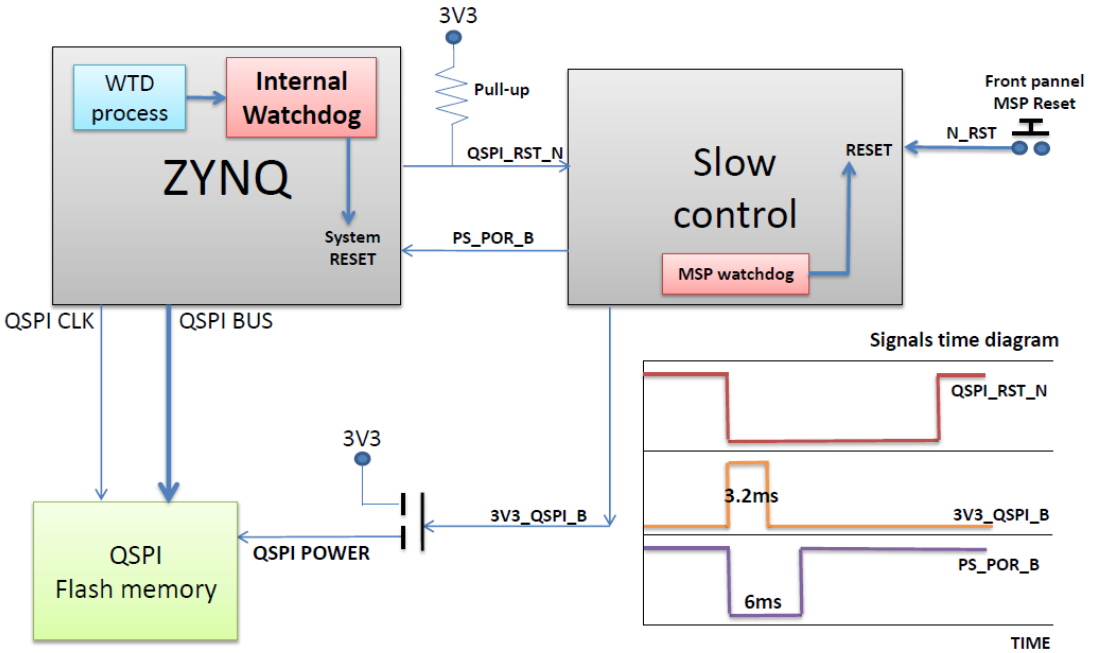
Never clearly specified:

- Watchdog: Reset UUB (FPGA+SC) or only FPGA?
- "Radio" Reset: UUB (FPGA+SC) or only FPGA?



ECR 14.4

Watchdog circuit solution 1



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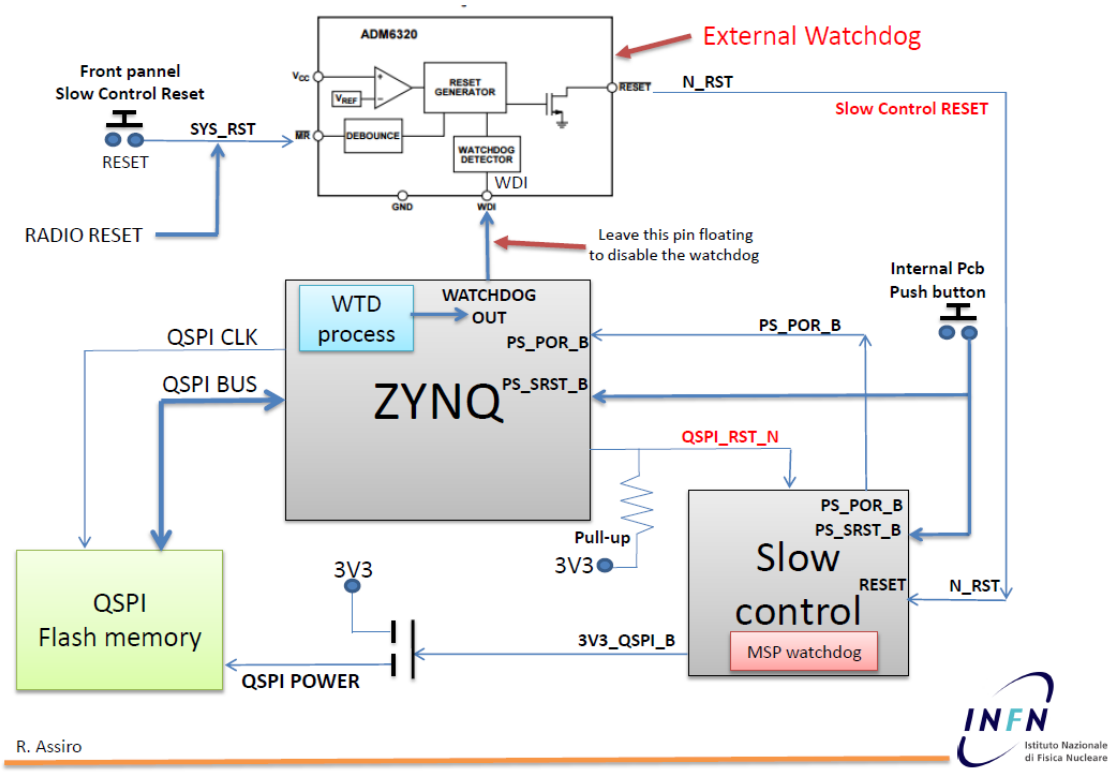
ECR 14.4

Watchdog circuit solution 2

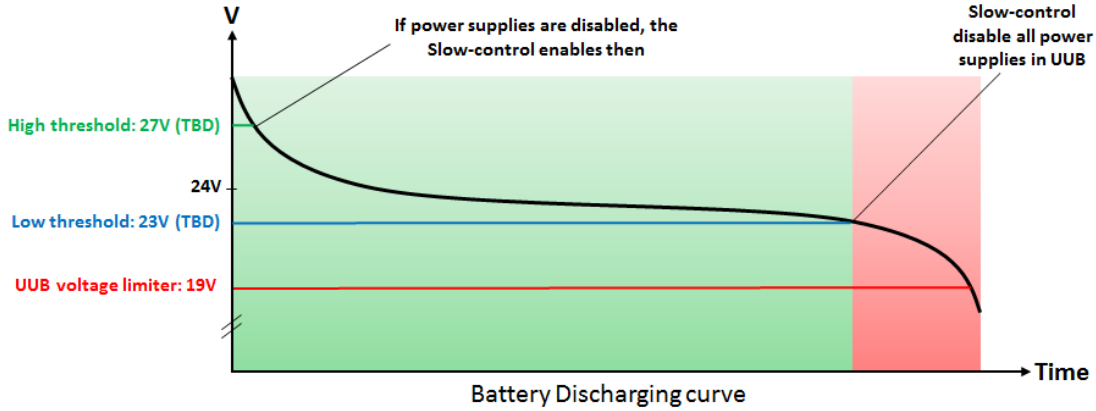


ECR (Dec 2016)

PIERRE AUGER OBSERVATORY

ECR 14.8, Solar power system Slow-control management:

If the battery voltage is too low, the electronic will twinkle. Could damage electronic and battery.



No hardware modification, only Slow-control software.

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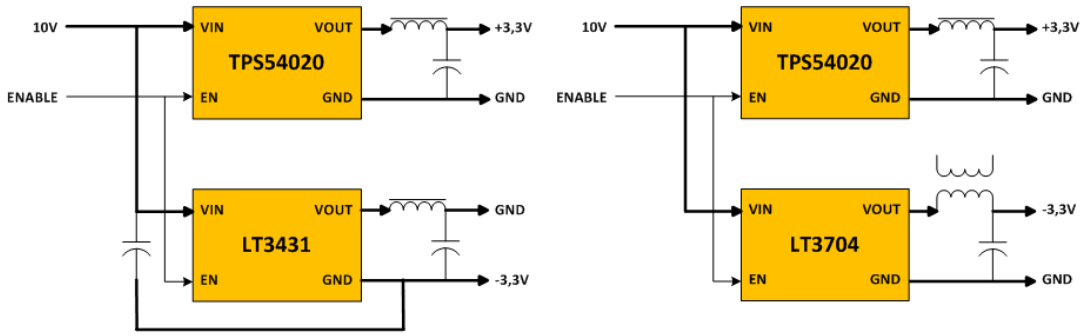
ECR (Dec 2016)

ECR 15-1, -3,3V DC/DC to be changed :



Charge pump technology
-3,3V is DC/DC voltage reference
-3,3V Enable, ERC 1-15(Feb 2016)

Not Charge pump technology: **less noisy**
¨Enable¨ NCR suppressed

Positive voltage -> negative voltage, noisy and low efficiency

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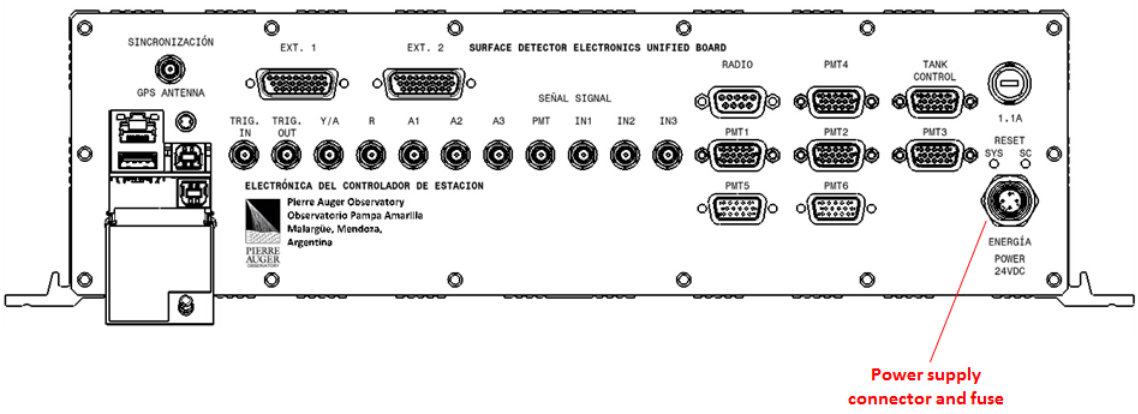
ECR (Dec 2016)

ECR 15.12, Change Power supply connector position:

Away from Front-end area on PCB to lower the noise (actual position -> specification request).



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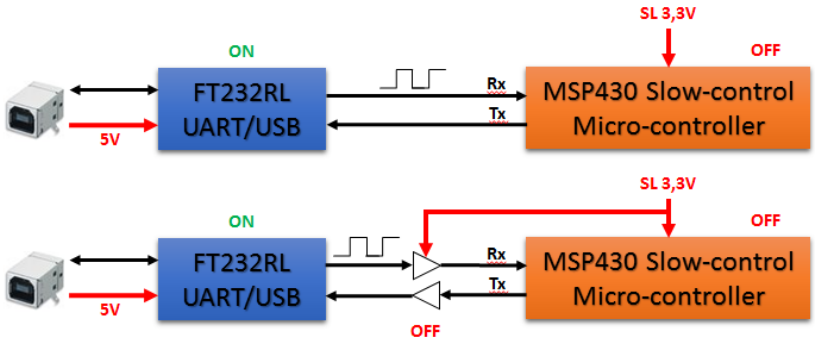
ECR (Dec 2016)

ECR 15.24, Start problem Slow-control micro-controller:

Sometime, the micro-control stopes during start sequence (NCR n° 2-67). Only when a PC is connected before the UUB turn ON.

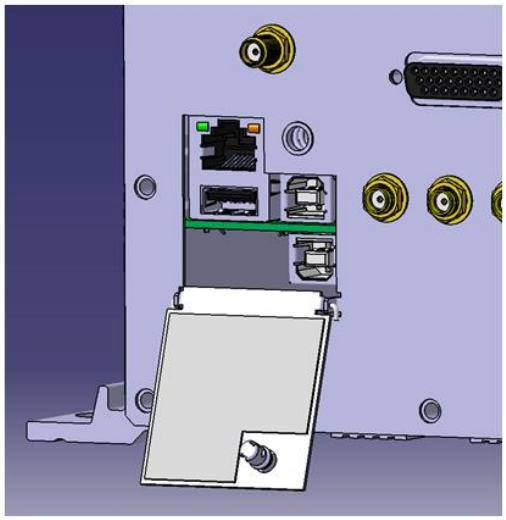


This must be made also for FPGA UART.

ECR (Dec 2016)

- **ECR 15.26, Front-panel window:**

The Front-panel window is still not defined or confirmed. Presently only the WP5 proposal is available.



ECR (Dec 2016)

ECR 15.4 & 15.27, Optimized all DC/DC layout 1/2:

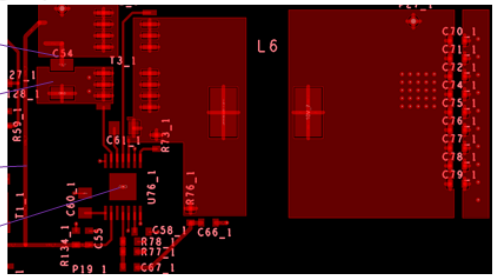
Change present 10V DC/DC LMR3150?

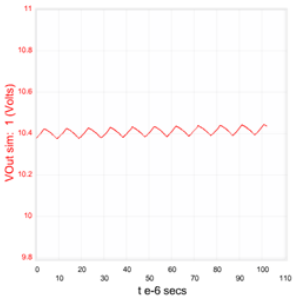
Design: adjust capacitor value

Layout: bad return current for input capacitor

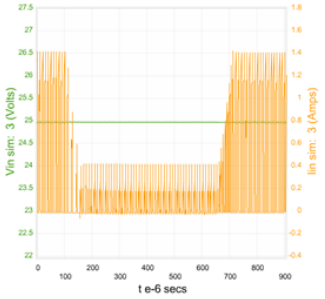
Layout: input 24V wire too thin (R bigger = more noise)

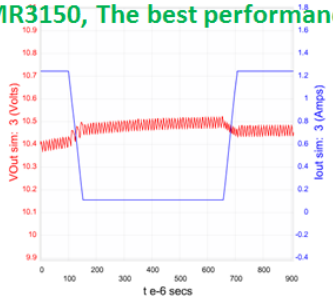
Layout: No GND junction center on DC/DC pad. Too few vias.

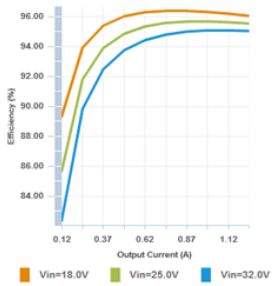




LMR3150, The best performances







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