

AUGER: SURFACE DETECTOR ELECTRONIC UPGRADE

VERSION: 1.12

DATE: 17/03/2015

BILL OF MATERIAL: X002-002-IE00-EVAL06



**PIERRE
AUGER**
OBSERVATORY

REF: /CAO-PROJETS/SPB16X/LAGORIO/AUGER/SDEU/IE00/

LPSC
53, AVENUE DES MARTYRS
38026 GRENOBLE CEDEX
+33 (0)4.76.28.41.65

ETUDE: SDEU

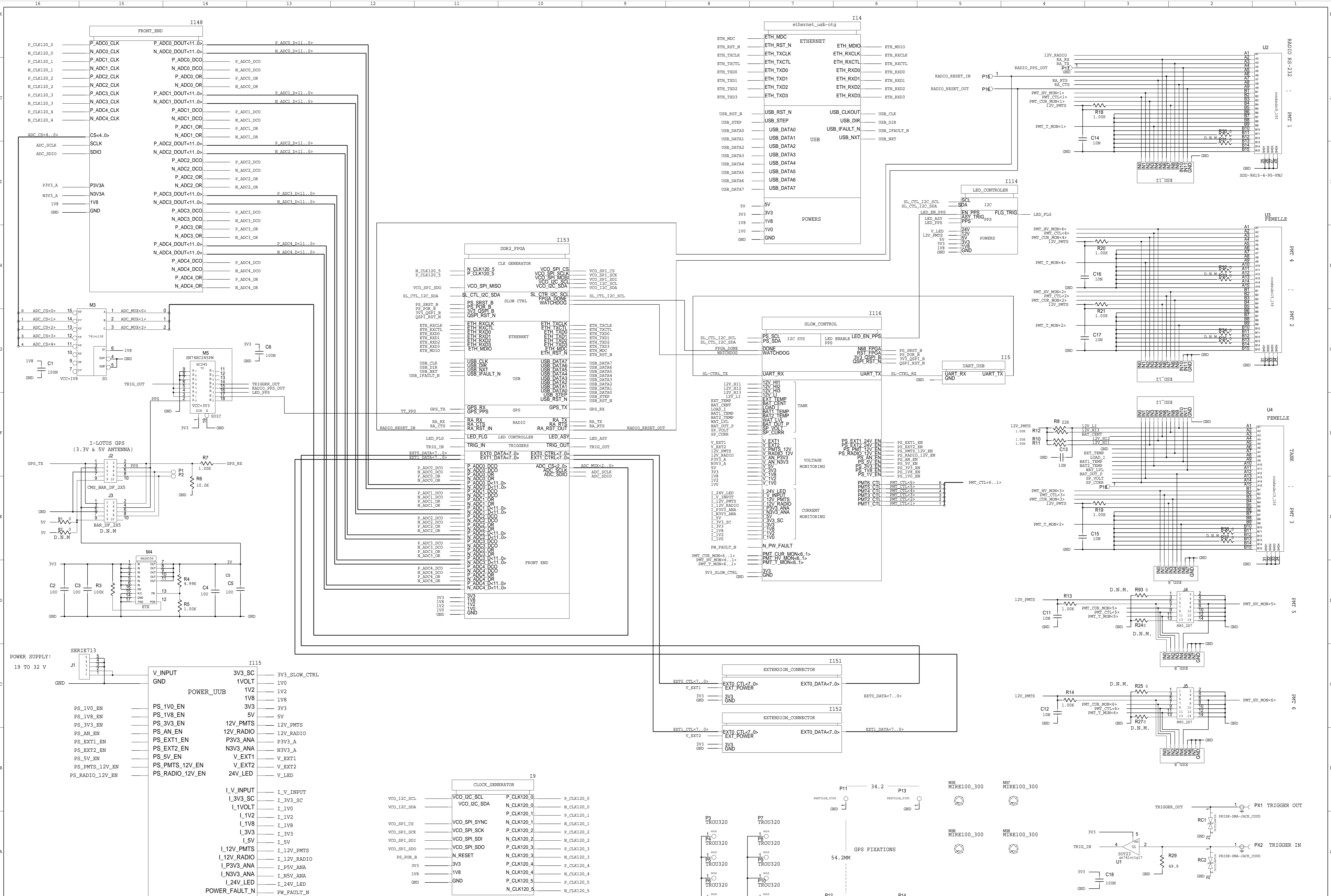
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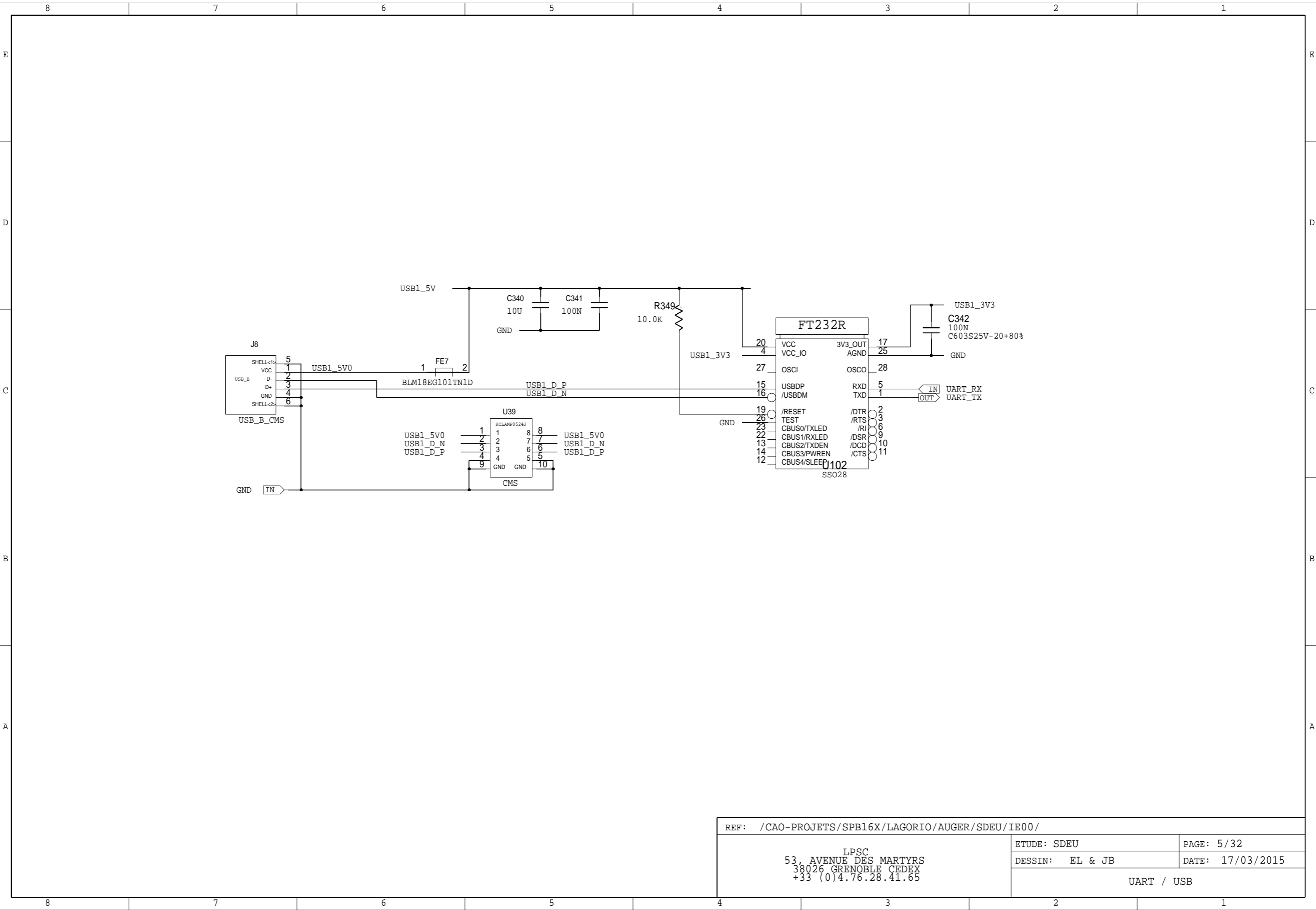
DESSIN: EL & JB

DATE: 17/03/2015

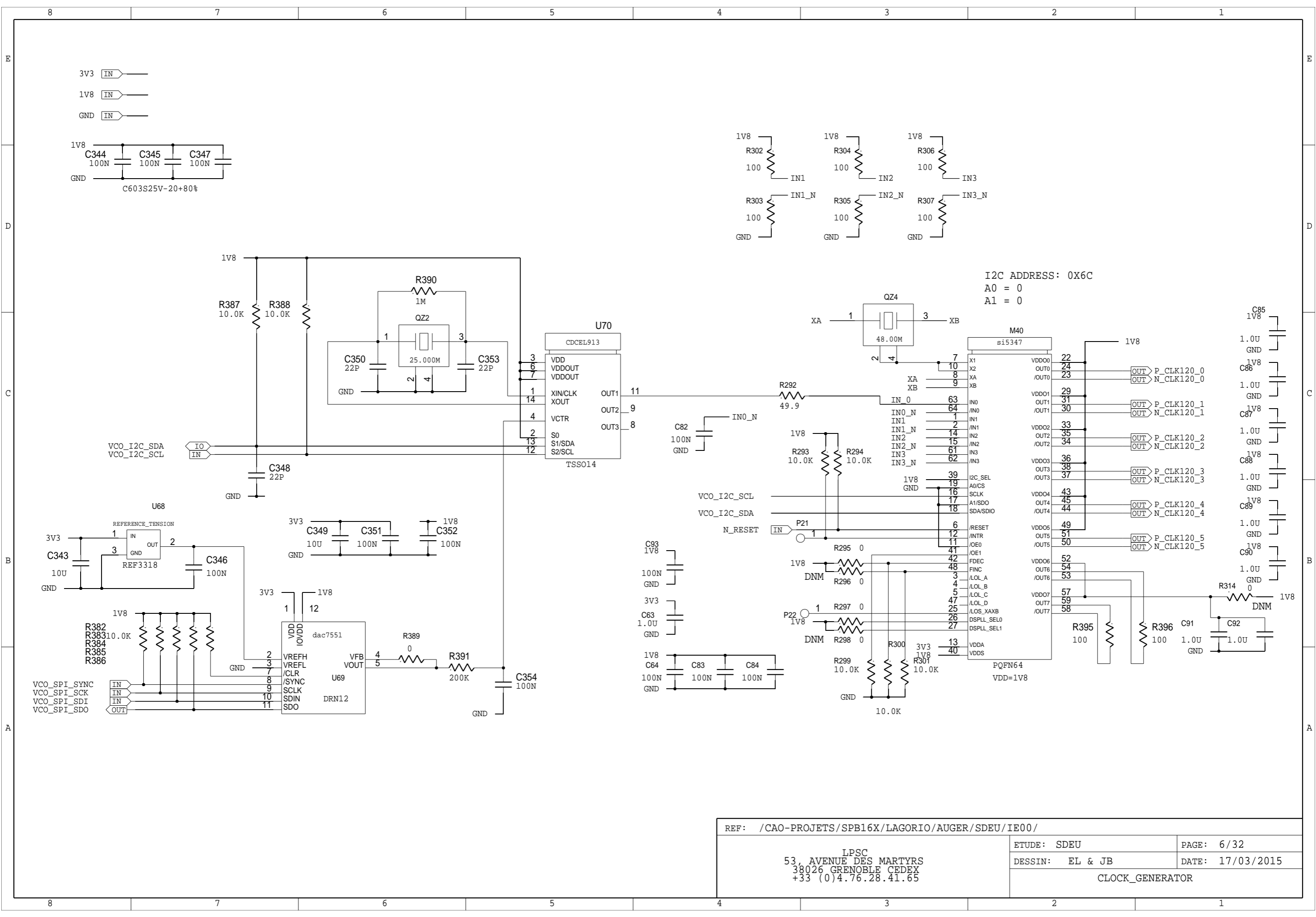
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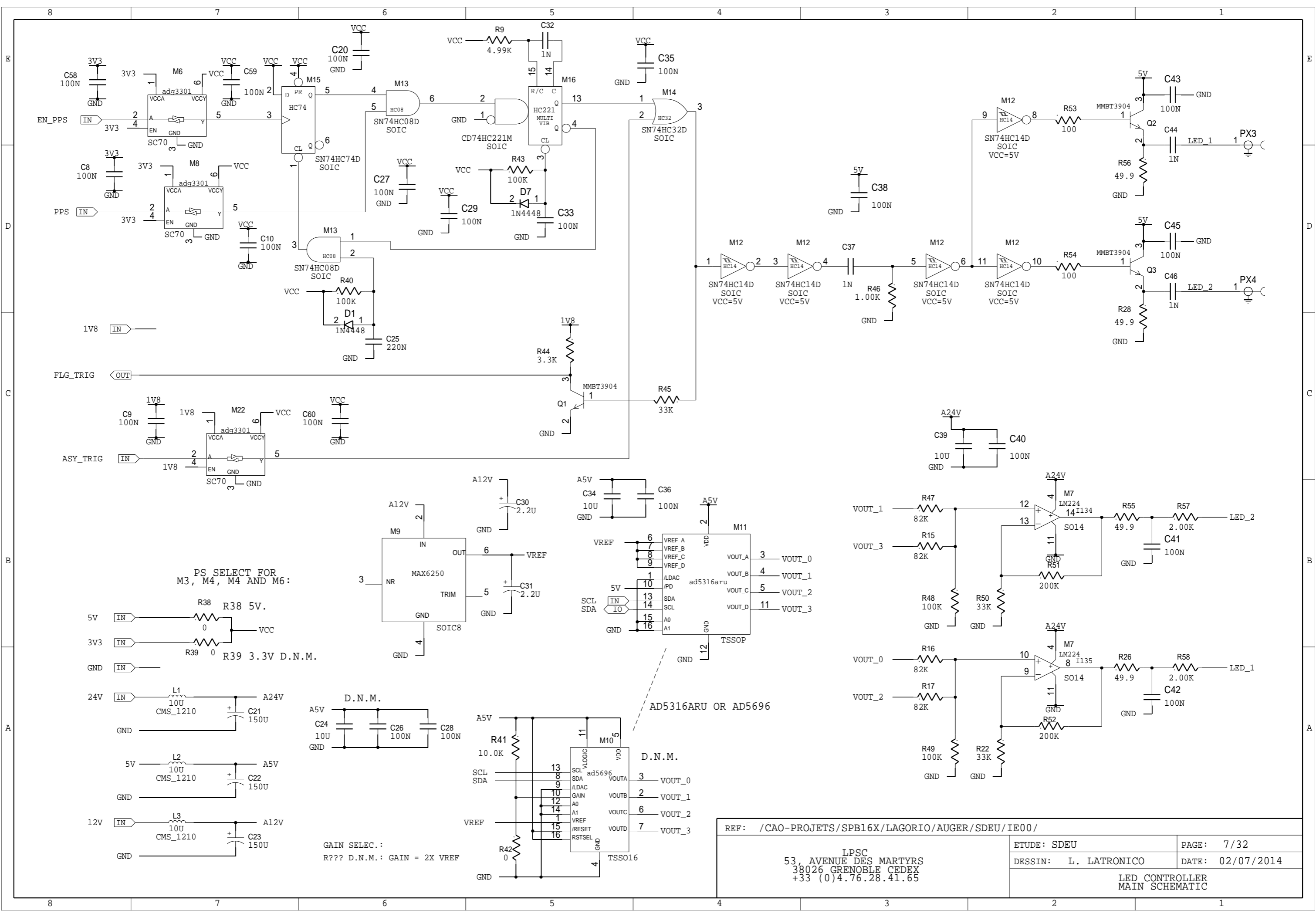


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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65	ETUDE: SDEU	PAGE: 5/32
	DESSIN: EL & JB	DATE: 17/03/2015
UART / USB		

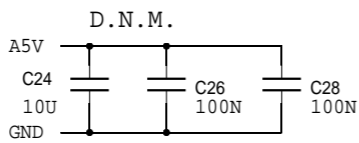
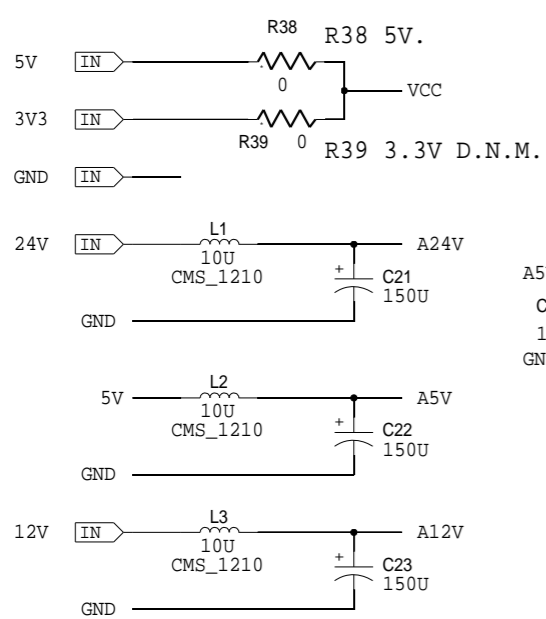


I2C ADDRESS: 0X6C
 A0 = 0
 A1 = 0

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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65		ETUDE: SDEU DESSIN: EL & JB
		PAGE: 6/32 DATE: 17/03/2015
CLOCK_GENERATOR		

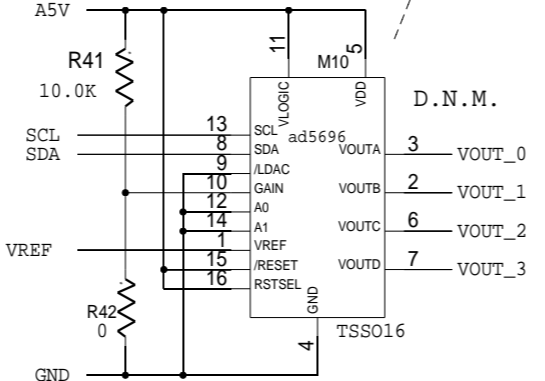


PS SELECT FOR M3, M4, M4 AND M6:



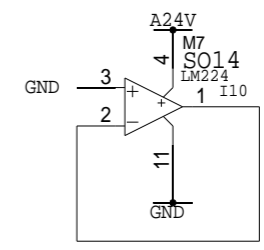
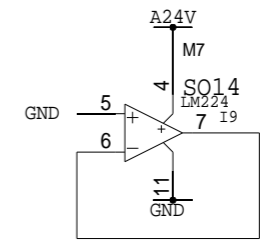
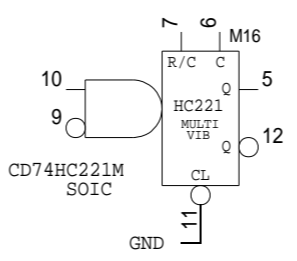
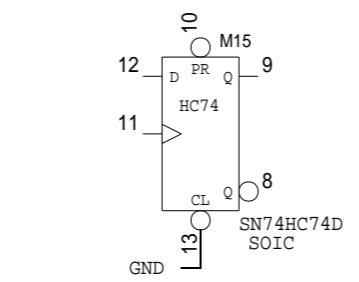
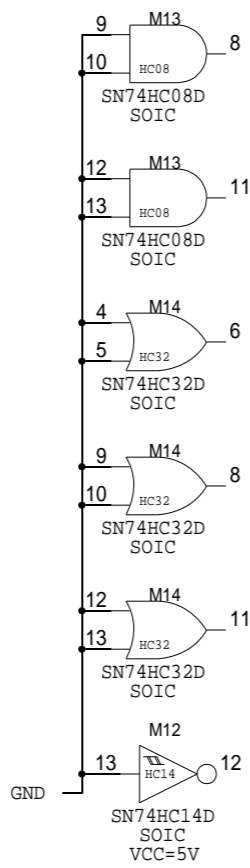
GAIN SELEC.:
R??? D.N.M.: GAIN = 2X VREF

AD5316ARU OR AD5696

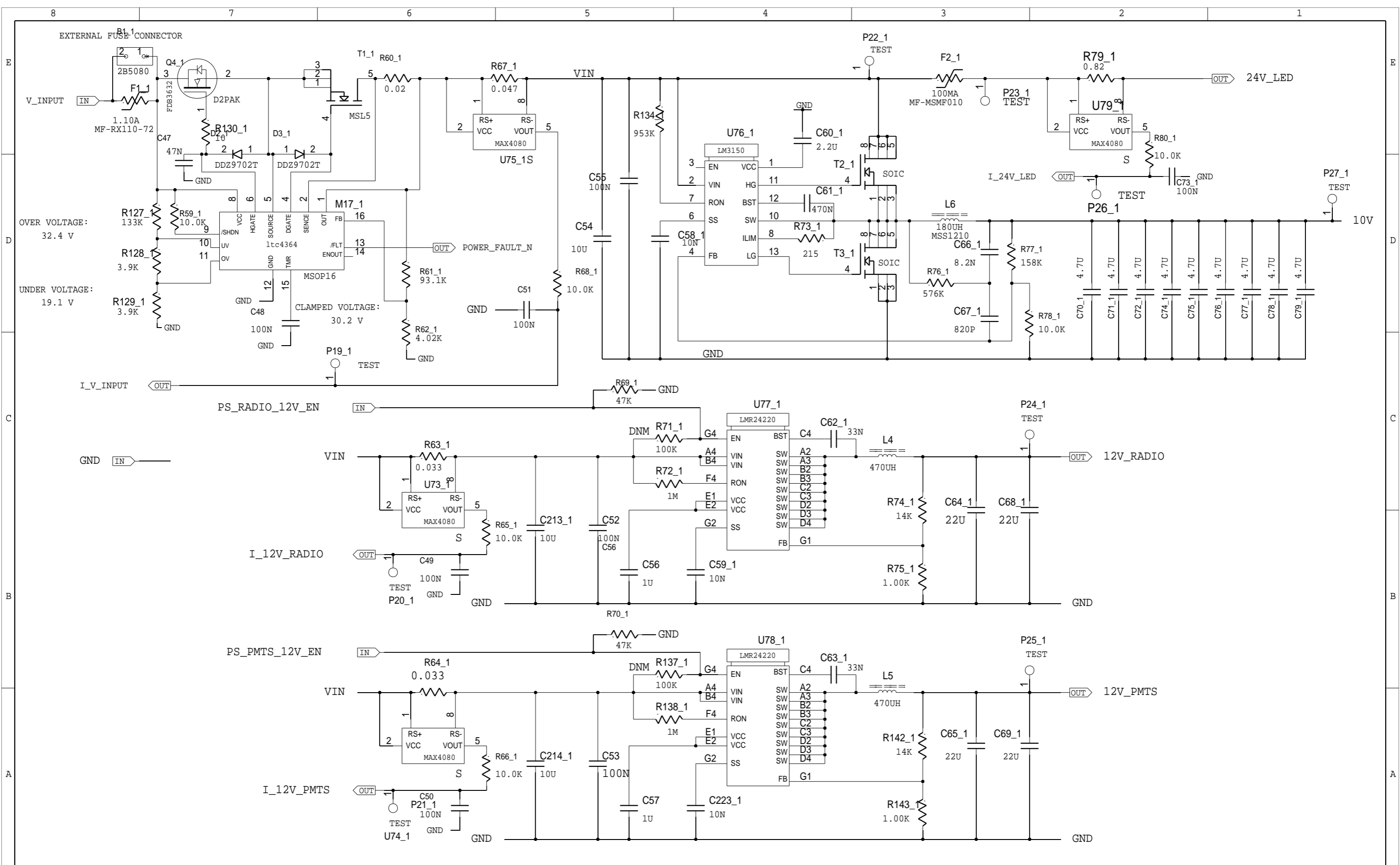


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DESSIN: L. LATRONICO	DATE: 02/07/2014
LED CONTROLLER MAIN SCHEMATIC	

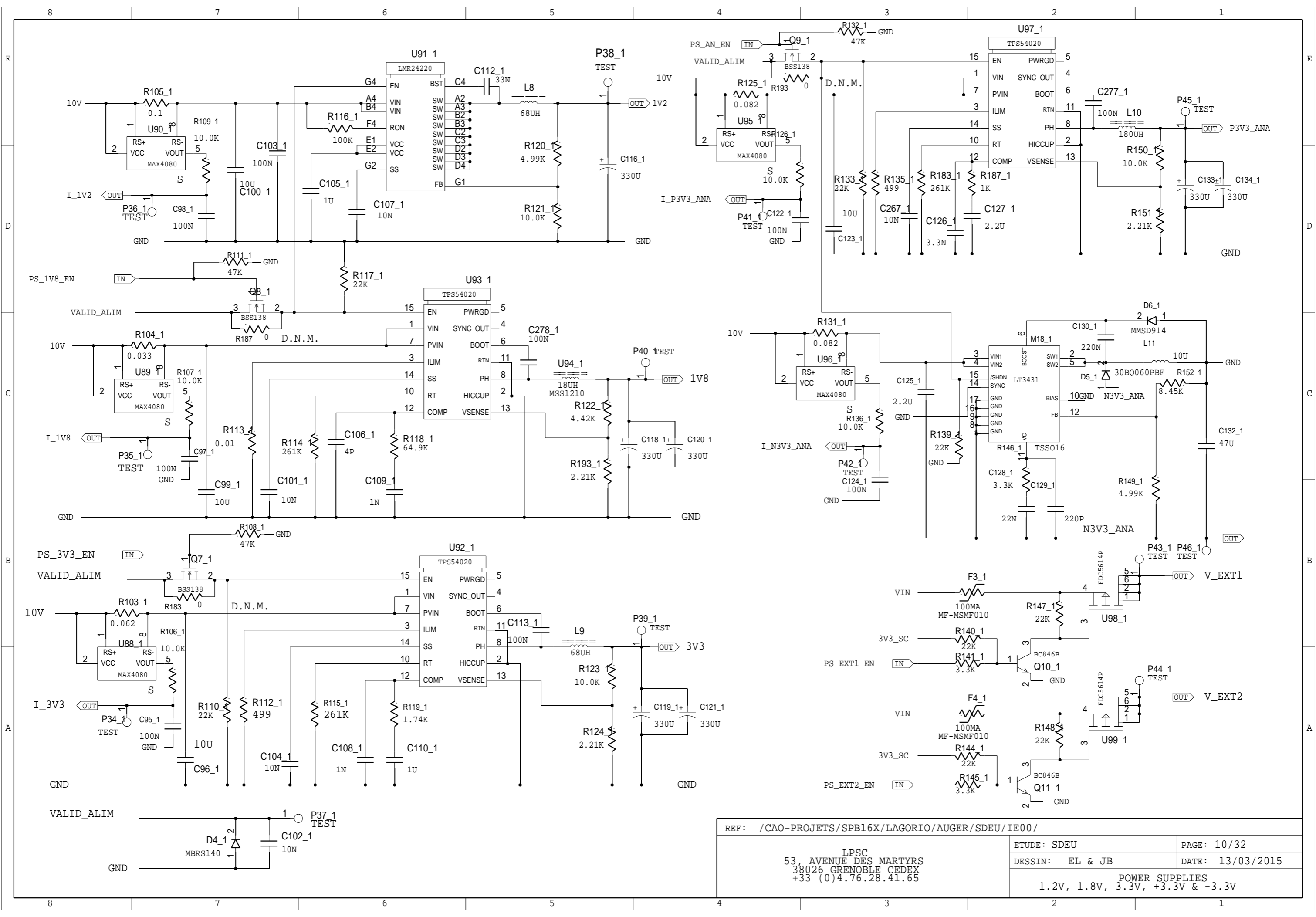
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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65	ETUDE: SDEU
	DESSIN: L. LATRONICO
LED CONTROLLER SPARE COMPONENTS	
PAGE: 8/32	DATE: 02/07/2014



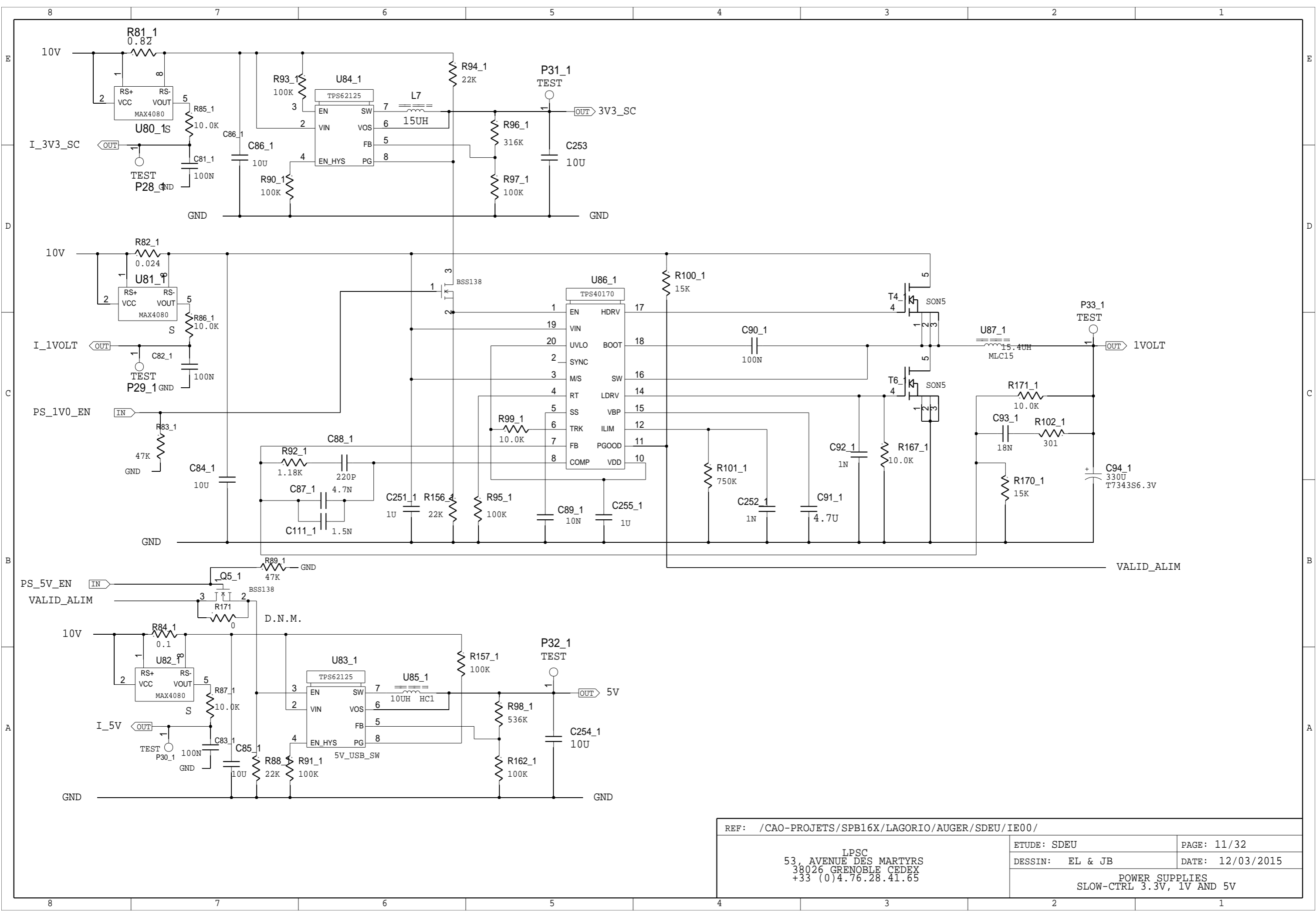
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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65	
POWER SUPPLIES PROTECTION, RADIO & PMTS 12V	



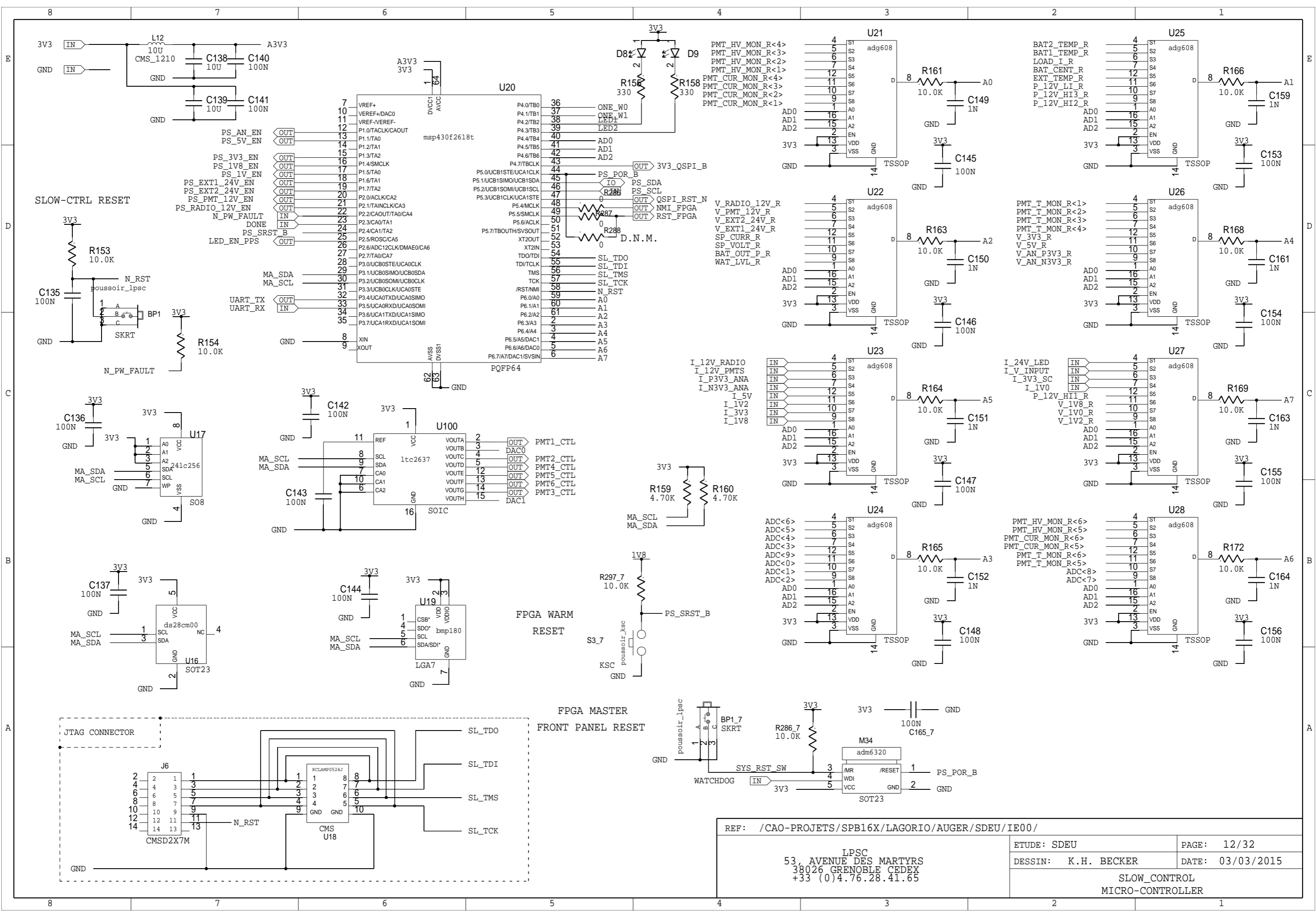
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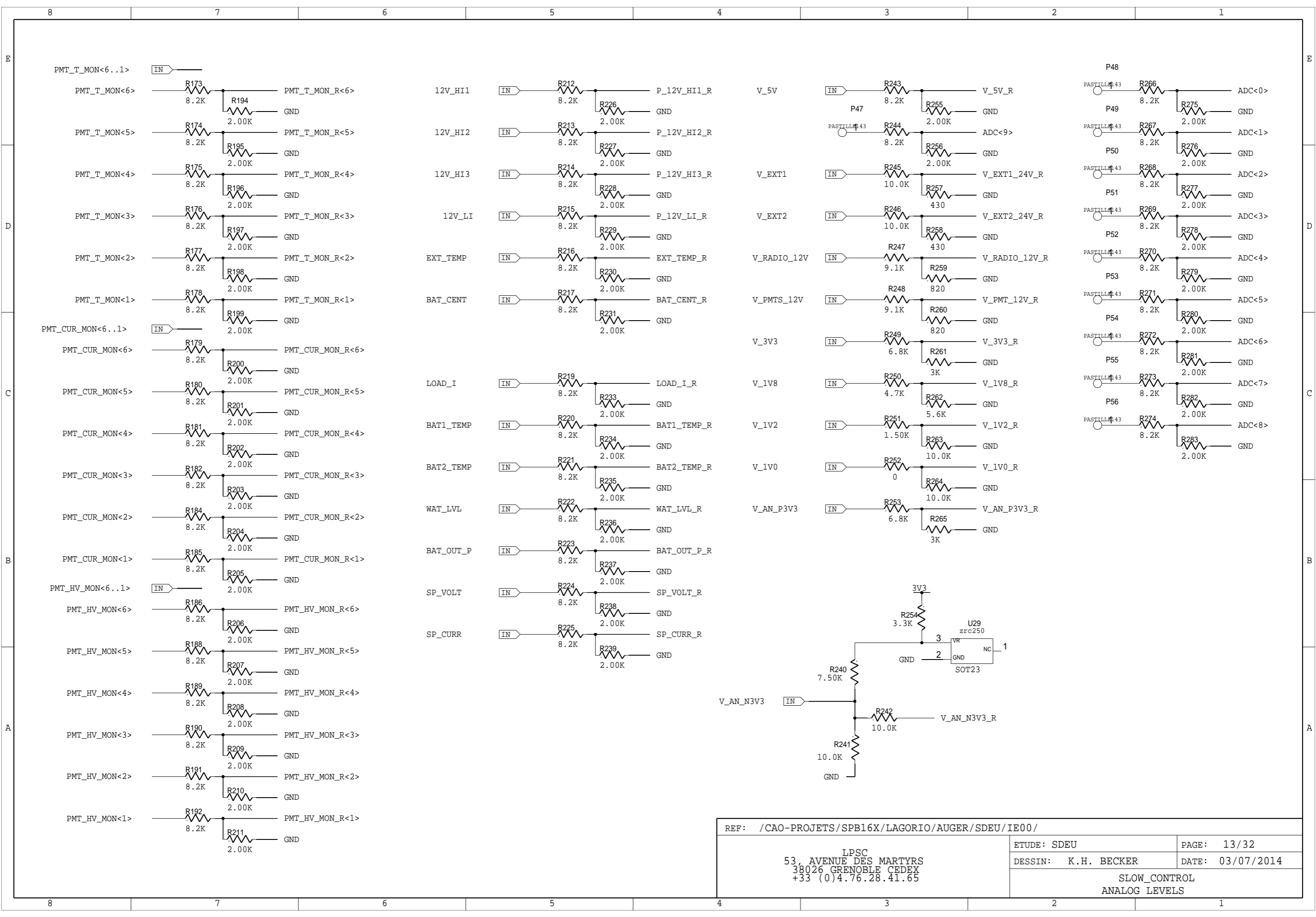
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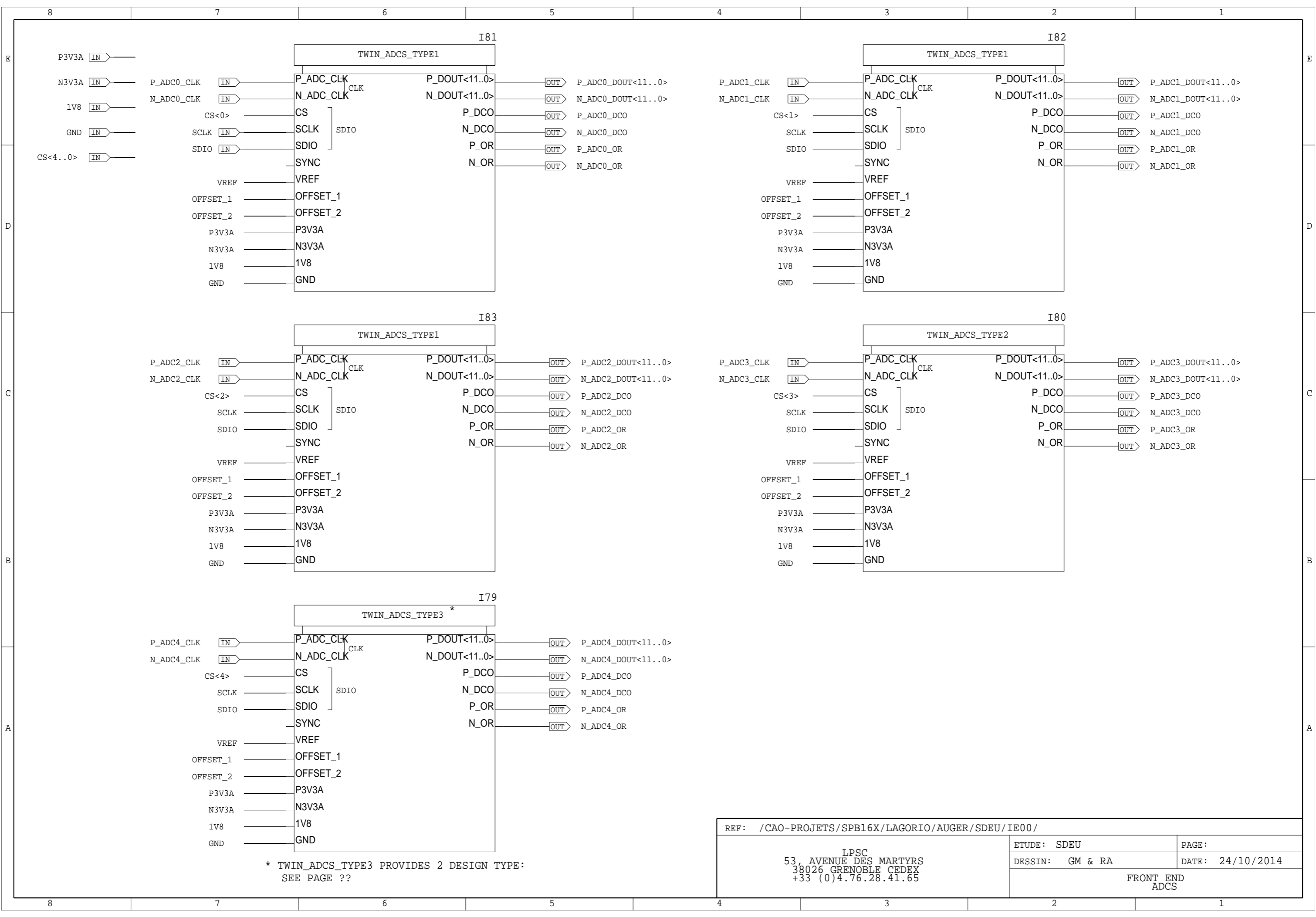
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DESSIN: EL & JB	DATE: 13/03/2015
POWER SUPPLIES	
1.2V, 1.8V, 3.3V, +3.3V & -3.3V	



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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65		DESSIN: EL & JB	DATE: 12/03/2015
		POWER SUPPLIES SLOW-CTRL 3.3V, 1V AND 5V	

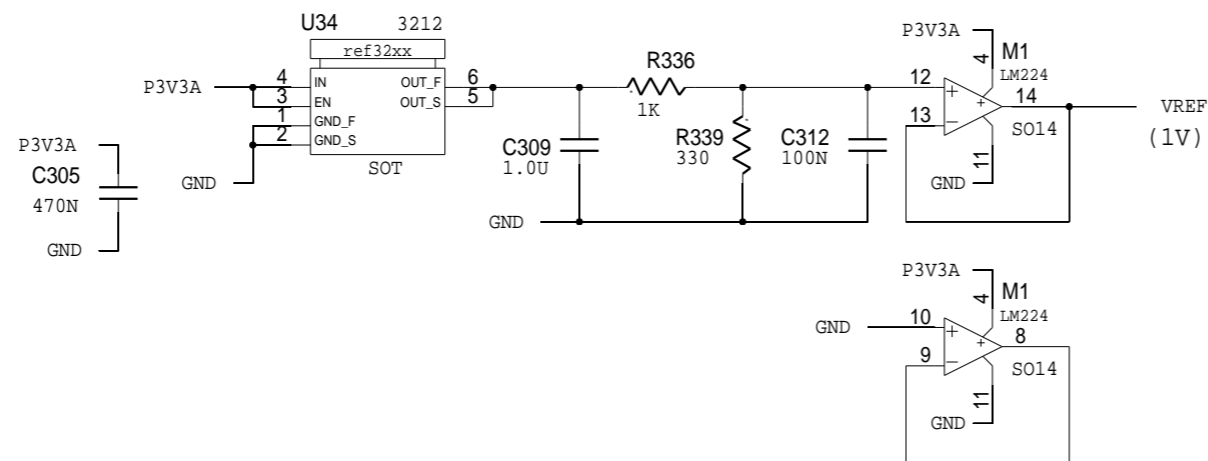
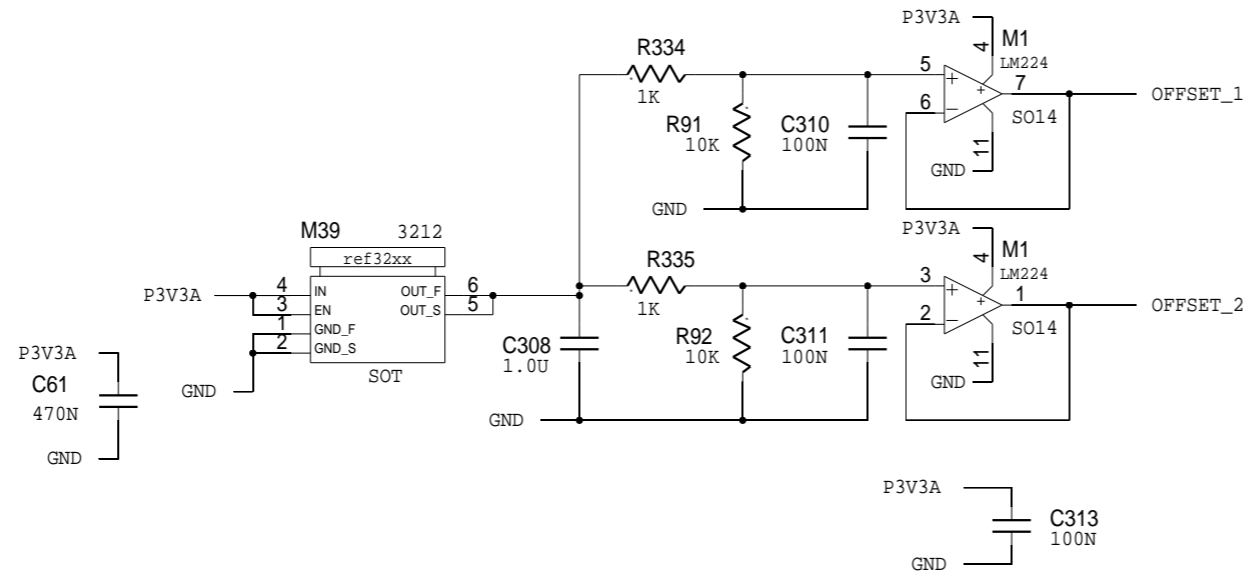






* TWIN_ADCS_TYPE3 PROVIDES 2 DESIGN TYPE:
SEE PAGE ??

REF: /CAO-PROJETS/SPB16X/LAGORIO/AUGER/SDEU/IE00/		ETUDE: SDEU	PAGE:
LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.41.65		DESSIN: GM & RA	DATE: 24/10/2014
		FRONT END ADCS	



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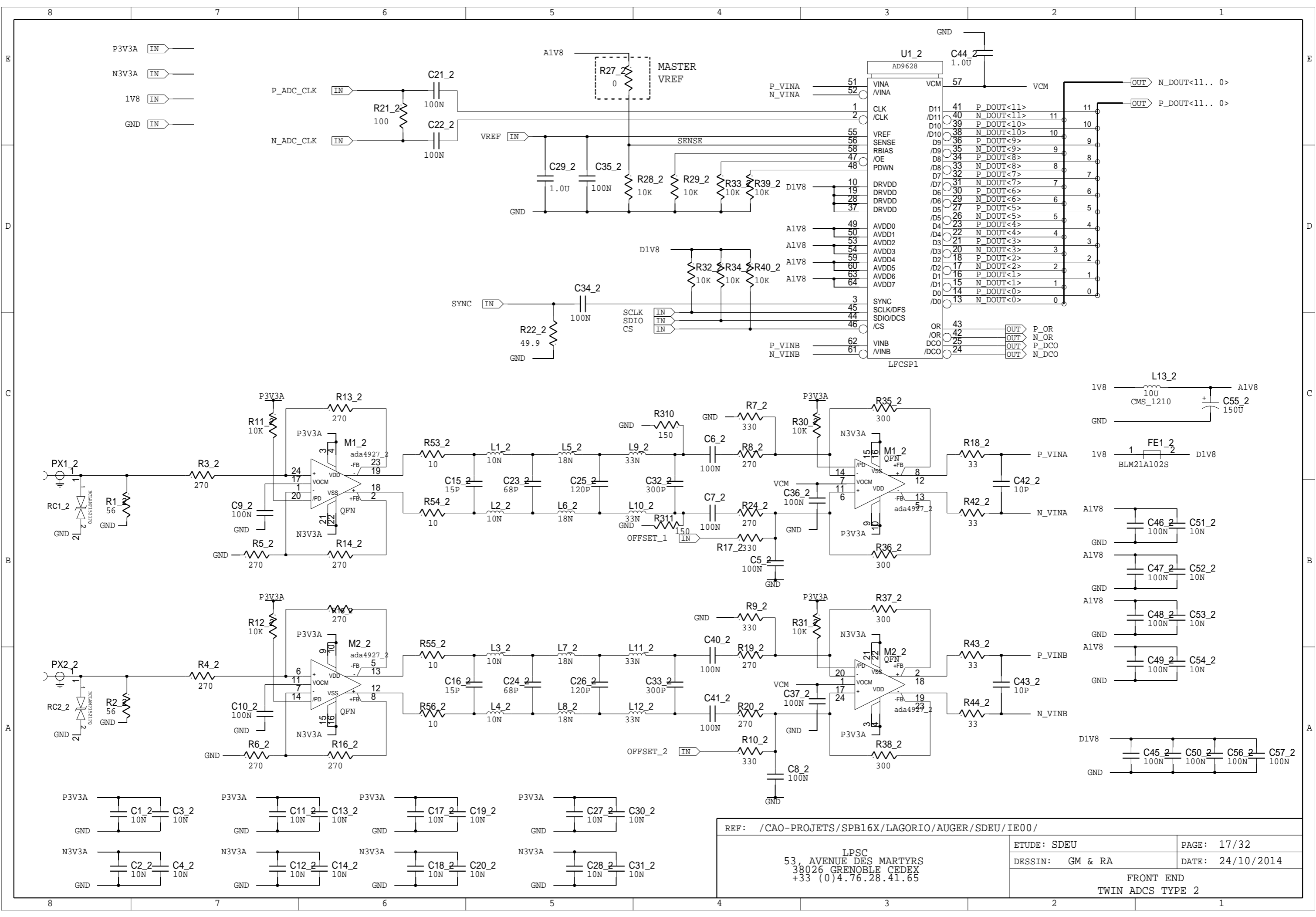
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DESSIN: GM & RA

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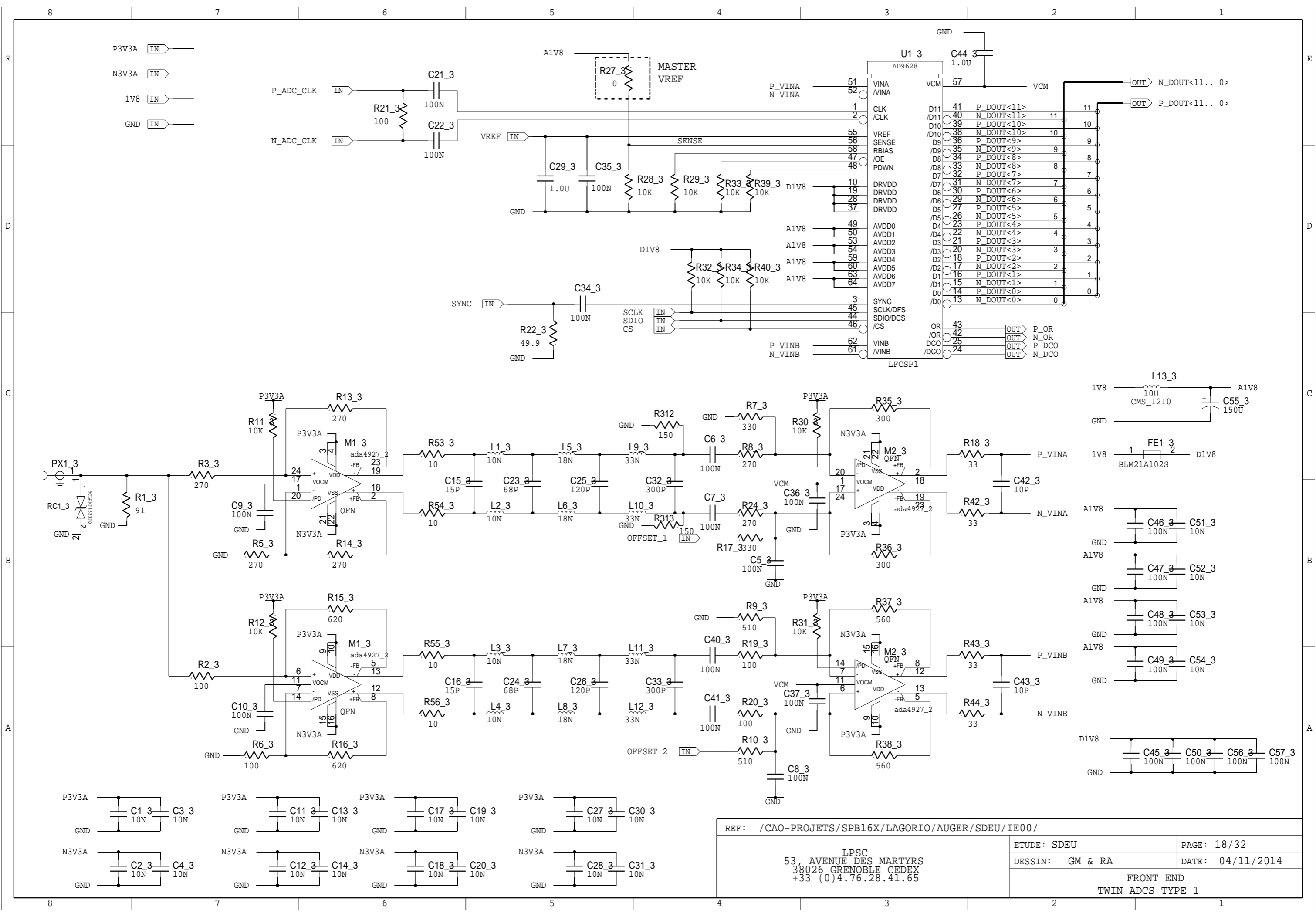
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REFERENCE VOLTAGES



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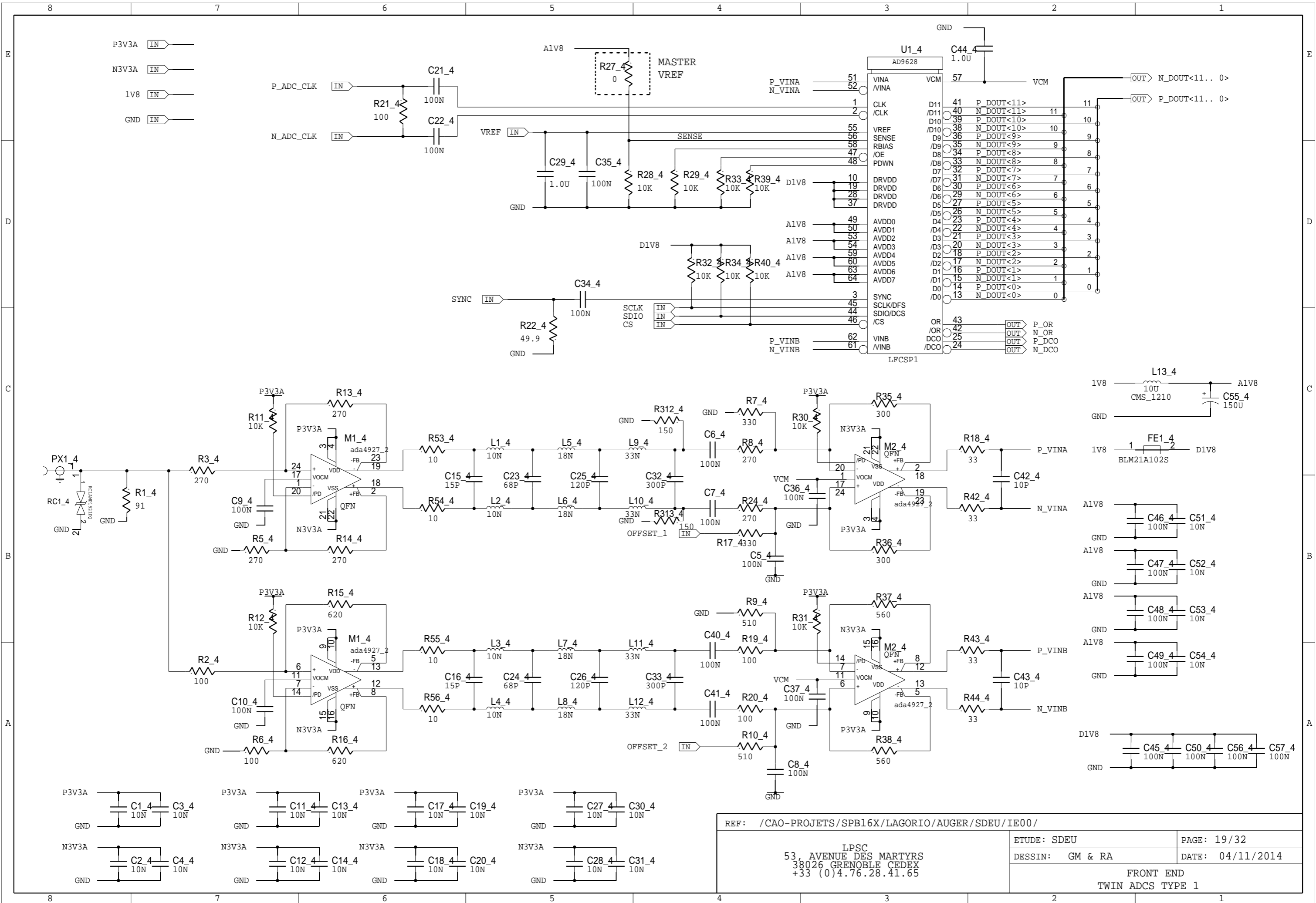
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DESSIN: GM & RA	DATE: 24/10/2014
FRONT END TWIN ADCS TYPE 2	



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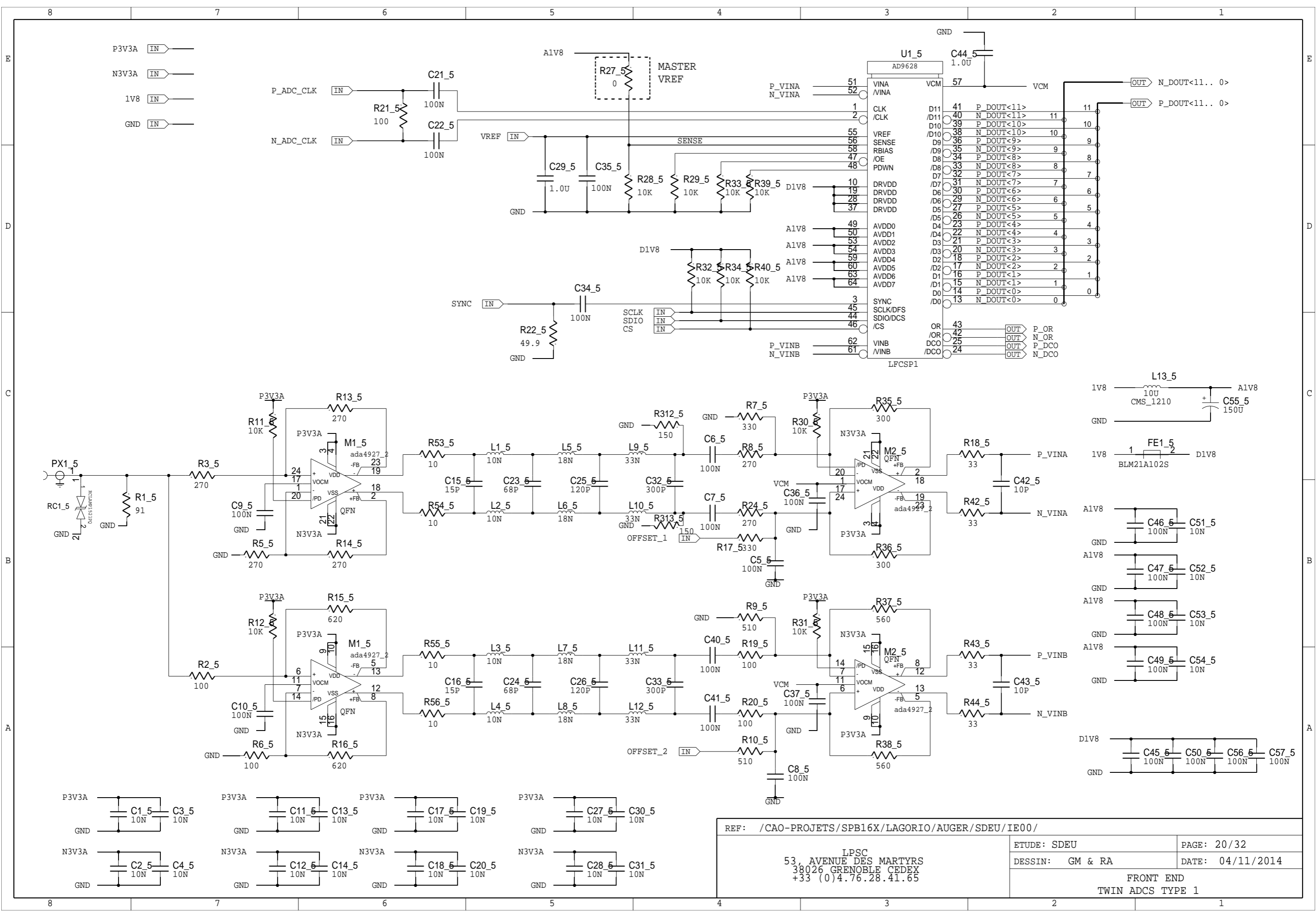
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DESSIN: GM & RA	DATE: 04/11/2014
FRONT END TWIN ADCS TYPE 1	



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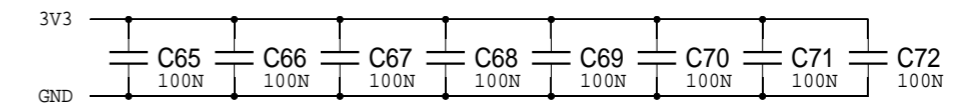
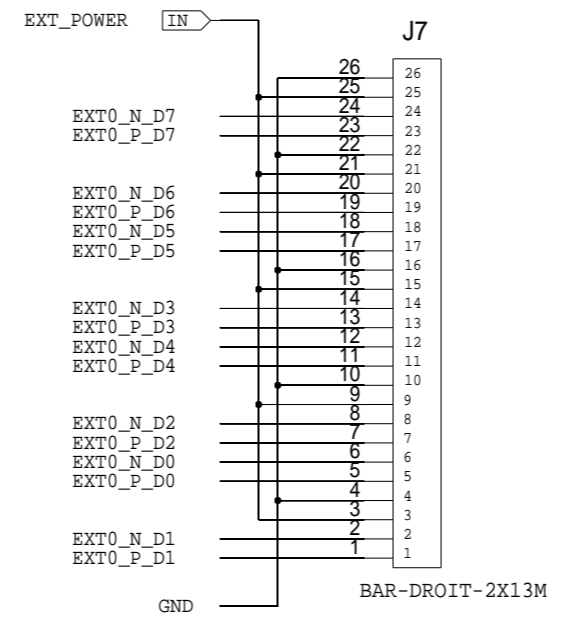
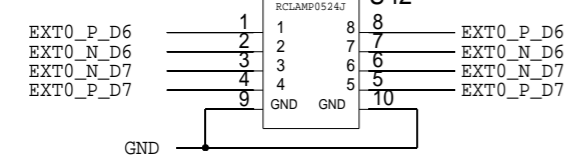
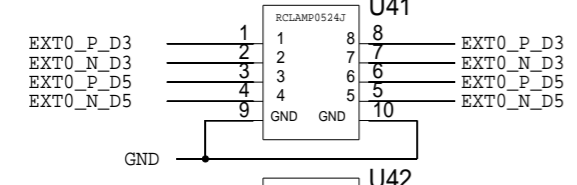
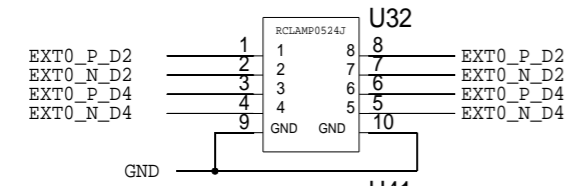
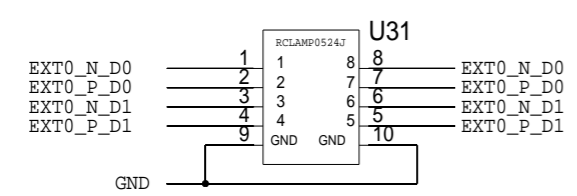
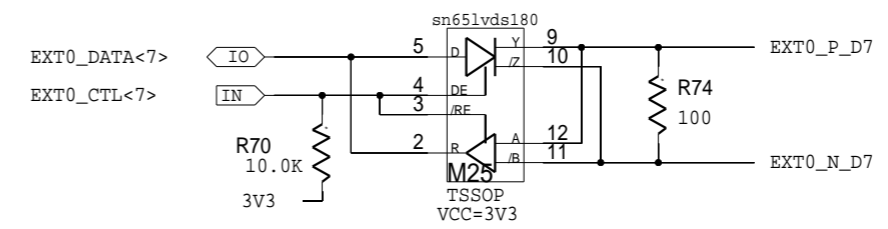
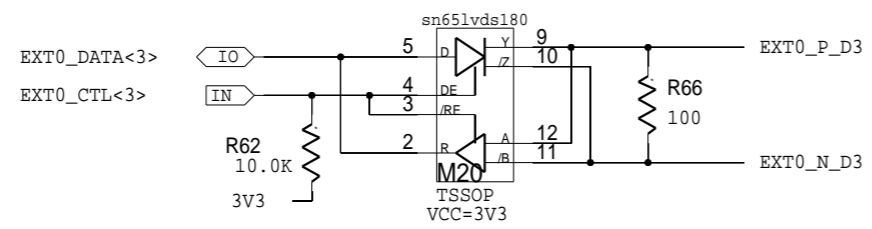
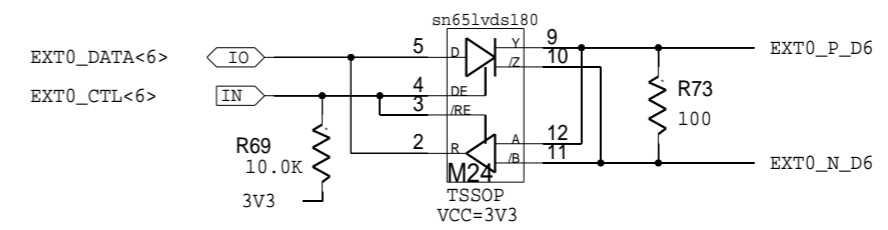
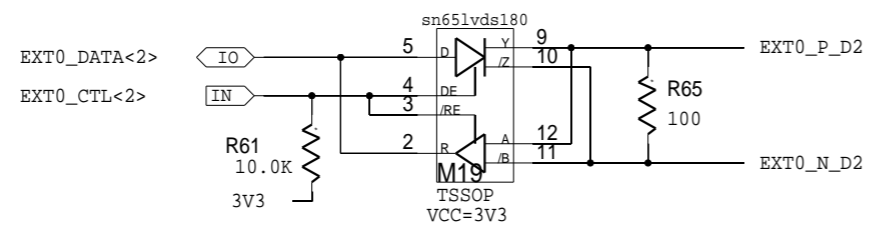
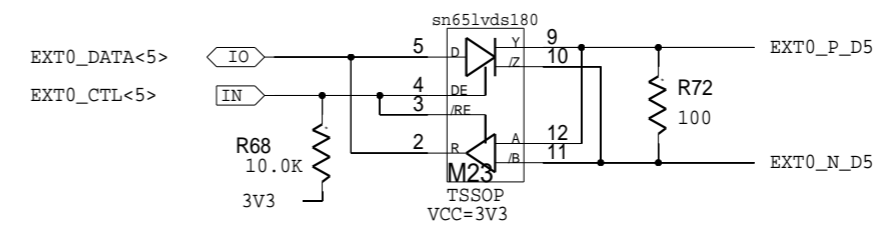
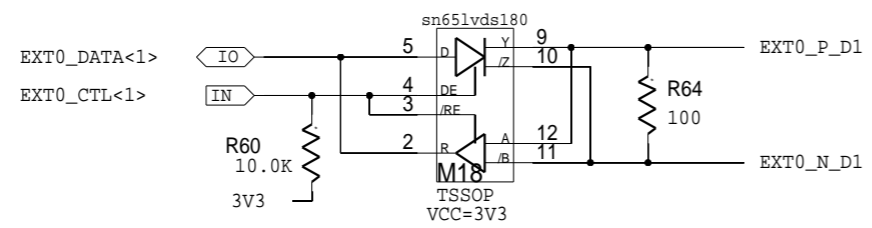
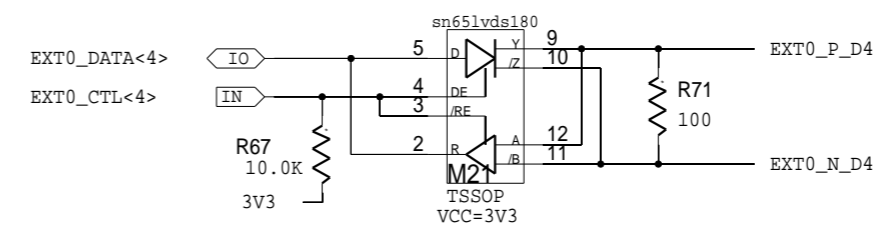
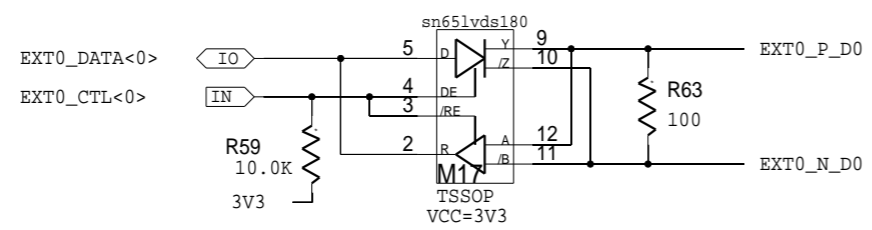
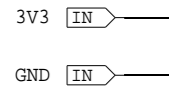
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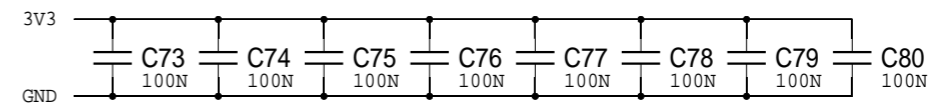
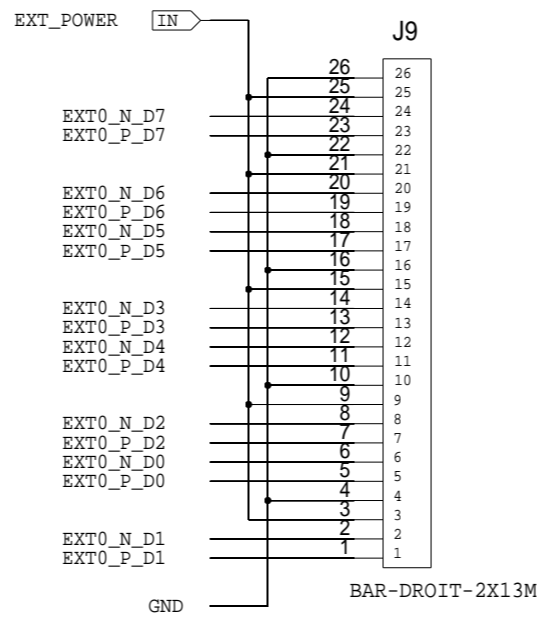
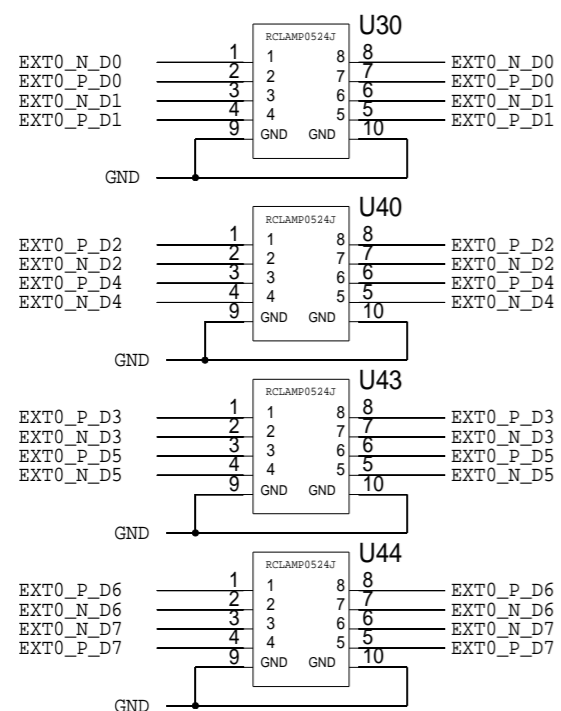
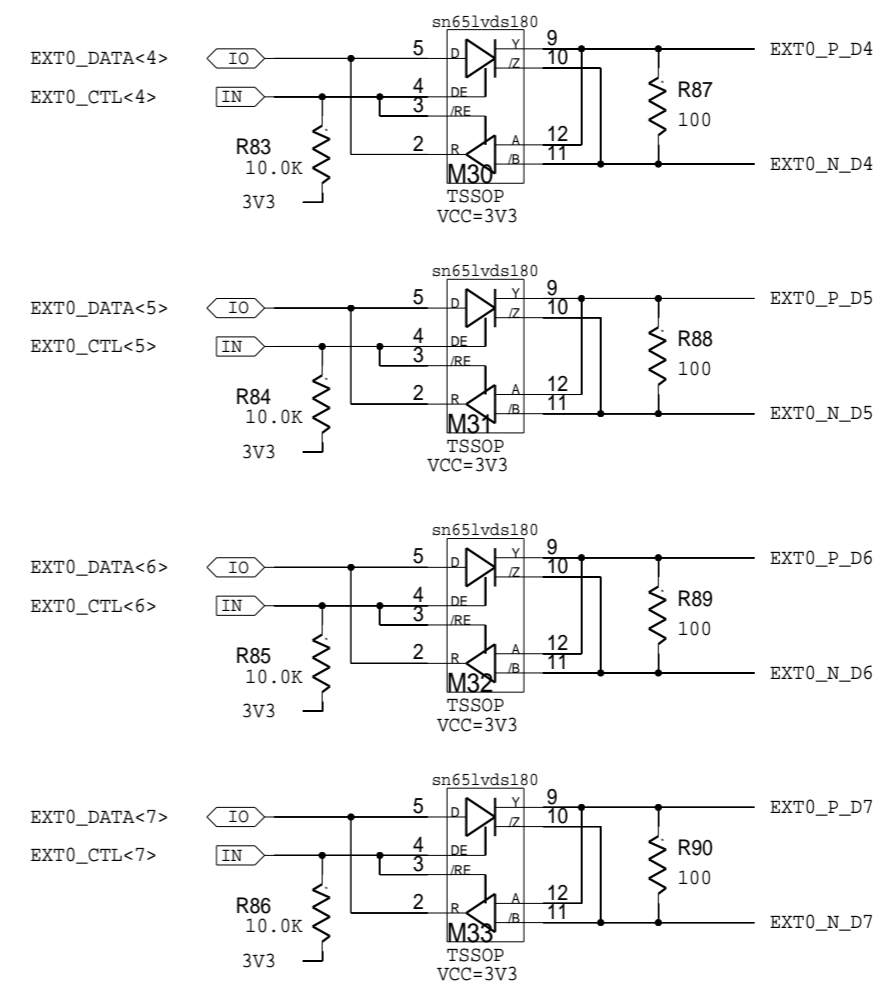
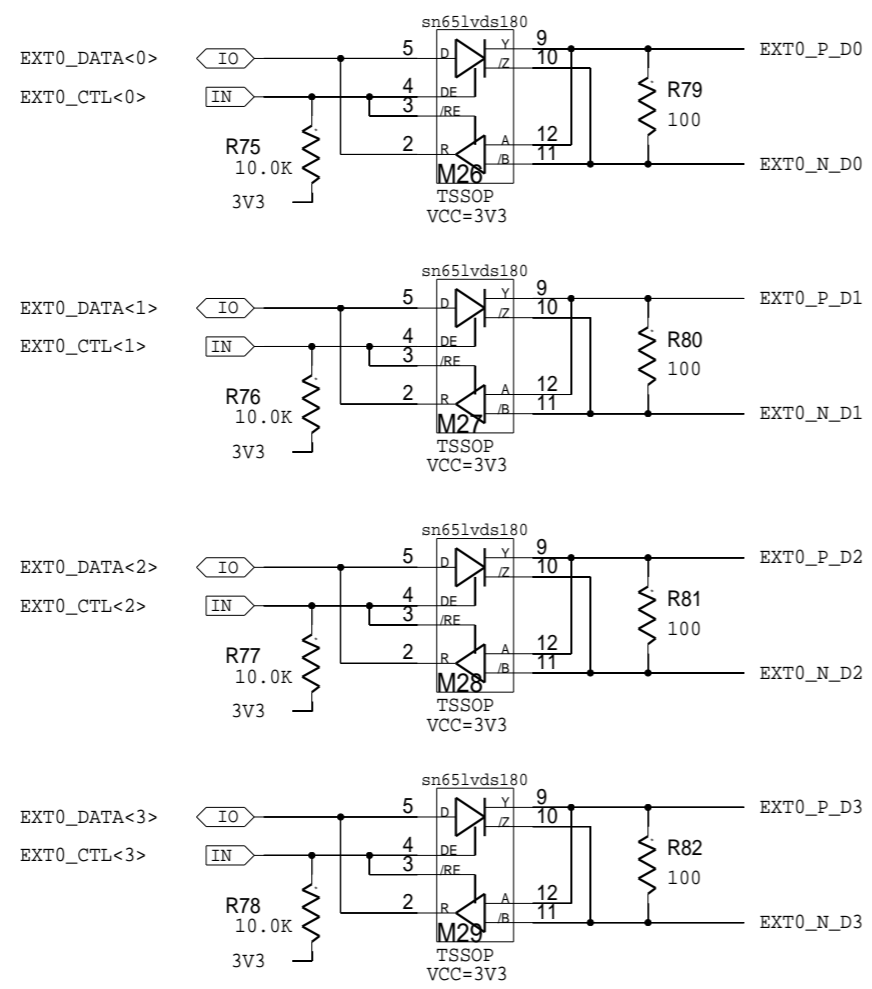
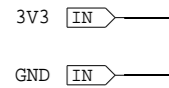


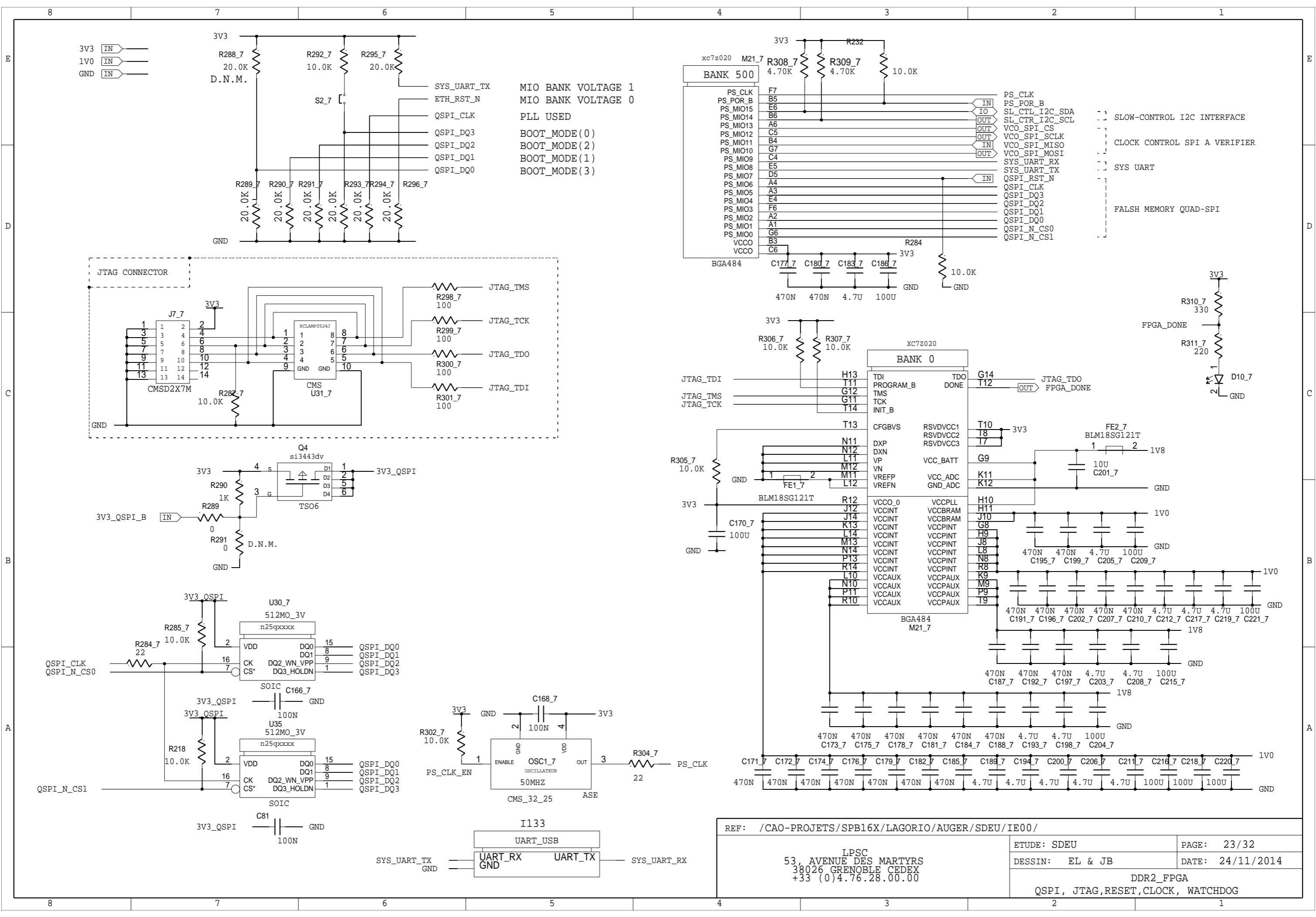
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38026 GRENOBLE CEDEX
+33 (0)4.76.28.41.65

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FRONT END TWIN ADCS TYPE 1	



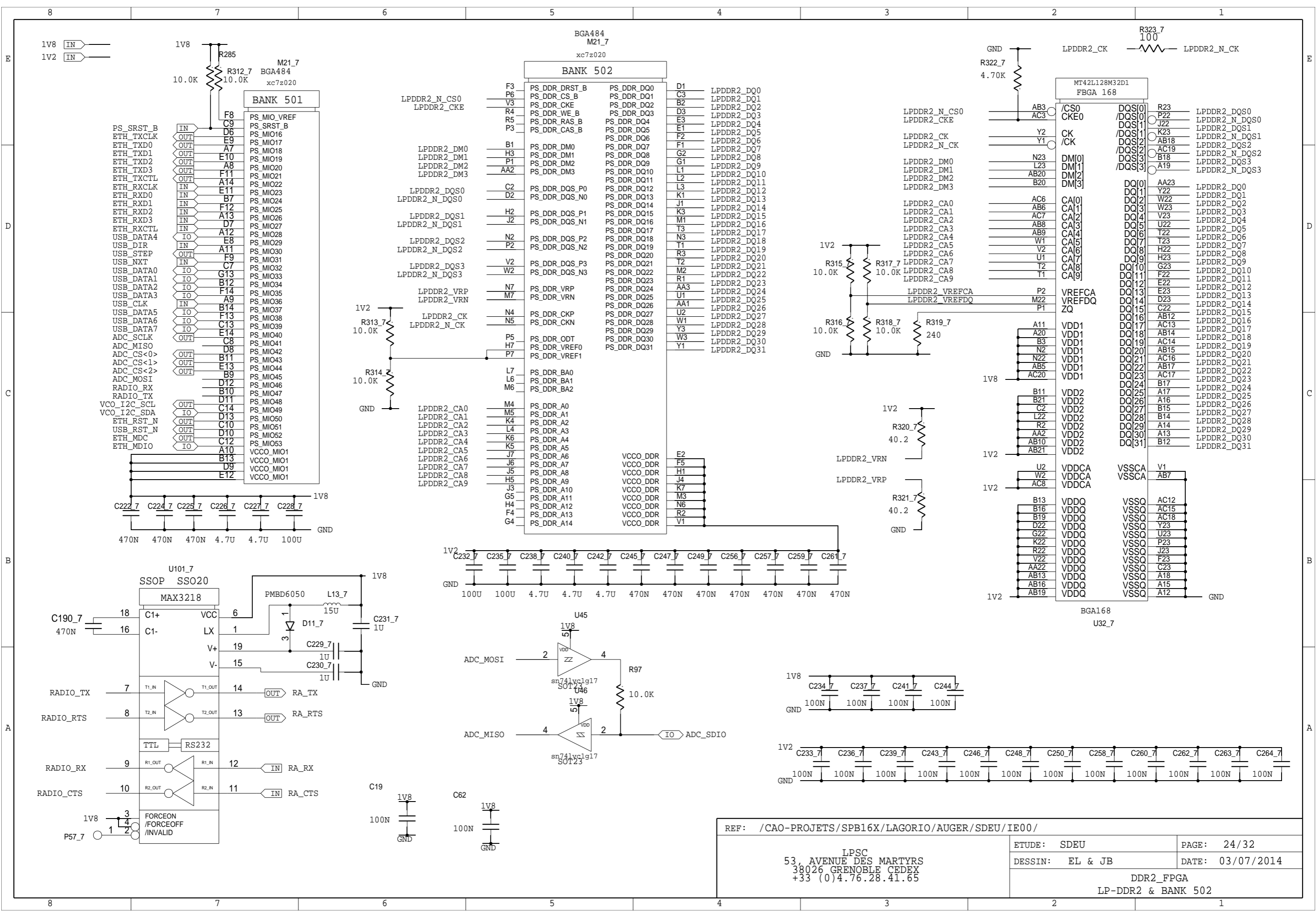


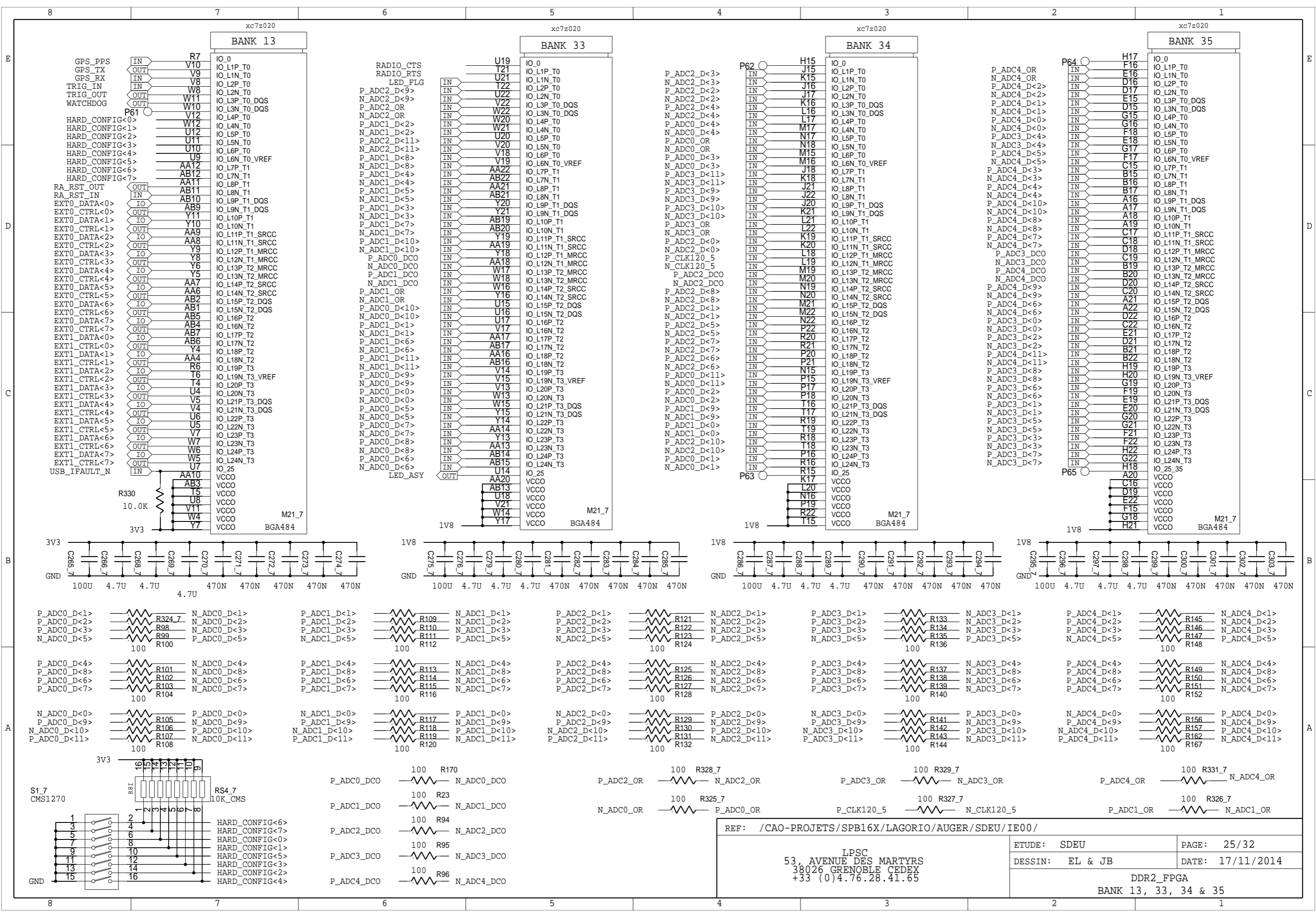


MIO BANK VOLTAGE 1
MIO BANK VOLTAGE 0
PLL USED
BOOT_MODE (0)
BOOT_MODE (2)
BOOT_MODE (1)
BOOT_MODE (3)

SLOW-CONTROL I2C INTERFACE
CLOCK CONTROL SPI A VERIFIER
SYS UART
FLASH MEMORY QUAD-SPI

REF: /CAO-PROJETS/SPB16X/LAGORIO/AUGER/SDEU/IE00/	
ETUDE: SDEU	PAGE: 23/32
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LPSC 53, AVENUE DES MARTYRS 38026 GRENOBLE CEDEX +33 (0)4.76.28.00.00	
DDR2_FPGA QSPI, JTAG, RESET, CLOCK, WATCHDOG	





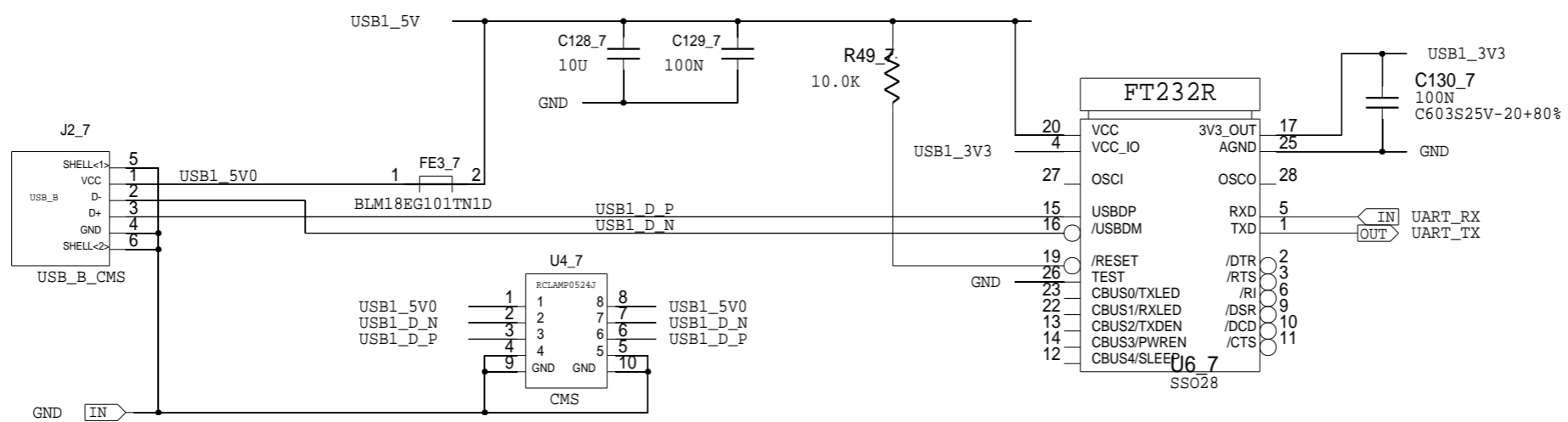
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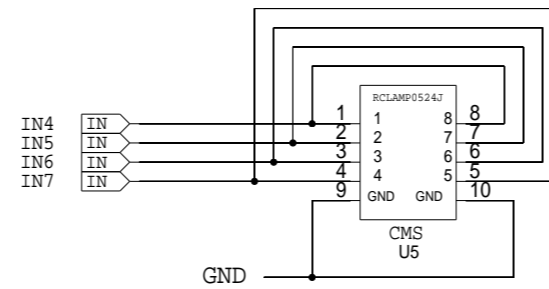
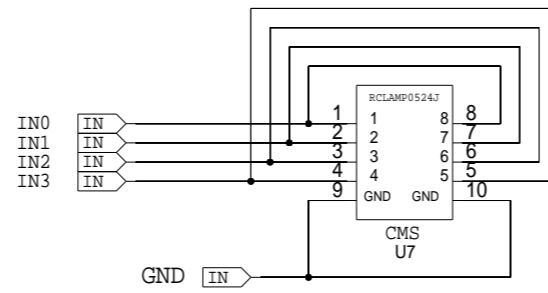
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DDR2_FPGA
BANK 13, 33, 34 & 35

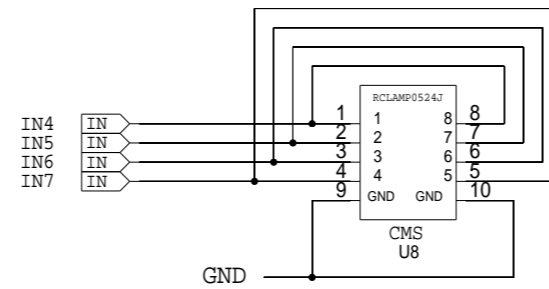
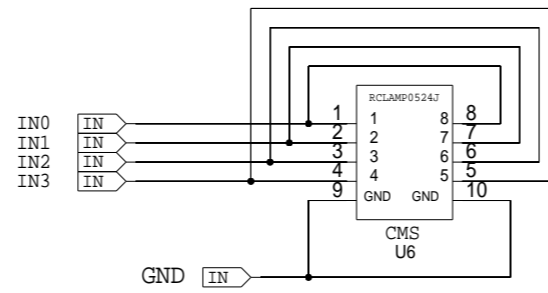
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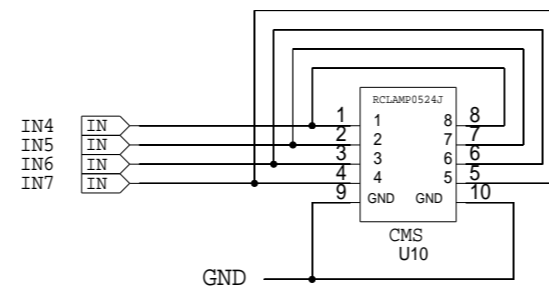
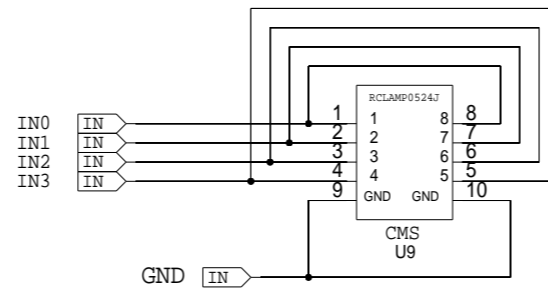
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	DESSIN: EL & JB	DATE: 17/03/2015
UART / USB		



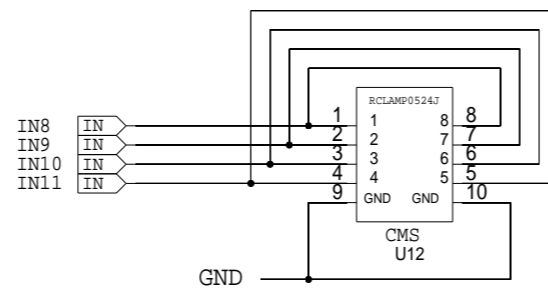
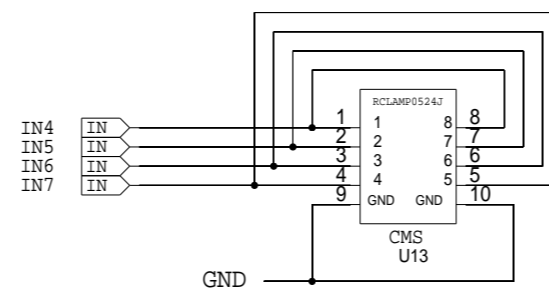
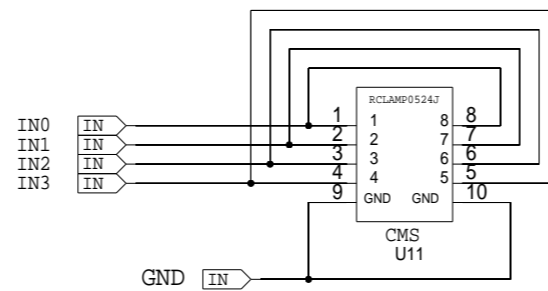
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PAGE: 27/32	
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ESD 8 PINS PROTECTION DB15 CONNECTORS	



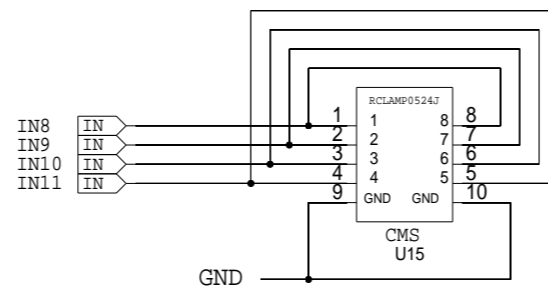
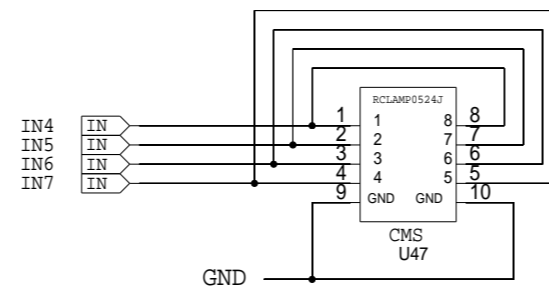
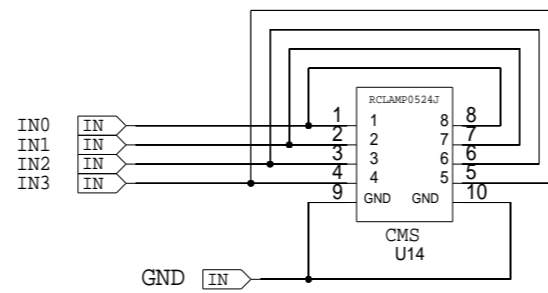
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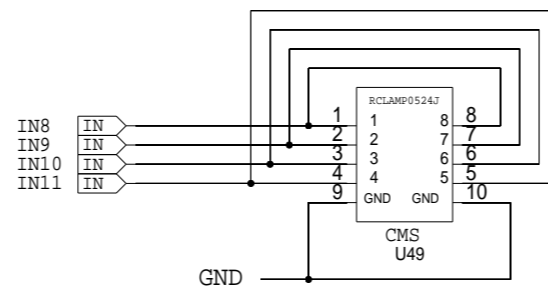
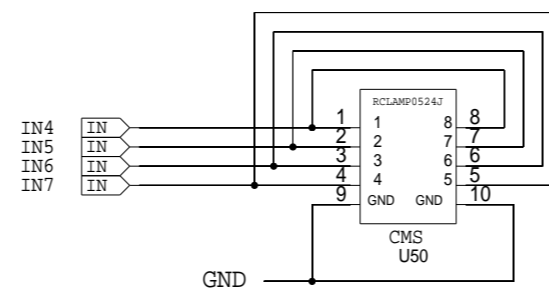
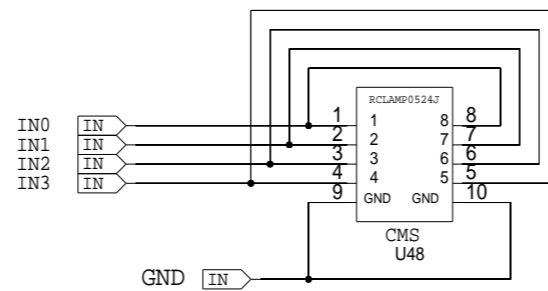
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