Pierre Auger Observatory
Surface Detector Electronics
4th February 2015 - Orsay

Critical Design Review

WP5

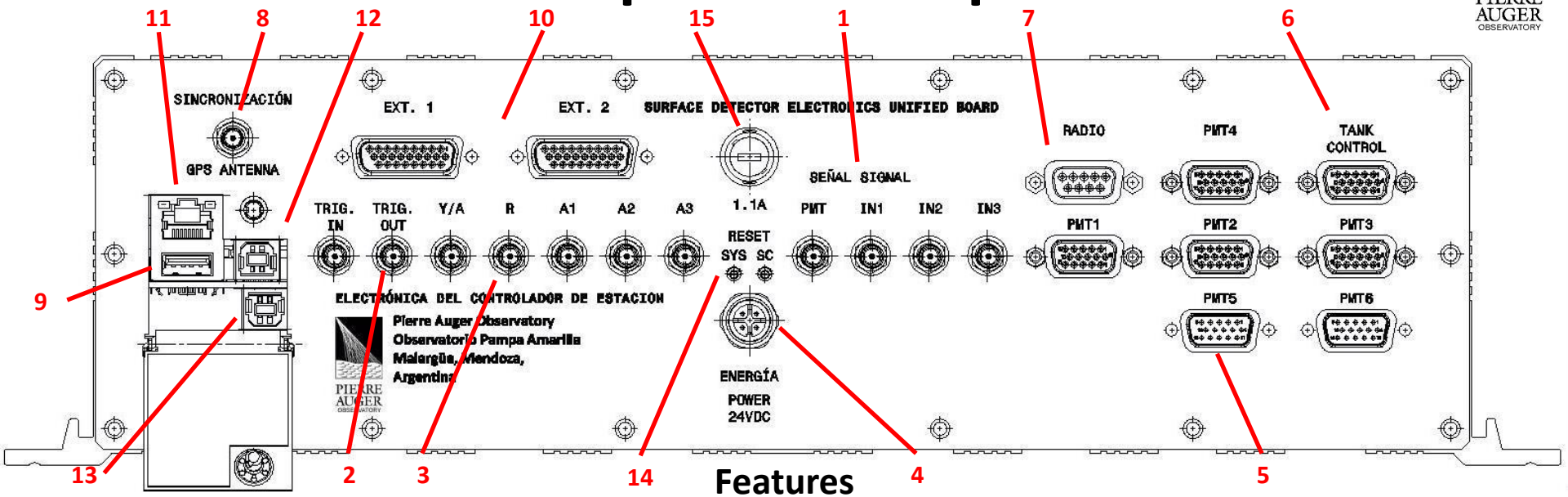
SDEU specifications

10x ADCs 12 bits 120 MS/s
Dual µ-processor ARM Cortex A9 333 Mhz
4 Gbits LP-DDR2 memory (Low Power DDR2)
1 Gbits Flash memory (storage memory)
i-LOTUS GPS
LINUX
Online VHDL & software updatable
Industrial power supply connector (IP67)
Ethernet (Front panel)
Master USB 2.0(to add an external electronic)
Slow-control and system USB control consoles interface

SDE input/output connectors

Existing UB	Upgraded UB
6 analog inputs (6 ADCs)	6 or 7 analog inputs (5x twin ADCs = 10x ADCs)
3 PMT control	6 PMT control
Ext control	Ext control
Trigger out signal	Trigger out signal
-	Trigger in signal
Power supply	Power supply (new connector)
2 switches	2 switches
2 LED-flasher control	2 LED-flasher control
"TEST" connector	-
"Console" connector	"Sys" connector with USB interface
	"Slow-Control" connector with USB interface
"Radio" connector	"Radio" connector
-	Ethernet 10/100/1000 Bits/s(Front panel)
-	Master USB 2.0 (Front panel)
	2x D-SUB 26 External extension connector (LVDS)

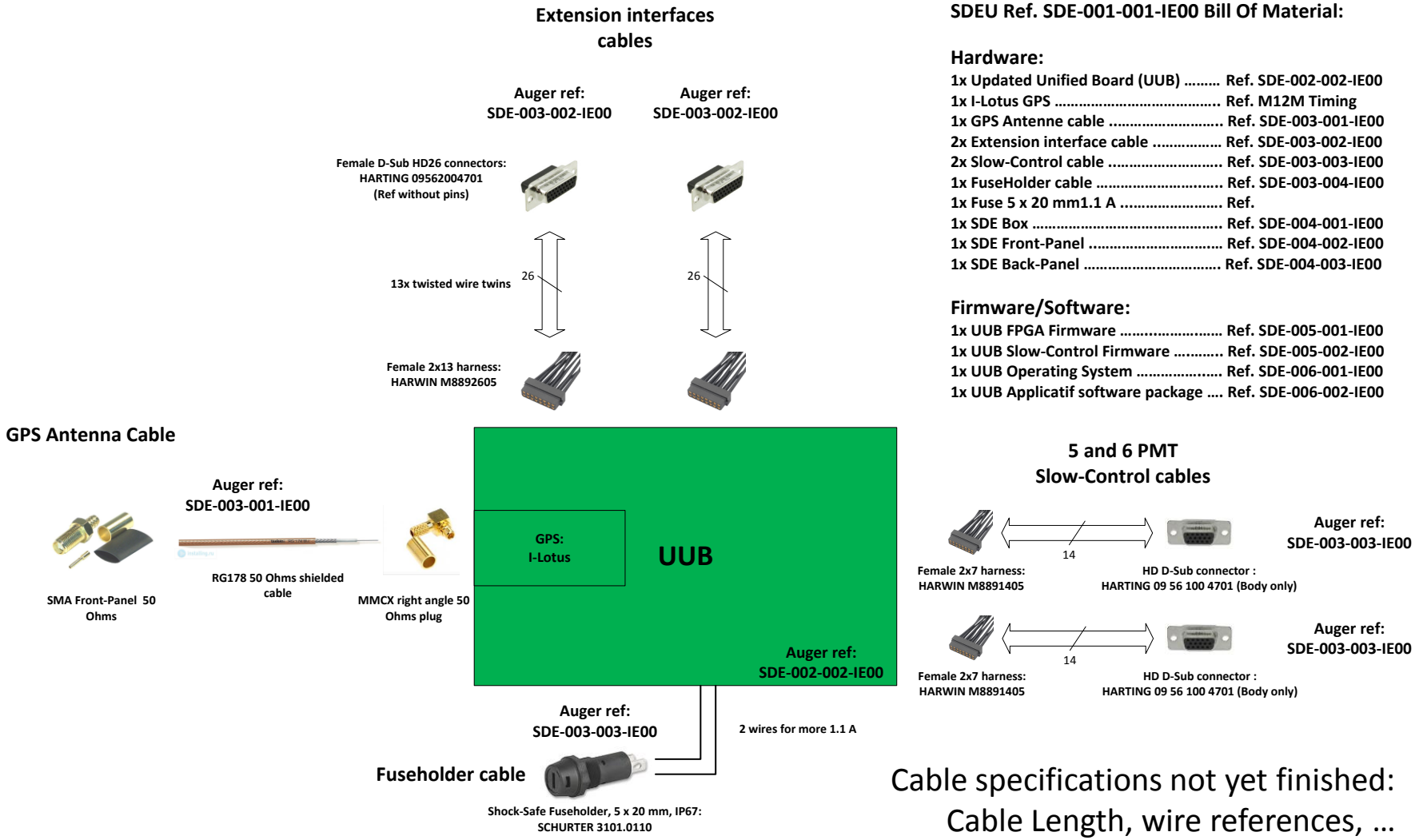
Front panel description



Features

1	7x Analogs inputs 12 bits@120MS/s and 3 of them 2x ADCs per input.
2	Digital input trigger and output trigger.
3	2x LED Flasher control
4	24 Volts Power supply .
5	**6X** PMT control.
6	Tank control.
7	RS-232 Radio connector.
8	GPS antenna connector.
9	USB 2.0, for external devices (0.5 Watts max.).
10	External extension connector. Works with an external electronic (19-32 Volts no regulated). 8 LVDS bits
11	Ethernet 10/100/1000 Mbits/s.
12	System Terminal (UART to USB interface inside).
13	Slow-Control Terminal (UART to USB interface inside).
14	2x RESET switches, System and Slow-control.
15	Fuse holder (1,1 A fuse).

Integration SDEU schematic



SDEU Ref. SDE-001-001-IE00 Bill Of Material:

Hardware:

1x Updated Unified Board (UUB) ..... Ref. SDE-002-002-IE00
1x I-Lotus GPS ..... Ref. M12M Timing
1x GPS Antenne cable ..... Ref. SDE-003-001-IE00
2x Extension interface cable ..... Ref. SDE-003-002-IE00
2x Slow-Control cable ..... Ref. SDE-003-003-IE00
1x FuseHolder cable ..... Ref. SDE-003-004-IE00
1x Fuse 5 x 20 mm1.1 A ..... Ref.
1x SDE Box ..... Ref. SDE-004-001-IE00
1x SDE Front-Panel ..... Ref. SDE-004-002-IE00
1x SDE Back-Panel ..... Ref. SDE-004-003-IE00

Firmware/Software:

1x UUB FPGA Firmware ..... Ref. SDE-005-001-IE00
1x UUB Slow-Control Firmware ..... Ref. SDE-005-002-IE00
1x UUB Operating System ..... Ref. SDE-006-001-IE00
1x UUB Applicatif software package .... Ref. SDE-006-002-IE00

Cable specifications not yet finished:
Cable Length, wire references, …

Absolute peak power estimate detail

Work Package	Function	Device	Maximum current (mA) / power supply (V) / Device										Max Power / Device	Nb.	Power	Power / WP
			FPGA				Slow C	Analog		GPS	USB	Radio	PMT				
			1	1,2	1,8	3,3	3,3	3,3	-3,3	5	5	12	12				
WP1	Front-End	Anti aliasing filter (TBD)						0						0	3	0,00	
		Low-gain path filter proposal						0	0					0	3	0,00	
		High-gain path filter proposal						0	0					0	3	0,00	4514,70
		Dual Differential amplifier (ADA4927-2)						47,2	47,2					311,52	10	3115,20	
		12 bits ADC 120MS/s (Twin AD9628) proposal			155,5									279,9	5	1399,50	
WP2	Trigger	IN Digital Triggers (SN74LVC1G17)				0,5								1,65	1	1,65	
		OUT Digital Triggers (SN74LVC1G125)				0,5								1,65	1	1,65	56,10
		Test connector (32 signal,) (2x 74LCX16245)				8								26,4	2	52,80	
WP3	Time Tagging	GPS (I-LOTUS: ref ???)				52								171,6	1	171,60	301,60
		Antenna (Type II ref ???)								26				130	1	130,00	
WP4	Slow Control	µ-controller (MPS430F2618)					9,5							31,35	1	31,35	
		LED flasher controller (DAC 4 outputs : AD5624)					0,85							2,805	1	2,81	
		DAC (LTC2637-12)					1,3							4,29	1	4,29	67,55
		Ampliers (LT1112)					0,88							2,904	10	29,04	
		MUX (ADG608)					0,01							0,0165	4	0,07	
WP5	VCO/ fanout/ Clock_ADC	**Clock generator (with VCO control) & DAC :**															
		Clock generator with external VCO control (CDCEL913)			11,7									21,06	1	21,06	
		LVDS double fanout repeater (CDCUN1208LP)			85									153	1	153,00	
		DAC VCO control (AD7390 & REF3318: Rail to Rail)				1,5								4,95	1	4,95	
	FPGA (and µP)	Xilinx ZYNQ 7020 Industrial : 2 cores 333.5Mhz BRA	1864,8	150,15	432,6									2823,66	1	2823,66	
	Extention connector	**interface used an external electronic:**															
		Driver (2x DS90LV047ATM)				15								49,5	4	198,00	
		Receiver differential (DS90LV048ATM)				37								122,1	4	488,40	
	Watchdog/ RESET/ Clock CPU	WATCHDOG : MAX823EUK-S				0,012								0,0396	1	0,04	4799,96
		RESET : MAX811EUS-S				0,01								0,033	1	0,03	
		ABRACON ASE-50,000MHz-LC				19								62,7	1	62,70	
	Control	Switches												0	2	0,00	
	System Memory	LP-DDR2 Low Power4 Gb: MICRON MT42L128M32D1LF-25		210	10									270	1	270,00	
	Flash Memory	1 Gb : µ N25Q00AA13GSF40 @ 3.3 V (Wr cycle)				20								66	1	66,00	
	Interfaces	Radio RS232 (MAX3218)			3									5,4	1	5,40	
		Terminal USB interface (FT232R, powered by USB link)												0	2	0,00	
		Ethernet phy (MARVELL 88E1510 in EEE mode	14		35	14								123,2	1	123,20	
		USB (USB3320)			46,4									83,52	1	83,52	
		External Slave USB Power									100			500	1	500,00	
WP?	PMT 1,2 & 3 PMT	Main PMT											44,44	533,28	3	1599,84	
		Small PMT (ESTIMATE POWER)											44,44	533,28	1	533,28	5632,32
WP?	RADIO											291,6		3499,2	1	3499,20	
		Total Current / power supply (mA) :	1878,8	360,15	1401,2	331,522	20,47	472	472	26	100	291,6	177,76	**Total power (mW):**		**15372,23**	
		DC/DC efficiency (%) :	93,00	89,10	93,50	94,00	87,00	93,30	82,20	90,90	94,10						
		Power for under 7V power supply (mW) :	2020,22	485,051	2697,5	1163,85	77,6448	1669,45	1894,89	143,014	531,35						
		DC/DC efficiency (%) :	97,10%									97,50%	97,00%				
		Power (mW) :	11002,03									3588,92	2199,09				
		Internal Total Power (SDEU only) :	**16 790,04 mW**														
		Total Power (including 6,4 watts power for external devices) :	**23,19 W**														

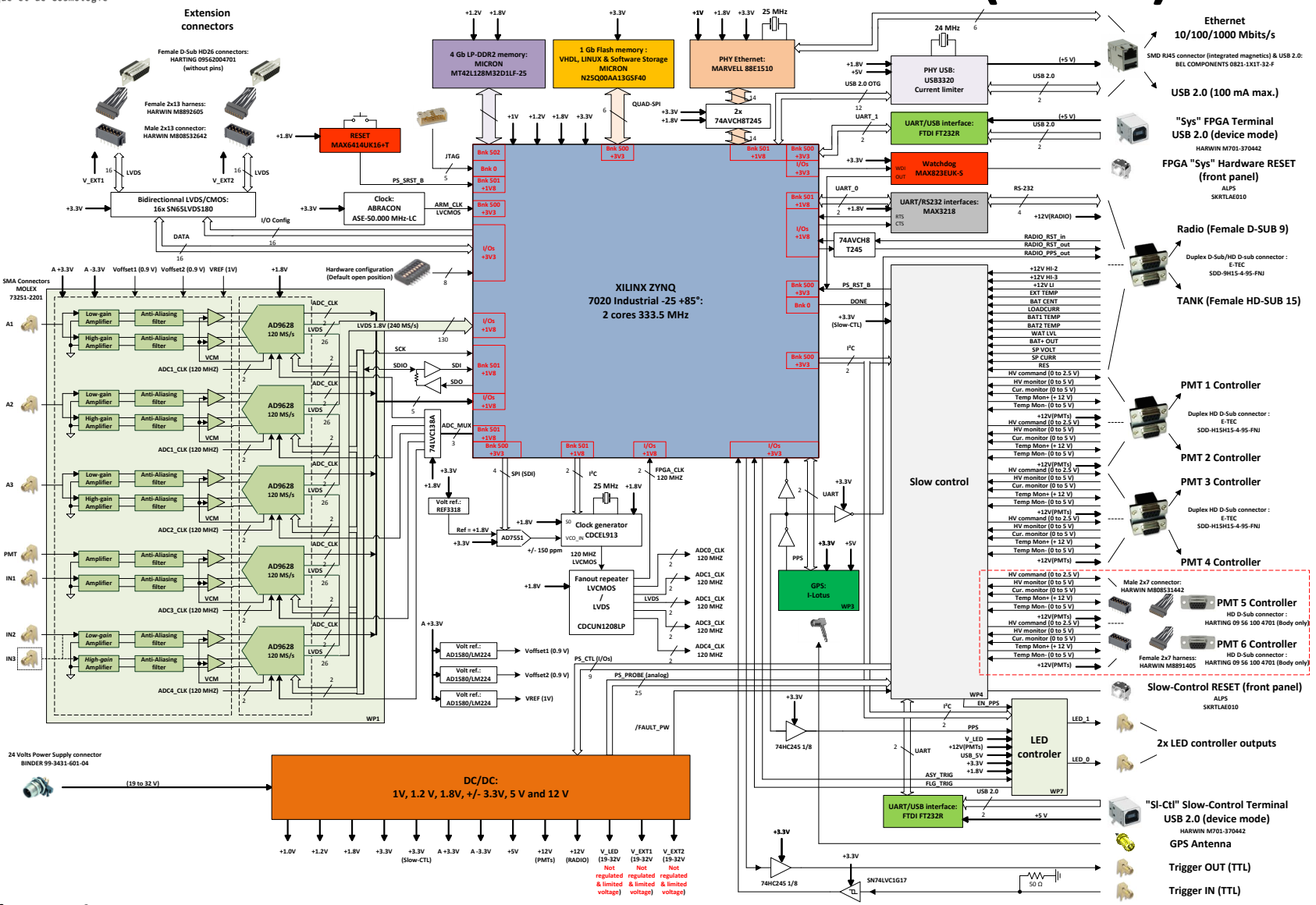
Electronics Dept.

Eric LAGORIO – WP5 – eric.lagorio@lpsc.in2p3.fr - LPSC Grenoble – SDEU CDR, Orsay, 4th February 2015

Absolute peak power estimate resume

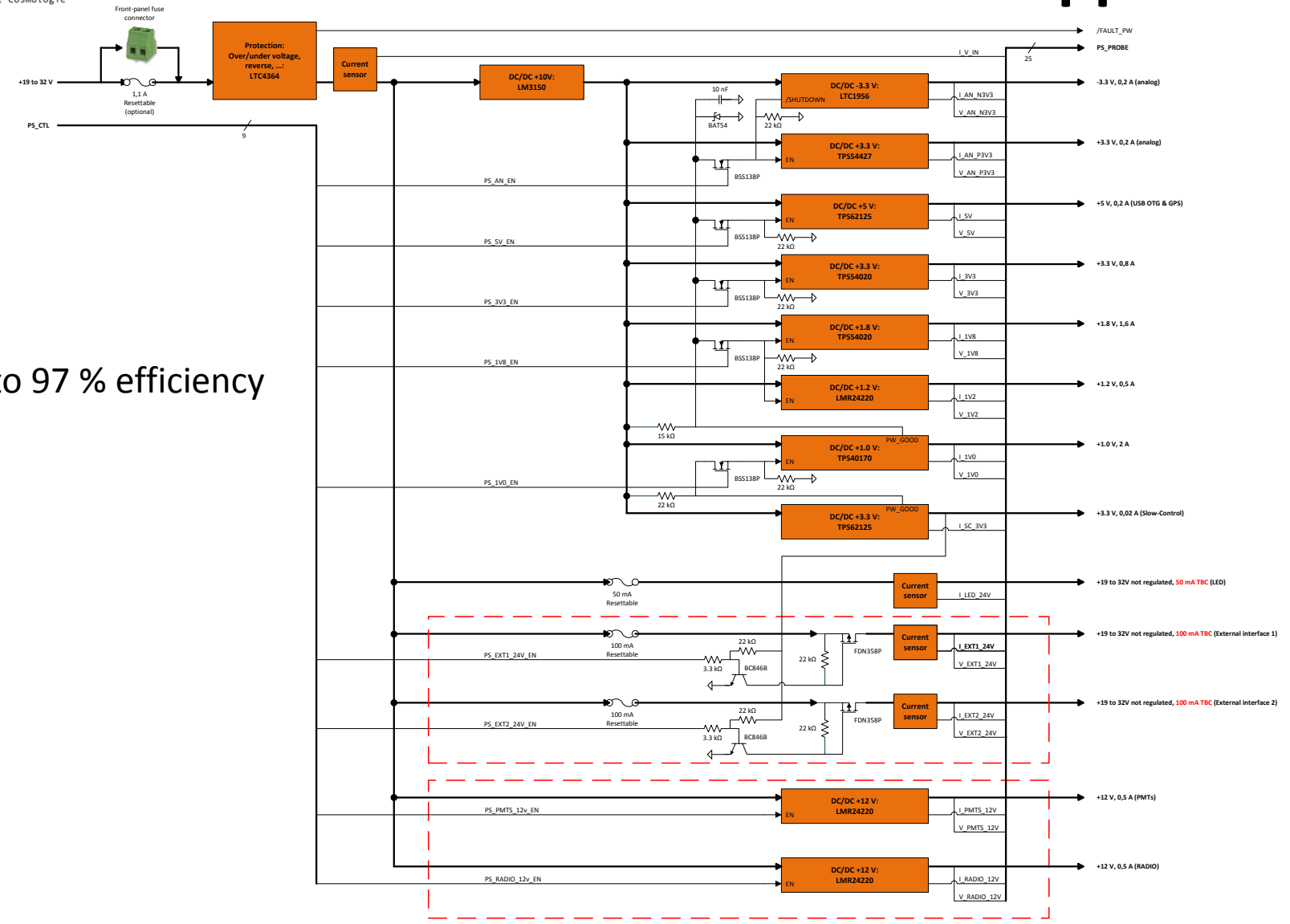
WP1 - Front-end :	4514,70 mWatts (**TBC**).
WP2 - Trigger :	56,10 mWatts.
WP3 - Time Tagging :	301,60 mWatts.
WP4 - Slow Control :	67,55 mWatts.
WP5 - FPGA, Processor, … :	4799,96 mWatts (**S/w dependent**).
PMTs & Radio :	5632,32 mWatts.
Total without power supplies (97%) :	15372,23 mWatts
Total:	**16790,04** mWatts
Power provided to external electronics:	6400 mWatts

UUB block Schematic – main (v1.10)

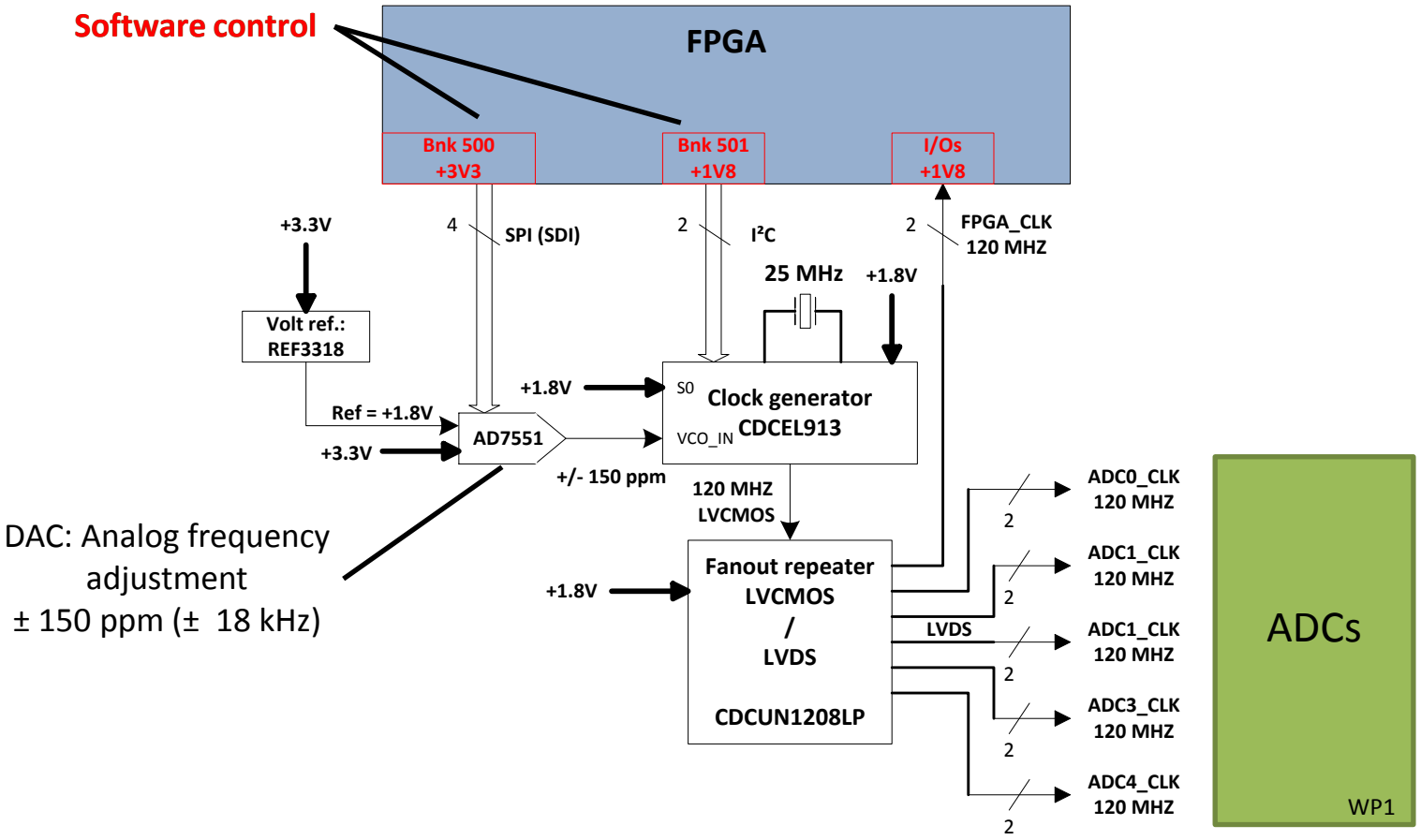


Global UUB Schematic – Powers supplies

Up to 97 % efficiency



Clock generator



ADCs (WP1) interfaces

Data stream from ADCs:
12x data bits, 1x Over Range signals in LVDS technology

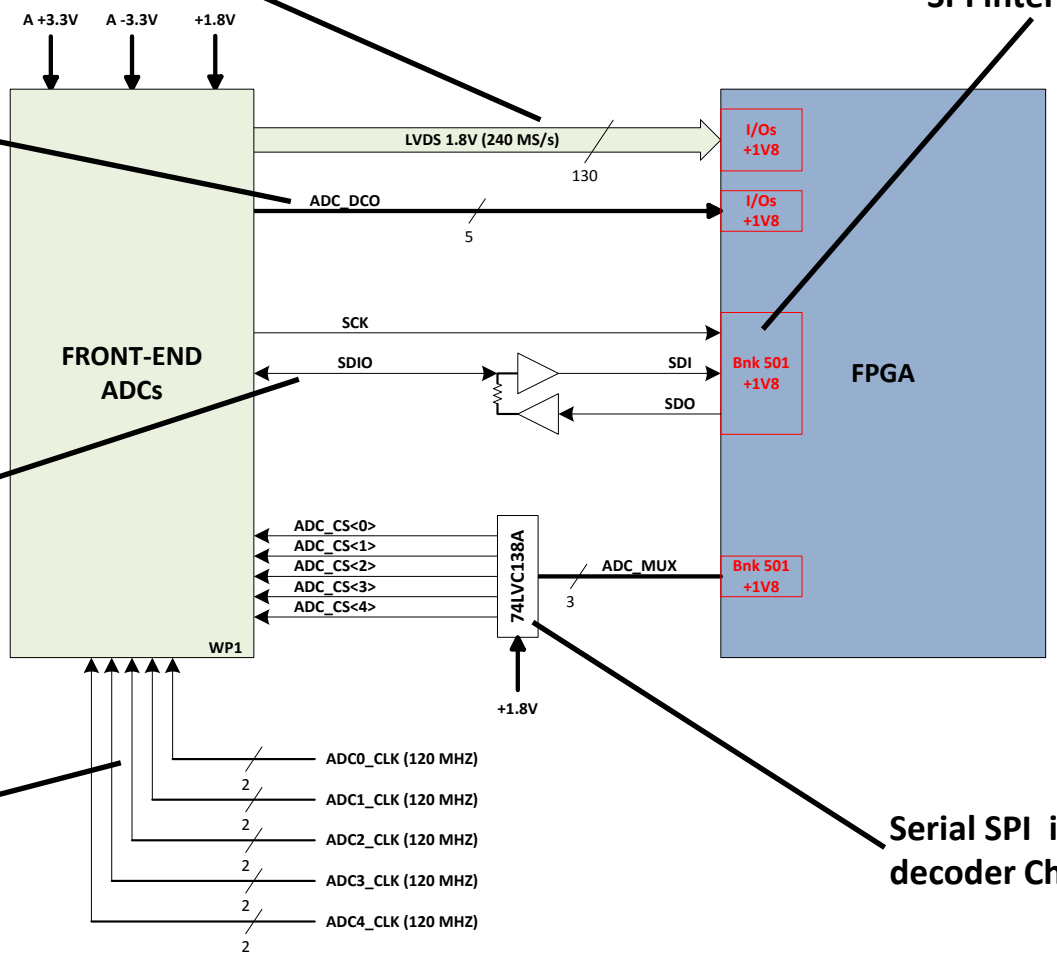
LVDS ADC output data clocks from each ADC component. In the layout but they shouldn't need to be used.

Serial SDIO interface for ADCs configuration and test (Output mode LVDS, delay, common voltage, …)

LVDS clock signals from the clock generator block (120 MHz)

Standard Serial SPI interface

Serial SPI interface decoder Chip Select

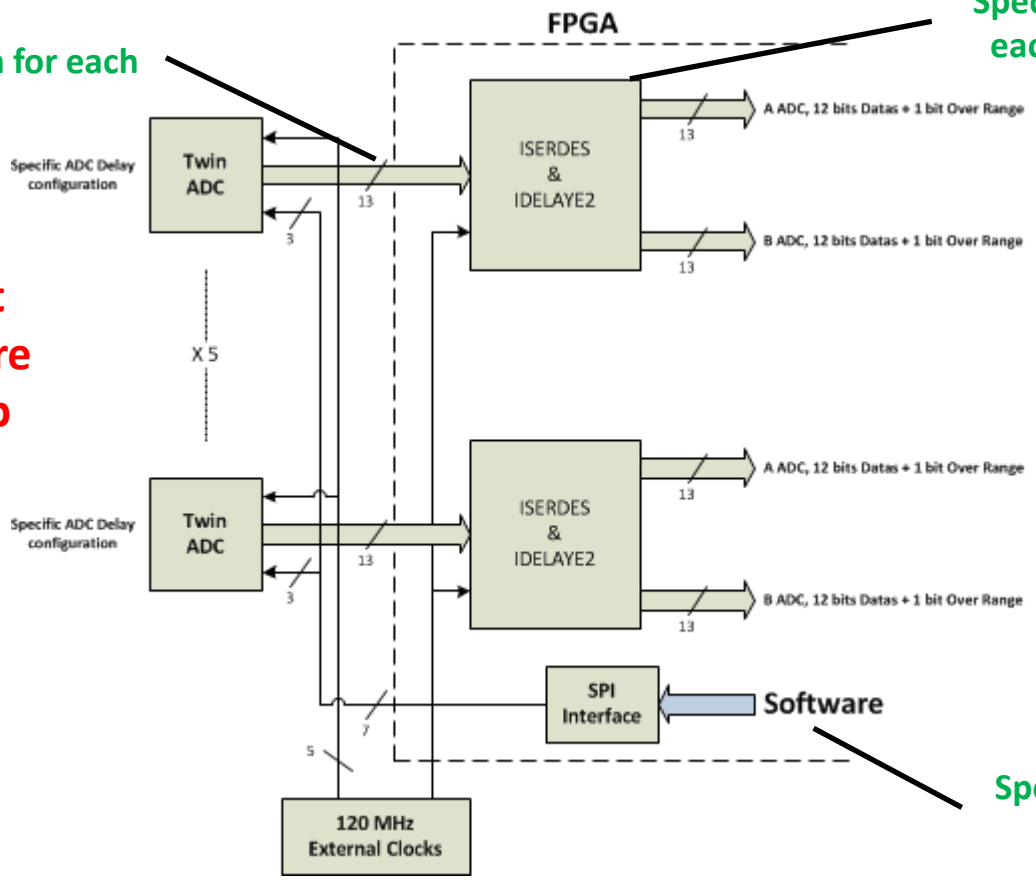


ADCs data stream synchronization

- Main Xilinx project made with Evaluation board constraint.
- Data stream interface: Simulation made, test on evaluation board (1x ADC) but must test with the prototype (5x ADCs).

Specific wire length for each twin ADCs

Specific " fixe " delay for each twin ADCs inside

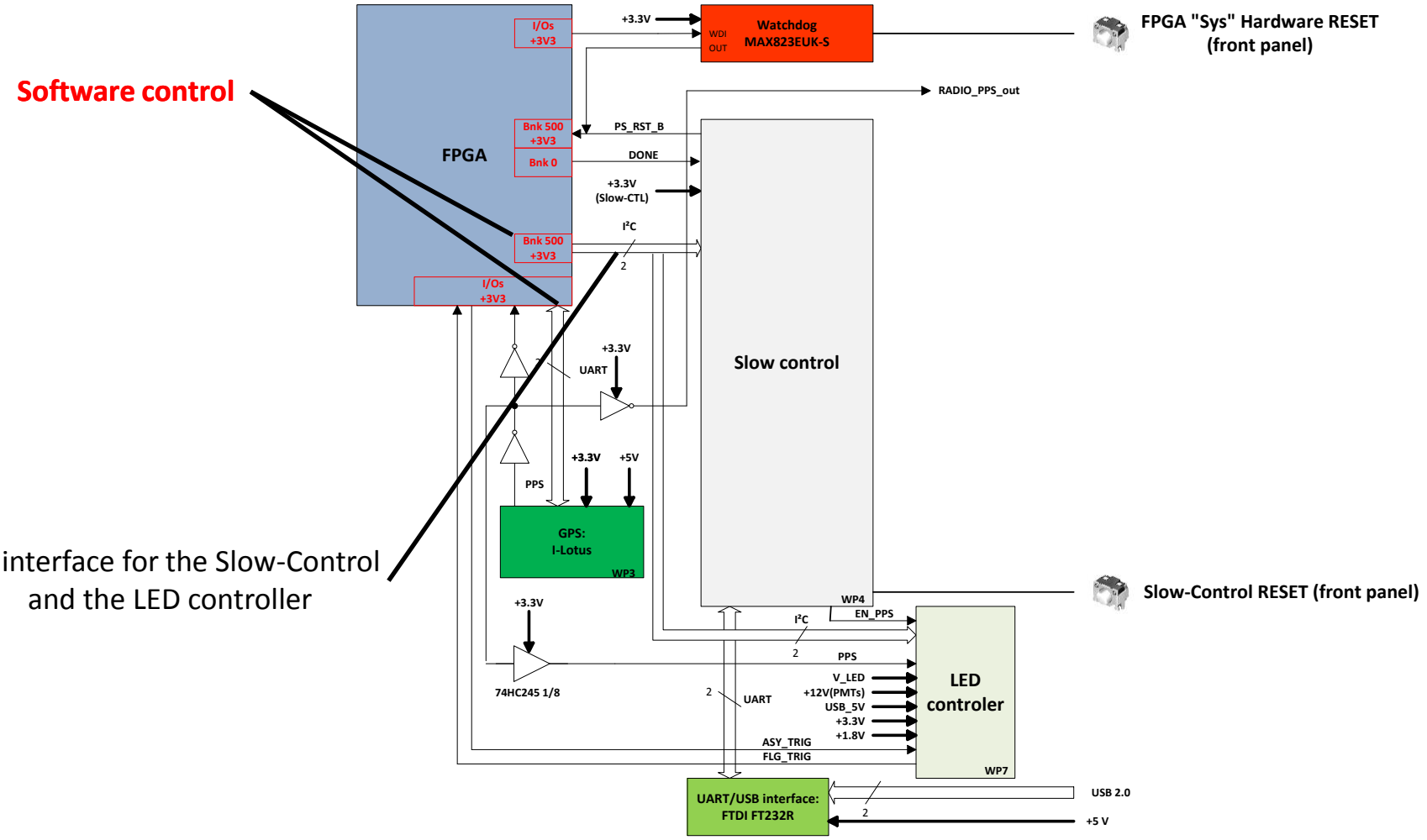


Data alignment made by software when power-up

Output data synchronized with 120 MHz external clock

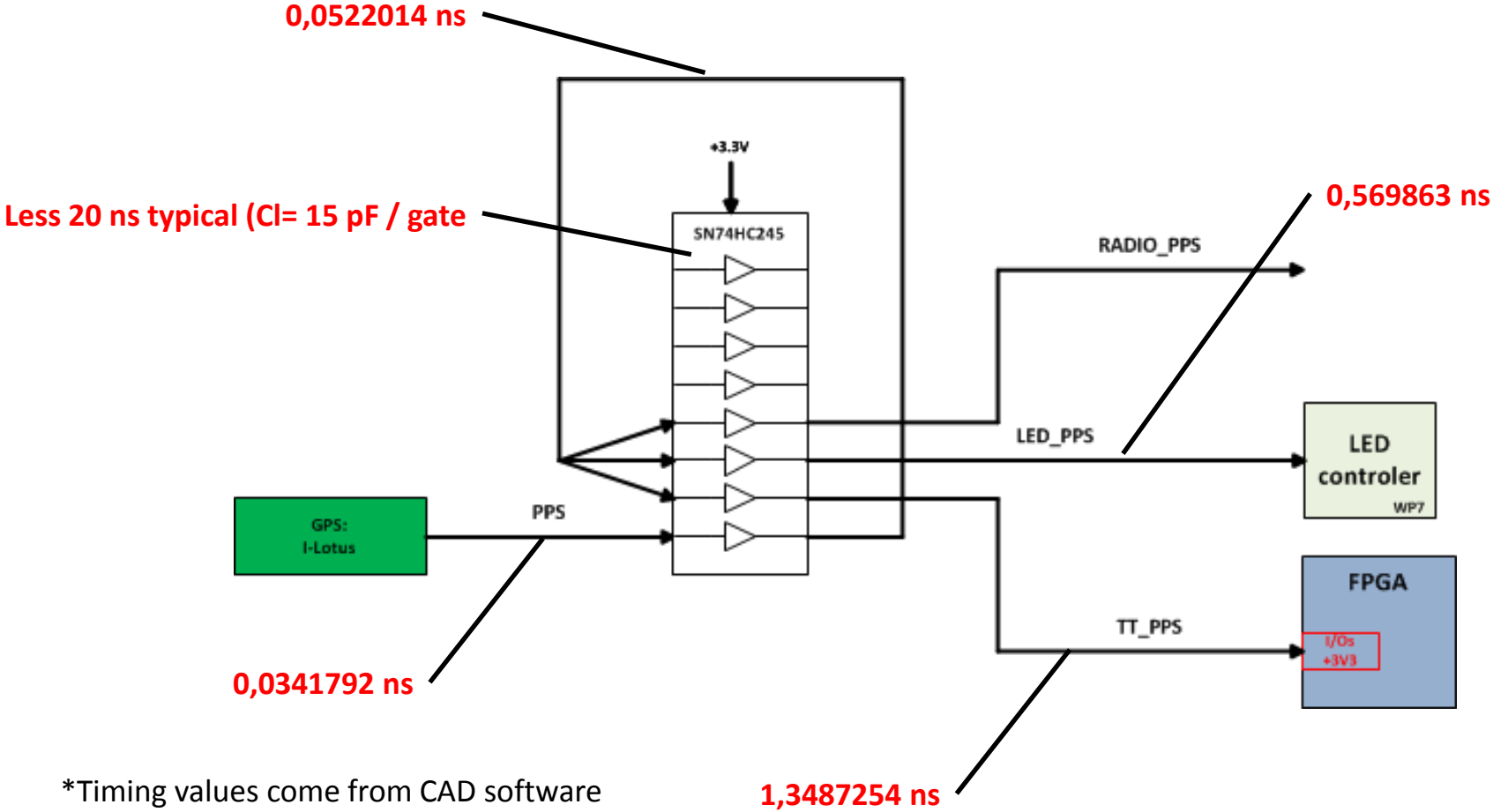
Specific "adjusted" delay for each twin ADCs inside

Hardware description
Slow-control, LED controller & GPS interfaces



PPS signal

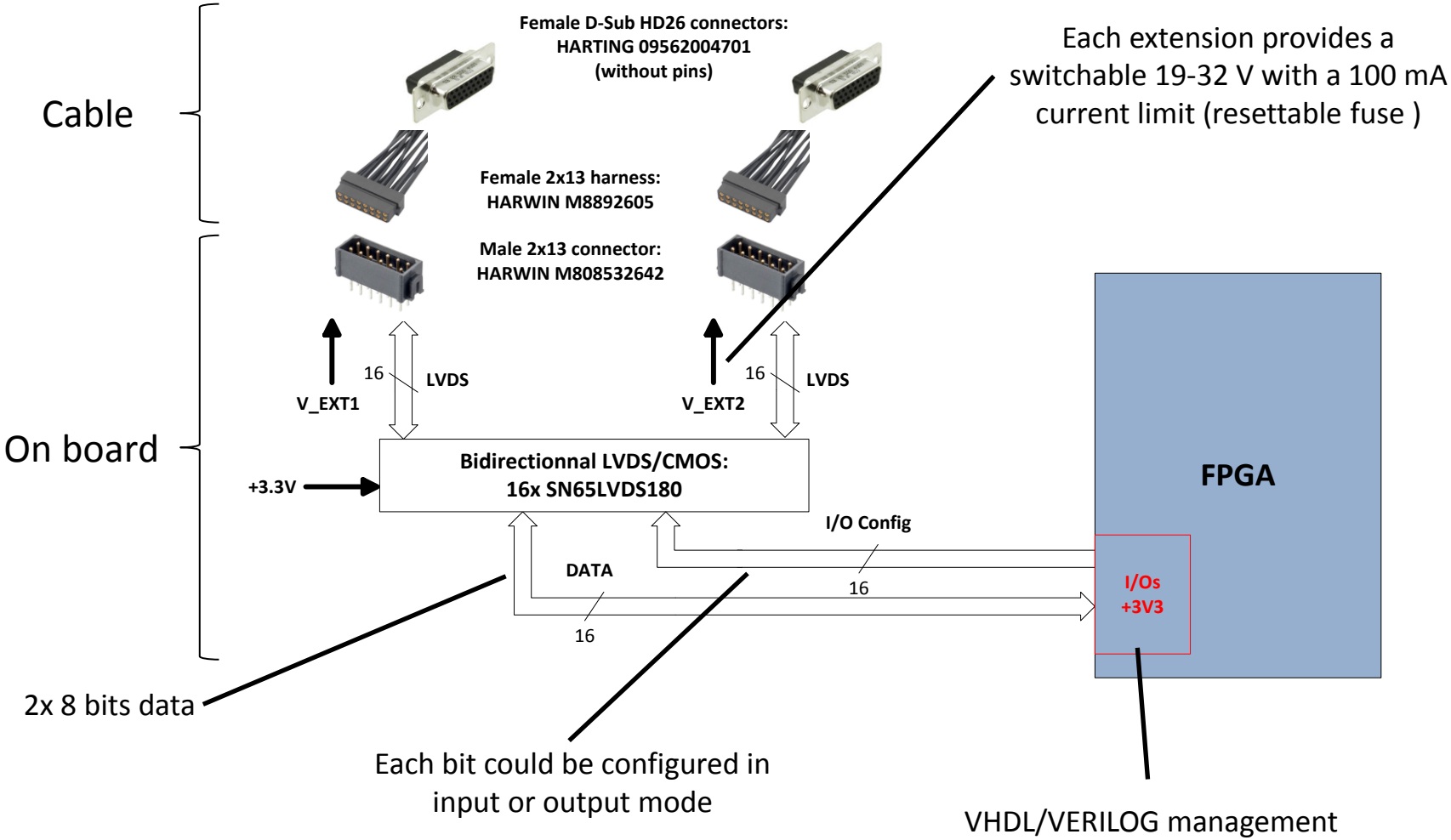
- Same schematic as the present SDE.
- Each PPS outputs use the same gate number in the same component.



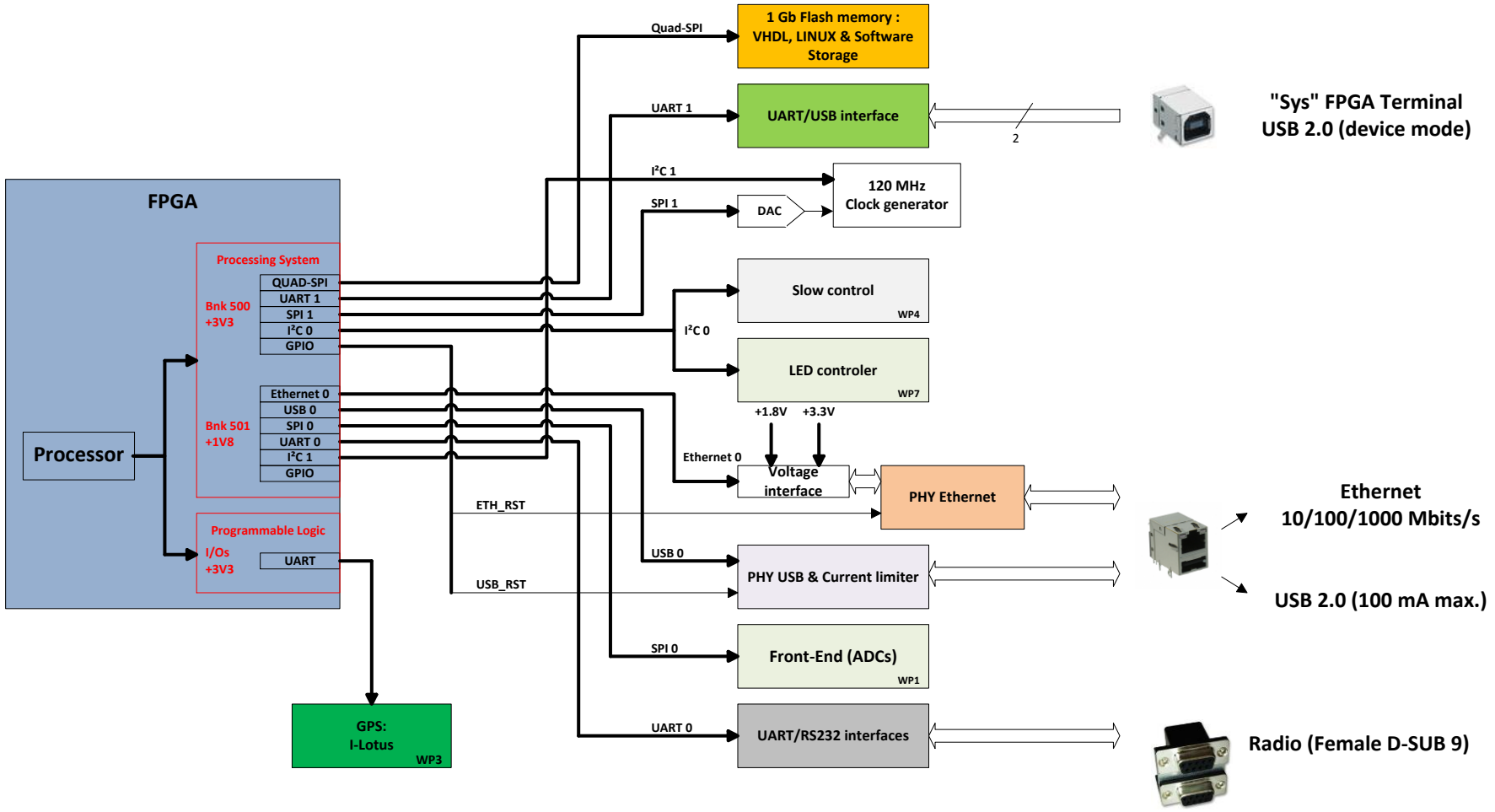
*Timing values come from CAD software

Electronics Dept.

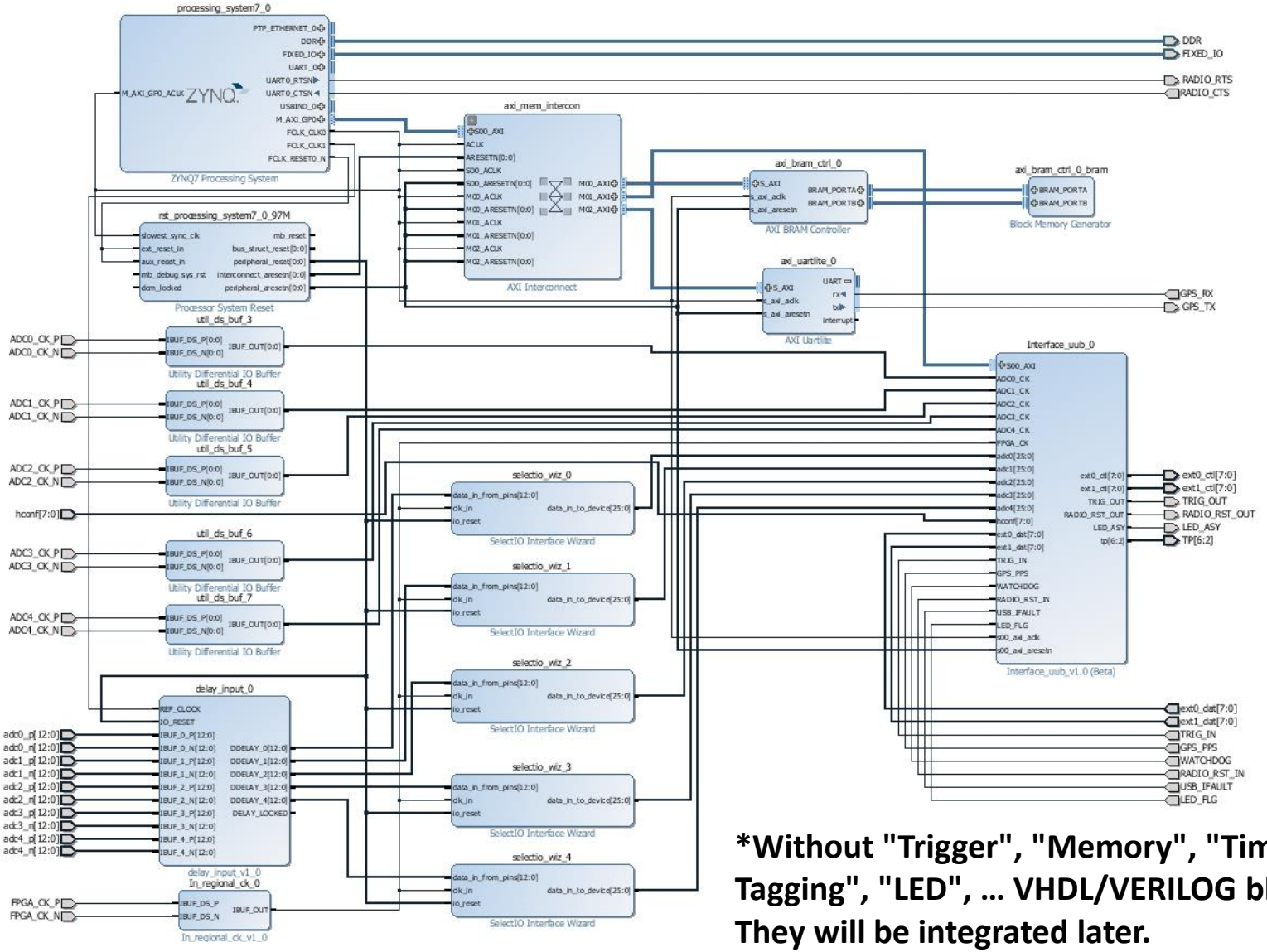
Extension connector interfaces



Devices managed by the processor

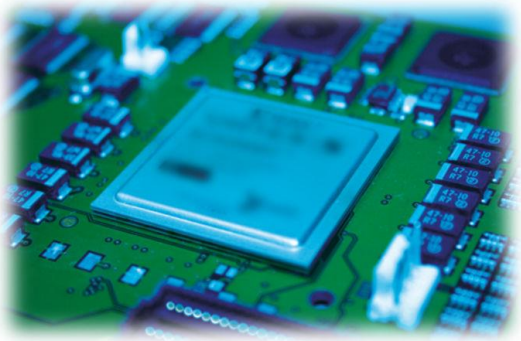


Firmware block schematic*



***Without "Trigger", "Memory", "Time-Tagging", "LED", … VHDL/VERILOG blocks They will be integrated later.**

Design layout requirements



Layout design:

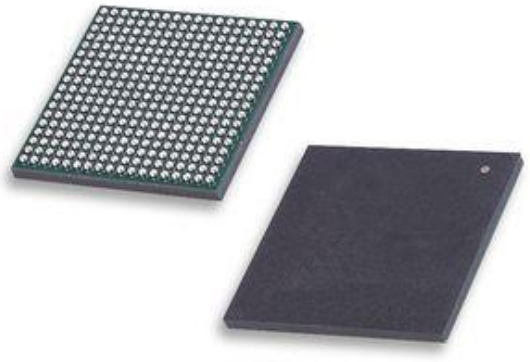
- LVDS: wire adapted 100 Ohms .
- Analog & trigger signals : 50 Ohms adapted.
- LP-DDR2 : 50 Ohms adapted.
- Same wire length between each ADC Clock and between each ADC data.

Electronic board:

- Class: 6
- 10 layers (symmetric)
- Size: 340 x 240 x 1,8 mm (maybe smaller)
- Tropical coating.

Top	Signal (adapted)
GND 1	Gnd layer
Int 1	Signal (partial adapted)
Power 1	Power layer
Int 2	Signal
Int 3	Signal
Power 4	Power layer
Int 4	Signal (partial adapted)
GND 2	Gnd layer
Bottom	Signal (adapted)

Component specifications



Global specifications:

- Available components for production up to 2020.
- Operating Temperature range: -20° to +70° C.
- RoHS compliant.
- No pending obsolescence components (warning: Obsolete components could be available).
- Standard Resistor: 1% tolerance.
- Optimized resistor and capacitor values.

Package:

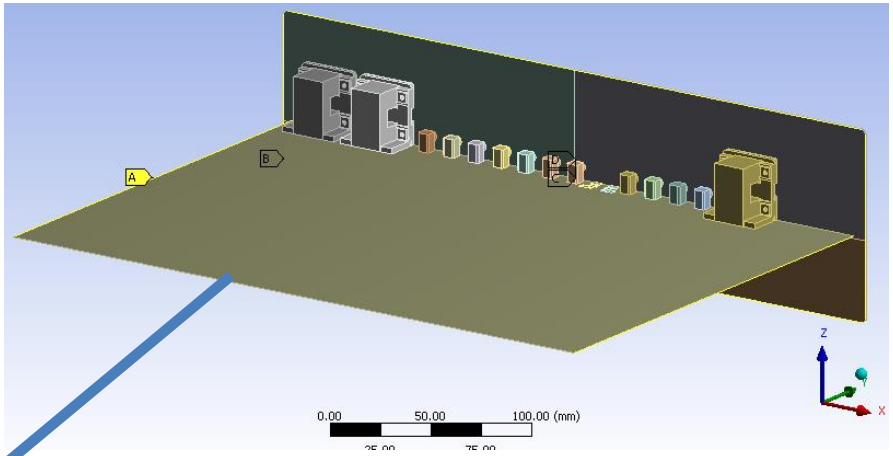
- SMD packages privileged. Connector could have through-hole.
- Passive components (standard resistors & capacitors): 0603 package (down to 0402 for WP1 & WP5).
- Preferred PQFP, SSOP, SO, … instead of QFN & BGA packages.

Mechanical UUB data

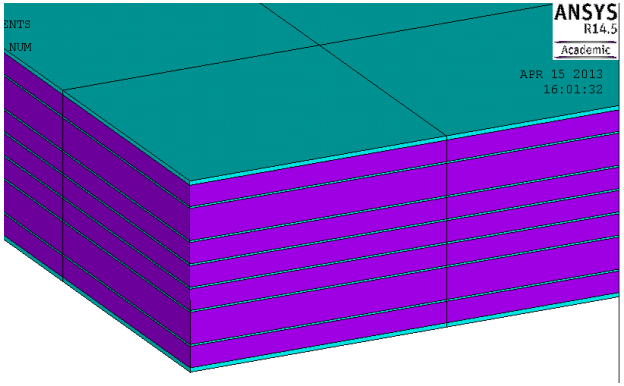
PCB configuration:

Global Thickness:	Layer Name:	Thickness:	N° layer	Matière
1.785 mm	TOP	40 µm	1	COOPER
		200 µm	2	FR4
	GND 1	17.5 µm	3	COOPER
		300 µm	4	FR4
	PWR1	17.5 µm	5	COOPER
		200 µm	6	FR4
	LAYER 1	17.5 µm	7	COOPER
		200 µm	8	FR4
	LAYER2	17.5 µm	9	COOPER
		200 µm	10	FR4
	PWR 2	17.5 µm	11	COOPER
		300 µm	12	FR4
	GND2	17.5 µm	13	COOPER
		200 µm	14	FR4
	BOTTOM	40 µm	15	COOPER

*Today, 10 layers

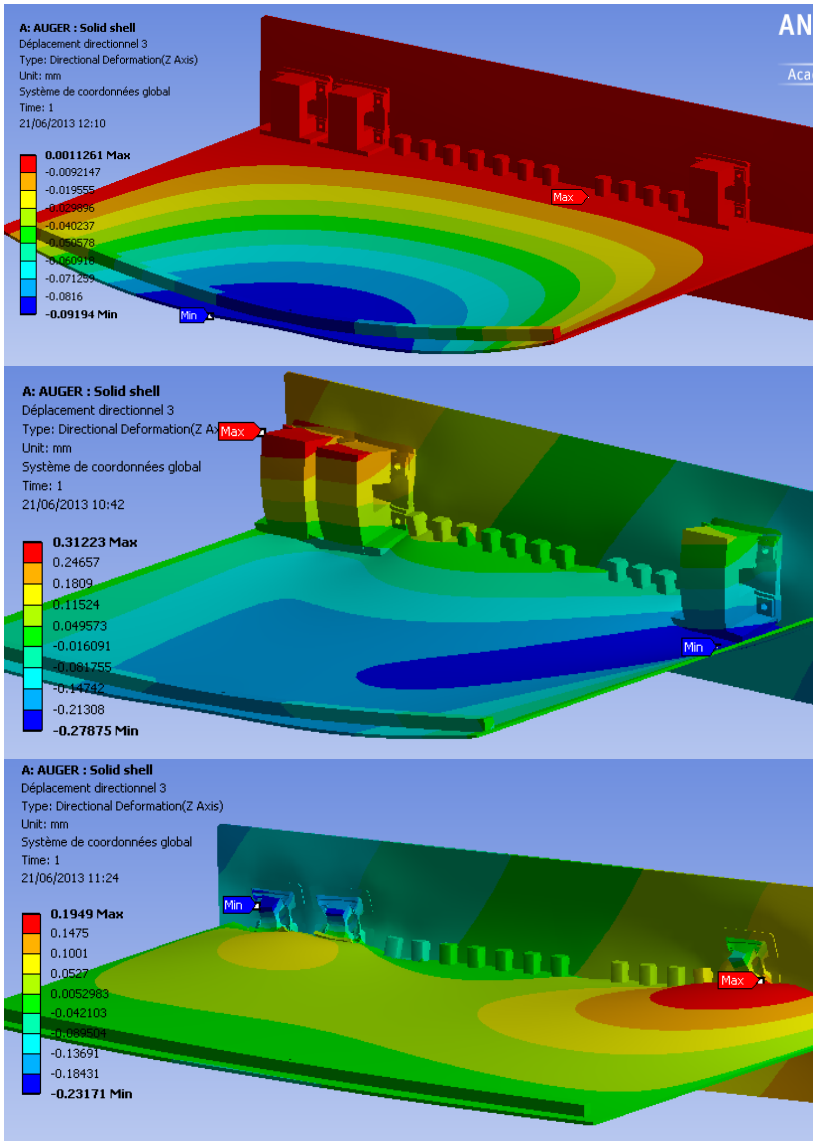


Layers defined in continuous plane



Max : +40.6°c (Could be up to 60°c in the box)
Min : -7.8°c => -10°c
Variation : 68.4° => 70°c
Coef. dilatation FR4 => 11 10^{-6}
Coef. dilatation Cu => 17 10^{-6}
Longer size : 340 mm => with 70°c => 0.4 mm
Symmetric layers
Manufacturer tolerance : 1% 416 mm => 4,16 mm

New stiffener UUB move



UUB gravity :

New	Z = **-0,09** mm
Present	Z = -0,04 mm
Without	Z = **0,26** mm

UUB gravity at + 40 °c :

New	Z = **-0,46** mm
Present	Z = **-1,34** mm
Without	Z = -0,63 mm

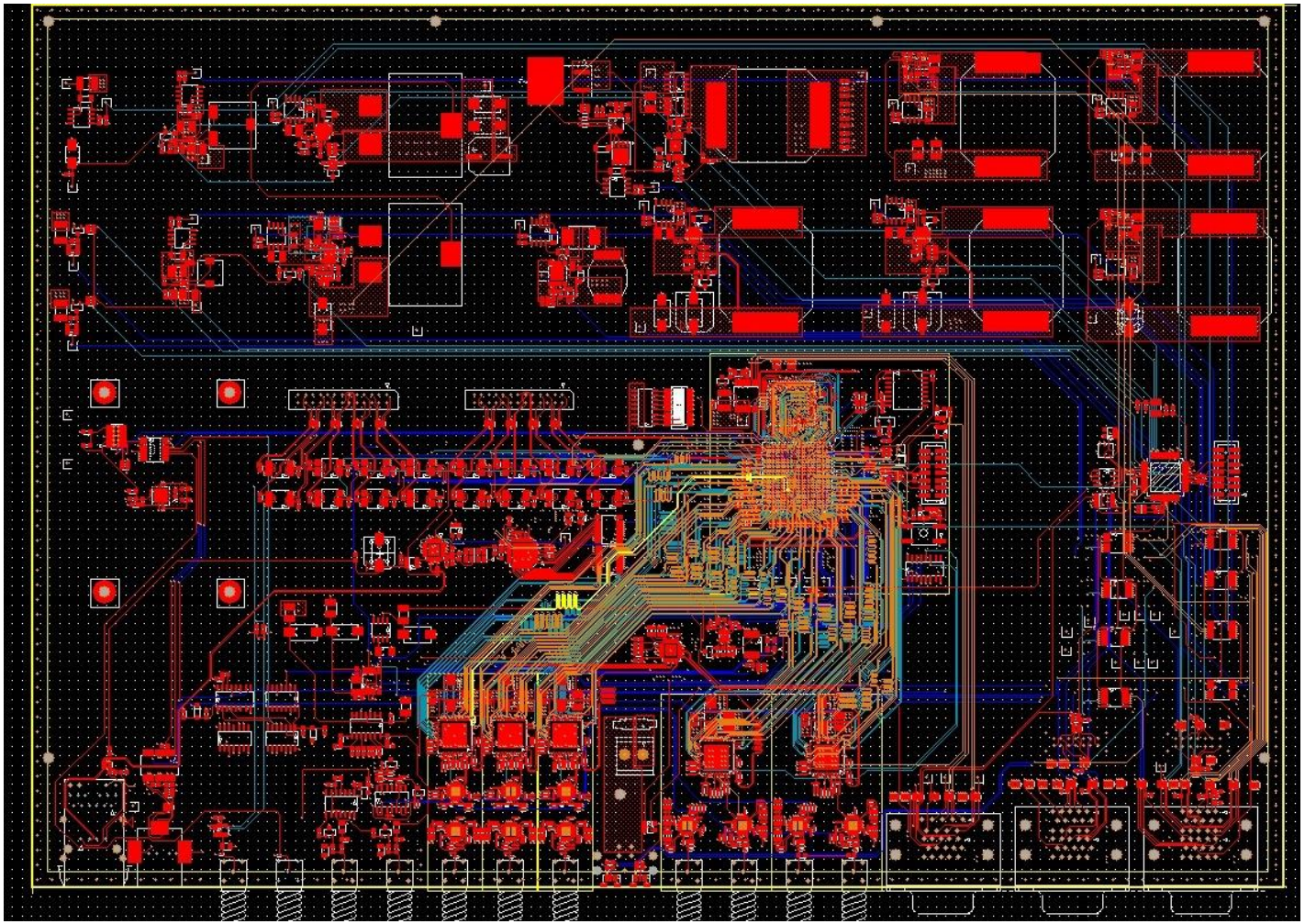
UUB gravity at - 30 °c :

New	Z = **0,43** mm
Present	Z = **+1** mm
Without	Z = 0,48 mm

Z value are given for entire board

SDE Layout

PCB files will be ready middle February, after WPs validation:



Test & Status

Tested & validated:

- Power supplies.
- VHDL firmware integration by JTAG probe.
- EEPROM was programmed and the FPGA was rebooted with it.
- LP-DDR2 memory.
- SPI, I^2C, UART.
- Clock generator configuration and analog frequency modification.
- ADCs configuration. ADC Auto-delay data system when the electronic starts.
- *.XDC Xilinx Definition Constraint files (FPGA pinout & level technology timing).
- CAD layout, Bill Of Material integration and components optimization.

Status:

- FPGA, **I/Os used at 98% (4 I/Os free)**.
- VHDL/Verilog integration could be difficult.

Preview SDEU